Electronic, Magnetic, Superconducting, and Neuromorphic Devices

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100-nm Channel Length E-mode GaN p-Channel Field Effect Transistor (p-FET) on Si Substrate

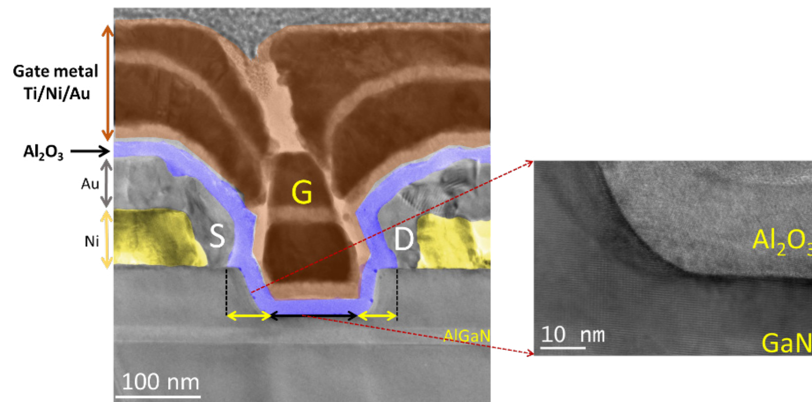
N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

GaN-complementary circuit technology could be instrumental towards realizing high-power-density, high-speed, low-form-factor, and highly efficient power electronic circuits, which has sparked many efforts to develop a high performance GaN p-channel field-effect transistor (p-FET). However, most of these demonstrations show normally-ON operation with ON-resistance over 1 kΩ·mm. The GaN/AlInGaN heterostructure-based p-FET shows low ON-resistance because of higher 2-DHG density and hole mobility but with D-mode operation. A GaN/AlN heterostructure-based p-FET shows enhanced-mode (E-mode) operation with R_{ON} of 640 Ω·mm. However, n-FET integration with this p-FET requires regrowth.

In this work, we demonstrate a self-aligned p-FET with a GaN/$Al_{0.2}Ga_{0.8}N$ (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on Si substrate. The utilization of a GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionality.

While most of the GaN p-FET demonstrations so far in the literature focus mainly on recessed gate metal-insulator-semiconductor FET (MISFET) structure, we choose to develop a self-aligned structure (see Figure 1 for the device structure) as it offers the following advantages over a recessed gate MIS p-FET: (1) the shortest possible source to the drain distance, cutting down the access region; (2) low ON-resistance because of negligible access resistance; and (3) easier gate alignment.

Our 100-nm-channel-length self-aligned device with recess depth of 70 nm exhibits a record ON-resistance of 400 Ω·mm and ON-current over 5 mA/mm with ON-OFF ratio of 6×10^5 when compared with other p-FET demonstrations based on a GaN/AlGaN heterostructure (see Figure 2 for benchmarking of our device with other p-FETs demonstrated in the literature). The device shows E-mode operation with a threshold voltage of −1 V, making it a promising candidate for a GaN-based complementary circuit that can be integrated on a Si platform. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated.



▲Figure 1: Transmission electron microscopy (TEM) image of the fabricated self-aligned p-FET with 100-nm channel length. TEM image showing the smooth interface between the GaN and gate dielectric attesting to the high quality of gate recess process with low surface roughness.

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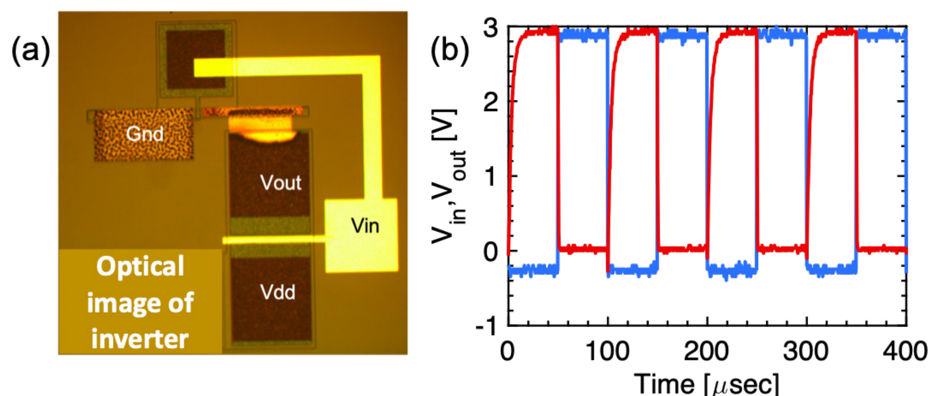
GaN CMOS Gate Driver for GaN Power Transistor

N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

In combination with its excellent transport properties, the high critical electric field of GaN, allows for GaN power transistors with much shorter drift regions and narrower gate widths than their Si or SiC counterparts. This allows for significantly lower gate capacitances and faster switching frequencies than traditional power switches at the same operating voltages. To take full advantage of the reduced gate capacitance and high switching speed of GaN power transistors, it is necessary to minimize parasitic inductances between the power switches/transistors and the gate driver circuit. For this, the GaN community has traditionally leveraged enhancement-mode/depletion-mode logic also known as direct coupled logic (DCL) to integrate relatively simple gate-driver circuits on the same chip as the GaN power devices; however, this technology suffers from significant power consumption and limited circuit design flexibility. To overcome these issues, recently there has been much research on a new all-GaN complementary technology that allows integration of high-performance n-channel and p-channel GaN enhancement-mode transistors on the same chip without the need for epitaxial regrowth. The epitaxial structure used for the demonstration of the all-GaN complementary technology consists of a GaN/AlGaN/GaN double heterostructure. This structure was grown by the company Enkris Semiconductor on 6” silicon wafers. Enhancement-mode p-type transistors were fabricated by contacting the two-dimensional hole gas at the top GaN/AlGaN interface while n-type devices are obtained by recessing the structure to allow direct ohmic contact connection to the two-dimensional electron gas at the bottom AlGaN/GaN interface. A simple gate driver with a 350-pF load is switched at 100-kHz frequency.



▲Figure 1: (a) Optical micrograph of an all-GaN complementary gate driver. (b) Input and output voltages for a 35-pF load.

FURTHER READING

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Self-Aligned p-FET with I_{ON}~100 mA/mm

N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

GaN-complementary circuit technology could be instrumental towards realizing high-power-density, high-speed, low-form-factor, and highly efficient power electronic circuits, which has sparked many efforts to develop a high performance GaN p-channel field-effect transistor (p-FET). However, most of these demonstrations show normally-ON operation with ON-resistance over 1 kΩ·m. In this work, we demonstrate a self-aligned p-FET with a GaN/$Al_{0.2}Ga_{0.8}N$ (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition on Si substrate. The utilization of a GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionality. While most of the GaN p-FET demonstrations so far in the literature focus mainly on a recessed gate metal-insulator-semiconductor FET (MISFET) structure, we choose to develop a self-aligned structure as it offers the following advantages over a recessed gate MIS p-FET: (1) the shortest possible source to the drain distance, cutting down the access region; (2) low ON-resistance because of negligible access resistance: and (3) easier gate alignment. The device with L_{SD}=200 nm shows a record combination of I_{ON}~50 mA/mm and ON-OFF ratio of 10^4 when compared with other p-channel transistor demonstrations. The device also exhibits enhancement mode operation with threshold voltage of -0.5 V. The best device shows a record current density of 100 mA/mm but at the expense of a lower ON-OFF ratio of 10^2. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated.

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Reliability of AlGaN/GaN-on-Si High-Electron-Mobility Transistors

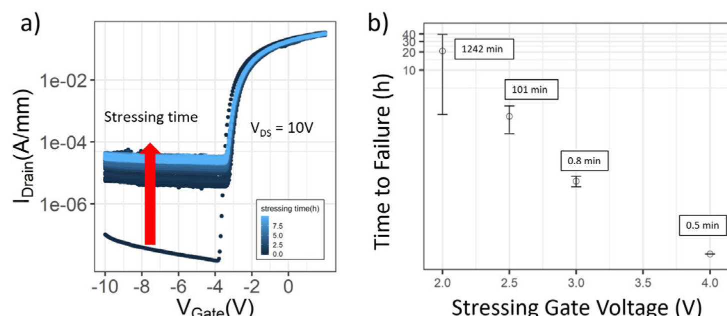
Y. Gao, W. A. Sasangka, C. L. Gan, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology Center

AlGaN/GaN high-electron-mobility transistors (HEMTs) are of interest for high-frequency and high-power applications such as in 5G networks and autonomous vehicles. Fabrication of GaN-based devices on silicon substrates can lead to reduced costs as well as enable monolithic integration of Si-complementary metal-oxide-semiconductor devices with GaN HEMTs. However, due to the large mismatches in lattice constant and coefficient thermal expansion between GaN and Si, GaN-on-Si HEMTs face challenges in terms of long-term reliability.

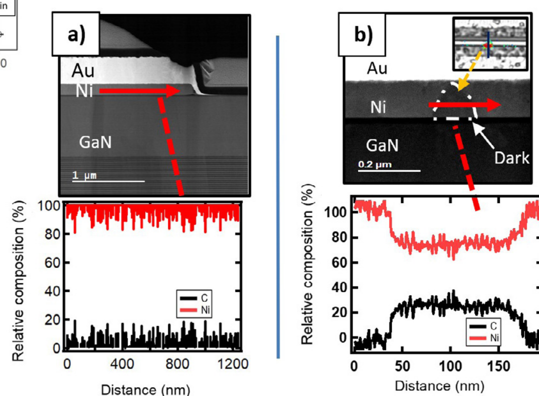
Our previous work has focused on degradation of the maximum drain current observed after off-state and on-state stressing in reverse or zero gate bias conditions. Decreases in the drain current, I_D, and increases in the gate leakage current, I_G, were found to be associated with electrochemical oxidation and pit formation at the gate edges. This degradation can be suppressed by using high-density passivation layers, reducing the threading dislocation density and reducing oxygen impurities at the GaN-cap/passivation layer interface.

Given that HEMTs also operate in forward gate bias, we have more recently focused on forward-bias stressing of research-grade HEMTs by setting the gate bias $V_{G\text{-}stress}$ at 2, 2.5, 3, or 4 V with $V_D = V_S = 0$ V. I_D vs. V_G measurements were made at time increments during testing. As shown in Figure 1(a), the drain saturation current and threshold voltage do not change significantly over time while the leakage current increases dramatically. Moreover, increasing the stressing voltage highly accelerates this degradation (Figure 1(b)). This increase in the leakage current was accompanied by a decrease of the Schottky barrier height and an increase in the ideality factor, suggesting the degradation likely occurred at the Schottky gate contact.

Further analysis using photon emission microscopy (PEM), transmission electron microscopy (TEM), and electron energy loss spectroscopy (EELS) revealed that carbon impurities in the gate metal layer (nickel) were responsible for this degradation (Figure 2(a) and 2(b)). The carbon impurities likely originated from photoresist residues from the gate lift-off process.



◀ Figure 1: (a) Typical ID-VG characteristics over time for a device stressed at VG-stress = 3 V. (b) The average device failure times at four different stressing voltages (Failure criterion: IDrain at -8.5 V = 12.5 μA/mm).



▶ Figure 2. EELS line scans for (a) a fresh sample and (b) a stressed sample (failed) at a hotspot region.

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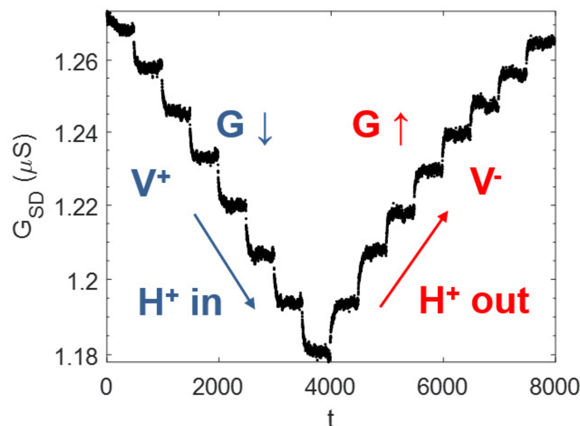
CMOS-Compatible Vanadium Pentaoxide-Based Programmable Protonic Resistor for Analog Deep Learning

N. Emond, M. Onen, J. Li, J. A. del Alamo, B. Yildiz
Sponsorship: MIT-IBM Watson AI Lab

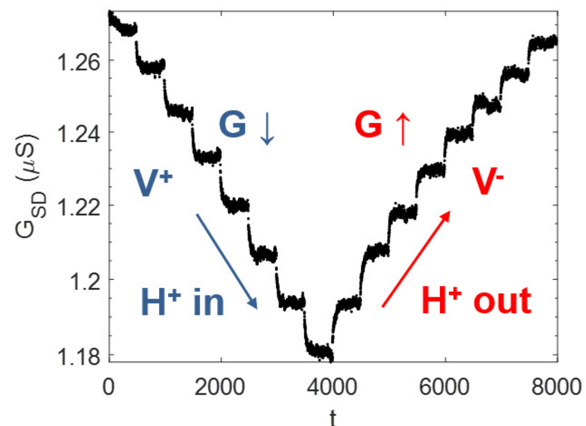
Deep learning proficiency in classification and clustering of data representations has fundamentally changed how information is processed. However, state-of-the-art digital processing units based on complementary metal–oxide–semiconductor (CMOS) circuits require large memory space and high power consumption to train deep neural networks. Improvements in computing performance therefore require designing novel scalable, fast, and energy-efficient hardware structures with both processing and storage capabilities using analog crossbar arrays.

The building block of these arrays is a programmable, non-volatile resistor, which should display multiple conductance states that are modulated reversibly, symmetrically, and reproducibly. Several device technologies, based mainly on filamentary conduction and phase-change mechanisms, have been proposed for analog deep learning; none of these however yet meets all device performance requirements. A recent concept, ion intercalation in transition-metal oxides, can potentially circumvent issues faced by other mechanisms.

We are therefore investigating a CMOS-compatible proton intercalation resistor that relies on a deterministic charge-controlled mechanism. The use of protons, the smallest cations, as the doping ion presents several advantages including high operation speed, good compatibility with current patterning processes, and long lifetime. Our initial design, shown in Figure 1, with a PdH_x solid hydrogen reservoir and a WO_3 active channel, demonstrated promising device characteristics but needs to be improved as : 1) it relied on Nafion, a non-CMOS-compatible electrolyte that strongly reacts with some other promising channel materials, and 2) the conductance of WO_3 and device energy consumption (conductance reading) increases through protonation. Herein, we present our progress towards device integrability using an inert CMOS-compatible electrolyte and on the reduction of the device energy consumption using a vanadium pentaoxide (V_2O_5) channel, which conductance decreases through protonation and can be modulated in a non-volatile, symmetric, reversible, and reproducible way, as shown in Figure 2.



▲Figure 1: Side-view schematic of the V2O5-based protonic programmable resistor.



▲Figure 2: Modulation characteristics of the V2O5-based protonic programmable resistor.

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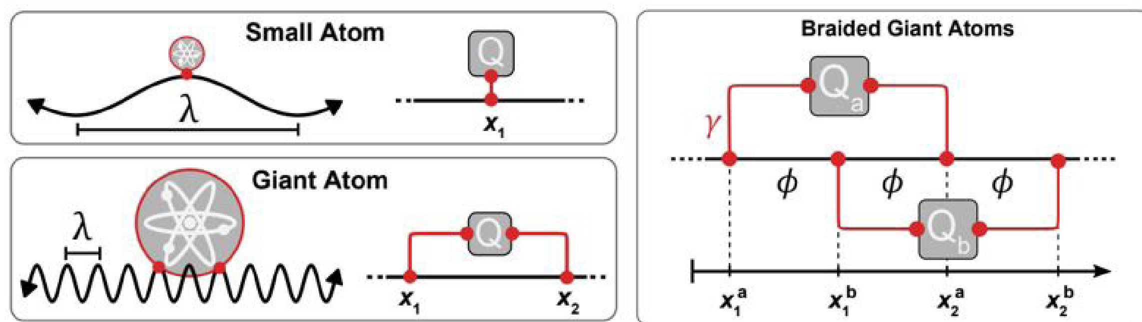
Waveguide Quantum Electrodynamics with Superconducting Artificial Giant Atoms

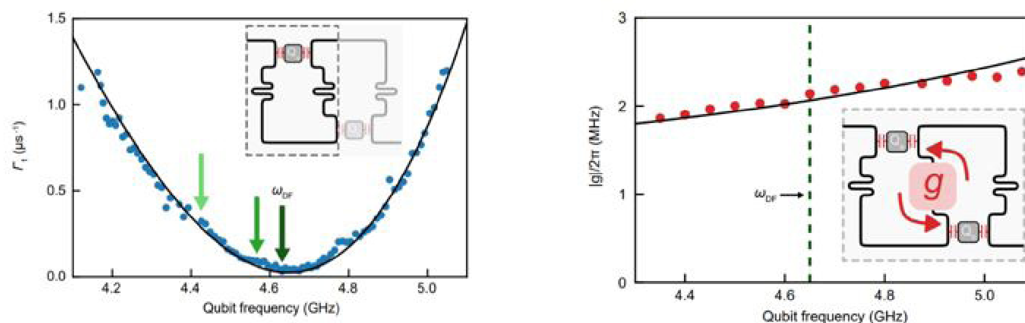
B. Kannan, M. Ruckriegel, D. L. Campbell, A. F. Kockum, J. Braumüller, D. K. Kim, M. Kjaergaard, P. Krantz, A. Melville, B. M. Niedzielski, A. Vepsäläinen, R. Winik, J. Yoder, F. Nori, T. P. Orlando, S. Gustavsson, W. D. Oliver
Sponsorship: DoE, Office of Science, Basic Energy Sciences, Materials Sciences and Engineering

Models of light-matter interactions typically invoke the dipole approximation, within which atoms are treated as point-like objects when compared to the wavelength of the electromagnetic modes that they interact with. However, when the ratio between the size of the atom and the mode wavelength is increased, the dipole approximation no longer holds, and the atom is referred to as a "giant atom." Thus far, experimental studies with solid-state devices in the giant-atom regime have been limited to superconducting qubits that couple to short-wavelength surface acoustic waves, probing the properties of the atom at only a single frequency.

Figure 1 shows an alternative architecture that realizes a giant atom by coupling small atoms to a waveguide at multiple, but well separated, discrete locations. We also show how multiple giant atoms can be coupled to the same waveguide in a braided fashion to enable interactions between the qubits that are mediated by the waveguide. Figure 2 shows how our realization of giant atoms enables tunable atom-waveguide couplings with large on-off ratios and a coupling spectrum that can be engineered by device design. We also demonstrate decoherence-free interactions between multiple giant atoms that are mediated by the quasi-continuous spectrum of modes in the waveguide-- an effect that is not possible to achieve with small atoms. These features allow qubits in this architecture to switch between protected and emissive configurations in situ while retaining qubit-qubit interactions, opening new possibilities for high-fidelity quantum simulations and non-classical itinerant photon generation.



▲ Figure 1: Schematic representation of small and giant atoms that are discretely coupled to a waveguide.



▲ Figure 2: Tunable atom-waveguide couplings (left) and waveguide-mediated interactions (right).

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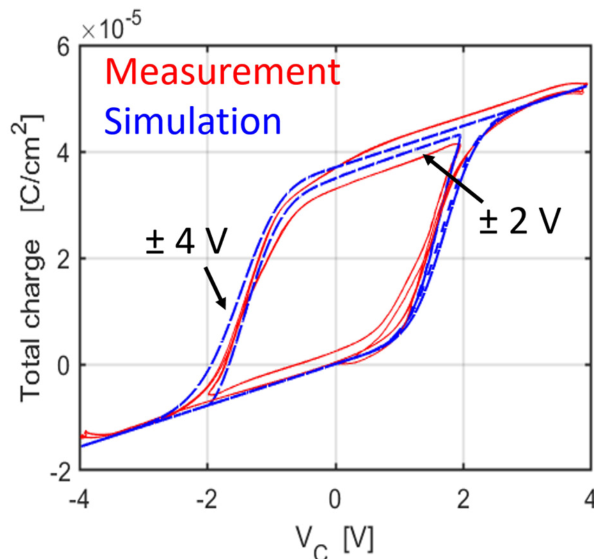
Dynamics of $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Structures: Experiments and Models

T. Kim, D. A. Antoniadis, J. A. del Alamo
Sponsorship: Semiconductor Research Corporation, Samsung Electronics

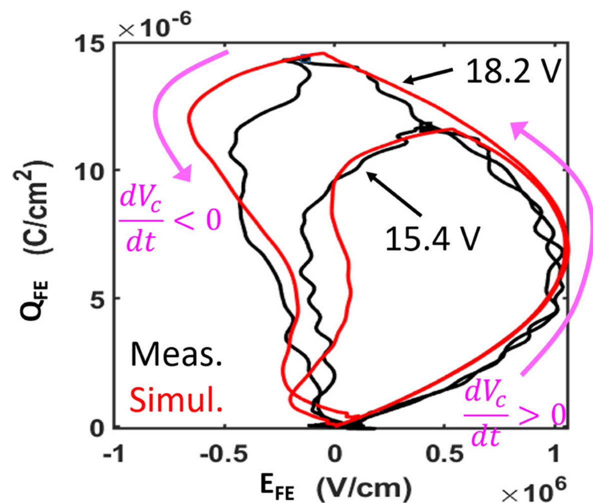
Due to its complementary metal-oxide-semiconductor compatibility, ferroelectric $HfZrO_2$ (FE-HZO) has attracted enormous interest in various semiconductor device areas, such as analog computing, logic, and memory. Despite intense research, controversy remains about the ferroelectric switching dynamics and the existence of negative capacitance (NC). To develop fundamental understanding, we have carried out detailed experimental studies of the FE-HZO switching dynamics of metal-ferroelectric-metal (MFM) and metal-ferroelectric-insulator-metal (MFIM) structures.

To extract the intrinsic dynamic response of the structures, our experimental methodology has paid close attention to minimizing and calibrating all circuit and sample parasitics. Based on the measured MFM dynamics, we have proposed a new nucleation-limited switching (NLS) model that captures the incubation and growth of polarization domain nuclei within each grain of a polycrystalline ferroelectric film, as described by a Weibull distribution. Figure 1 shows that the model describes well all observed behavior including major and minor charge-voltage loops under a broad range of conditions. Further, our work reveals that in R-MFM circuit configurations with an external resistor, the MFM dynamics show no evidence of NC-like behavior in contrast with other reports. Our study suggests that erroneous consideration of parasitic capacitance could explain earlier claims of NC effects in the MFM dynamics.

We observed clear NC behavior in MFIM structures. We confirm the transient quasi-static S-like FE behavior described in the literature and observe a dynamic response that displays hysteretic behavior in the NC region. A model based on the Landau-Khalatnikov equation that incorporates FE dynamics via a phenomenological frictional resistance adequately describes the observed results when that resistance is made dependent on the direction of the voltage drive vs. time, as in Figure 2. Mitigation of this hysteretic NC behavior will be crucial to harness NC in practical metal-oxide-semiconductor field-effect transistors.



▲Figure 1: Extracted major and minor QFE vs. VC loops from trapezoidal bipolar pulse measurement (red) and simulation (blue) for 400-µm2 MFM capacitor.



▲Figure 2: Dynamic response of FE-HZO in MFIM structure. Extracted QFE vs. EFE from 15.4-V and 18.2-V unipolar pulses measurement (black) and simulation (red) for 2500 µm2 capacitor. Purple lines show direction of voltage drive vs. time.

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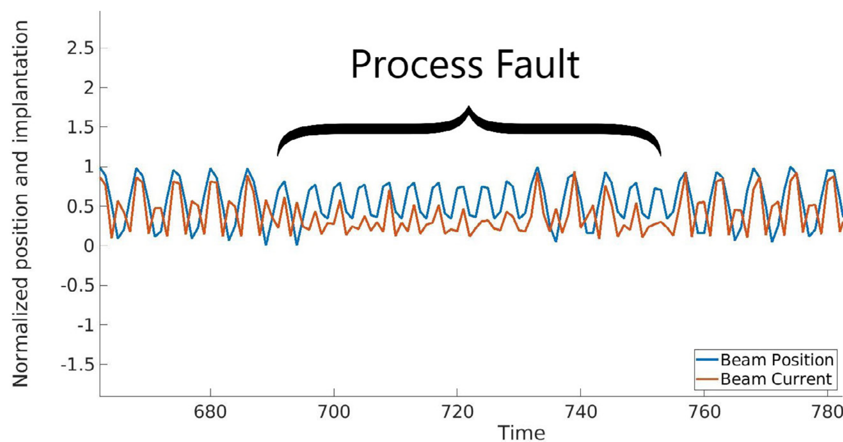
Fault Detection for Semiconductor Processes Using One-Class Parzen Window Classifiers

C. Lang, D. S. Boning
Sponsorship: Analog Devices, Inc.

Faults in fabrication processes are extremely costly. When undetected and unaddressed, they will continue to ruin wafer lots until the underlying problem is corrected, leading to massive yield losses. Our work uses one-class Parzen window classifiers to raise alerts when faults are suspected by monitoring process sensor information, reducing future yield loss. These models are kernel-based density estimation methods that determine the similarity of incoming data to known good process data. The method uses only nominal process data, which is desirable as faults are often unique, and examples will not be available before they occur. Using historical examples of a wide variety of faults in plasma etching and ion implantation (Figure 1), our fault- detection methodology captures more than 90% of faults, with a false positive rate of less than 0.5%. This method can be applied to a wide variety of processes without significant adjustment, making it ideal for generalized fault detection.



▲ Figure 1: Example fault in the ion implantation process causing yield losses. Within the faulty segment, beam current is lower than expected and does not follow the nominal pattern seen outside this range.

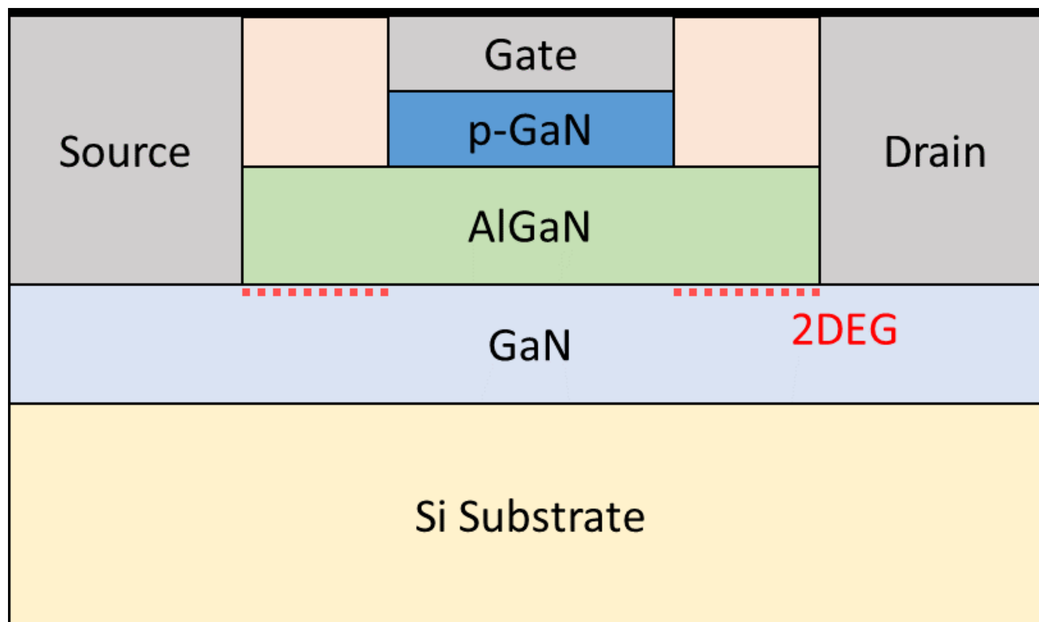
Bias Temperature Instability under Forward Bias Stress of Normally-Off GaN High-Electron-Mobility Transistors

E. S. Lee, J. A. del Alamo
Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining much attention as a necessary path to meet the growing demand for electrical energy and sustainability. GaN field-effect transistors (FETs) show great promise as high-voltage power switches due to their ability to withstand a large voltage and carry high current. For best circuit reliability, safety, and performance, a normally-off transistor is highly desirable. An attractive design is the p-doped GaN-gate high-electron-mobility transistor (p-GaN HEMT).

Our research aims to better understand the reliability issues impeding widespread adoption of p-GaN power HEMTs. One key issue is device degradation under prolonged operation, where key device performance metrics such as threshold voltage and gate leakage current change with electrical stress.

We show that device degradation under forward-bias electrical stress, i.e., when the transistor is turned on, shows multiple regimes that are voltage and time dependent. Due to the complex gate stack that includes a p-doped GaN layer, the device exhibits bias temperature instability degradation with signature characteristics of electron and hole trapping. Furthermore, we show that some of the degradation is recoverable. Altogether, our research reveals the presence of rich and dynamic degradation physics for the p-GaN HEMTs that must be well understood before the commercial success of this technology.



▲Figure 1: Simplified cross section of the p-GaN gate HEMT. AlGaN /GaN interface naturally induces a 2-dimensional electron gas (2DEG) that allows for conduction. However, the addition of the p-GaN layer leads to a natural depletion of the 2DEG and enhancement-mode operation.

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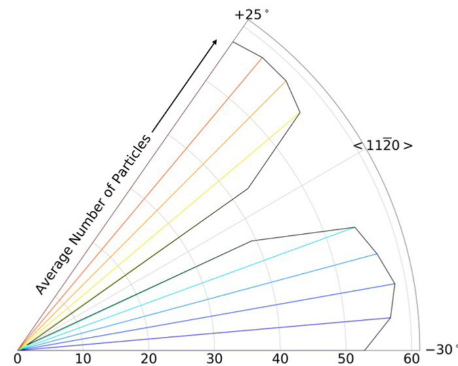
Morphological Stability of Nanometer-Scale Single-Crystal Metallic Interconnects

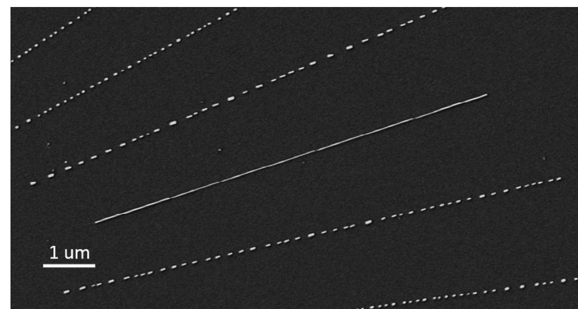
M. A. L'Etoile, Y. A. Shin, B. Wang, Q. Cumston, A. Warren, K. Barmak, K. R. Coffey, C. V. Thompson
Sponsorship: SRC, NSF

Continued integrated-circuit scaling requires interconnects with cross-sectional dimensions in the <10-nm range. At these dimensions, the resistance of interconnects increases dramatically due to surface and grain boundary electron scattering. The reliability of interconnects with nanoscale dimensions is also expected to be compromised by reduced morphological stability. As a part of a collaborative program focused on ballistic conduction and stability of single-crystal nanometer-scale interconnects, we are investigating the crystallographic dependence of the morphological stability of Ru wires.

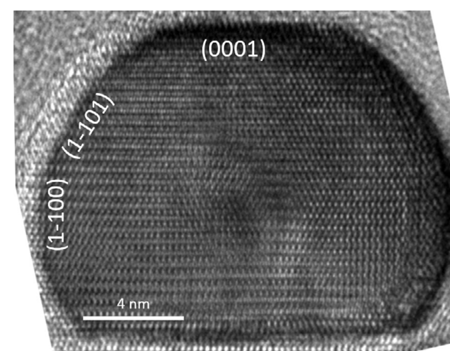
Thin single-crystal films agglomerate into small particles via capillary-driven surface diffusion in a process known as solid-state "dewetting." With decreasing film thickness, the temperature at which dewetting occurs is well below the constituent material's melting temperature. However, previous work on single-crystal Ni films has demonstrated that crystalline anisotropy gives rise to special crystallographic orientations along which single-crystal wires exhibit greatly enhanced morphological stability. Ru is a candidate material for future interconnects, and we have studied the morphological stability of arrays of Ru nanowires lithographically patterned from single-crystal (0001) films, such that the individual wires have axes lying in different crystallographic directions. After annealing, we find nanowires oriented along directions that are particularly stable; see Figures 1 and 2. Interconnects composed of such wires should have decreased vulnerability to morphological instabilities during processing and circuit operation. These wires also have strongly faceted surfaces, with facets parallel to the wire axis (Figure 3), which are predicted to reduce electron scattering and decrease interconnect resistance. This high degree of morphological stability and faceting also suggests that wires with these orientations will be particularly resistant to electromigration. Combining new data from this material system with results from past work on Ni, which has weaker surface energy anisotropy, will provide insights that will enable optimization of interconnect structural and crystallographic factors for design of morphologically stable nanowires with cross-sectional dimensions significantly below 10 nm.



▲ Figure 1: A stable, unbroken wire, surrounded by its 5°-offset neighbors, which have decomposed to form particles after annealing at 915 °C for 3 hours. Wires oriented along directions remained intact.



▲ Figure 2: Most nanowires broke into many particles after annealing.



▲ Figure 3: Cross-sectional TEM image of a stable wire confirms that stable wires are strongly faceted.

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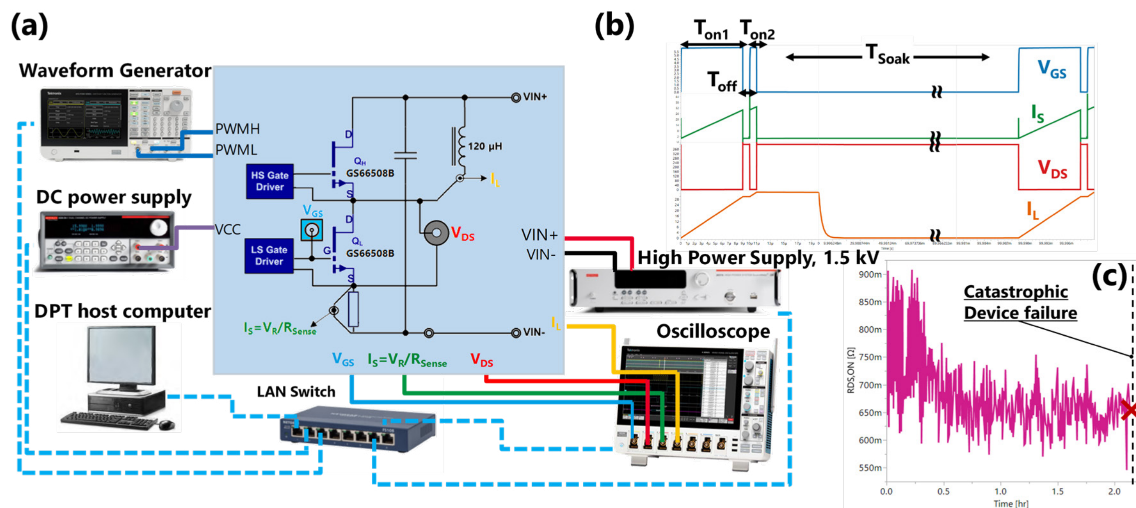
Switching Reliability of GaN Power High-Electron-Mobility Transistors

A. Massuda, J. A. del Alamo
Sponsorship: Analog Devices, Inc.

GaN electronics constitutes a new technology with superior power-handling capabilities compared to those of Si and other semiconductors in many applications. Power management applications typically involve operating the GaN transistors under rapid switching conditions between a high-voltage off-state and a high-current on-state. Depending on the system topology and specifications, two switching modes apply to power applications: soft switching and hard switching. The reliability and robustness of GaN transistors under repeated switching is a concern, particularly when they operate under hard-switching conditions.

The Double-Pulse Test is the most effective test for emulating high-power switching close to the mode of operation of the devices in electrical power management applications. In our work we have constructed a unique experimental setup to implement the Double-Pulse Testing technique. Figure 1a illustrates a physical implementation of the experimental setup. The system can conduct testing under severe stress conditions and monitor the induced degradation of device parameters up to the point of catastrophic device failure. Figure 1b shows a typical waveform of the Double-Pulse Test. The system allows users to repeat the test multiple times and measure device parameters at fixed intervals. Figure 1c shows an example of catastrophic degradation of dynamic $R_{DS,ON}$ when the transistor is subjected to hours of repeated switching operation. Degradation and hard-fail data will be used to verify failure modes and develop life-time models in order to project device survivability under various conditions.



▲ Figure 1: (a) Schematic diagram of experimental setup for switching reliability of GaN transistors; (b) typical waveform of Double-Pulse Test; (c) $R_{DS,ON}$ degradation vs. time for multiple Double-Pulse Tests.

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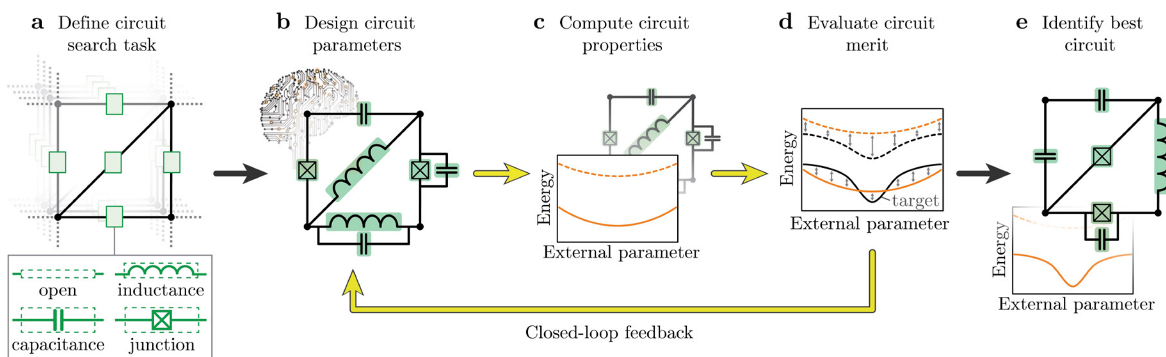
Automated Design of Superconducting Circuits and Its Application to 4-Local Couplers

T. Menke, F. Häse, S. Gustavsson, A. J. Kerman, W. D. Oliver, A. Aspuru-Guzik
Sponsorship: ODNI, IARPA, ARO, DoD via MIT Lincoln Laboratory

Quantum processors are well-controlled quantum systems capable of performing complex computational tasks. They have been shown to hold promise for the simulation of fundamental physical effects, as well as for solving computationally expensive yet practical problems. Superconducting circuits have emerged as a promising platform to build such quantum processors. These are microscale electrical circuit structures that are fabricated on an on-chip device. In a cryogenic environment, the chip behaves quantum mechanically and can be controlled using microwave pulses.

The challenge of designing a circuit is to compromise between realizing a set of performance metrics and reducing circuit complexity and noise sensitivity. At the same time, one needs to explore a large design space, and computational approaches often yield long simulation times. Here, we automate the circuit design task using **s**uperconducting **ci**rcuit c**l**osed-**l**oop **a**utomated design (SCILLA). The software SCILLA performs a parallelized, closed-loop optimization to design superconducting circuit diagrams that match predefined properties, such as spectral features and noise sensitivities. We employ SCILLA to design 4-local couplers for superconducting flux qubits and identify a circuit that outperforms an existing proposal with a similar circuit structure in terms of coupling strength and noise resilience for experimentally accessible parameters. Our results are important for the future development of quantum processors in two ways. First, the coupler circuit that we have found is expected to boost the capabilities of quantum processors. Second, our method demonstrates how automated design can facilitate the development of complex circuit architectures for quantum information processing.



▲Figure 1: Implementation of SCILLA, enabling automated circuit design. (a) Definition of the circuit design task, with details about general circuit architecture, parameter bounds, and design targets. (b) Based on the general architecture, the design module evokes parameter-generating algorithms to place components and choose component parameters in the circuit. (c) Calculation of circuit properties such as spectra or noise sensitivity. (d) Estimation of the agreement between computed properties and target properties. (e) Circuits close to the design target are identified. A database system facilitates asynchronous execution and parallelization of the workflow and refinement of design choices (closed-loop feedback) based on merit evaluations of previously proposed circuits.

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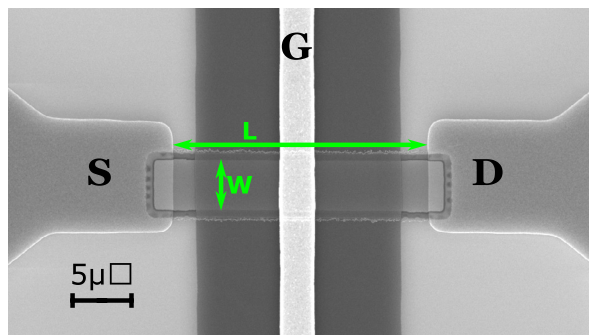
CMOS-Compatible Protonic Programmable Resistor Based on Phosphosilicate Glass Electrolyte for Analog Deep Learning

M. Onen, N. Emond, B. Yildiz, J. Li, J. A. del Alamo
Sponsorship: MIT-IBM Watson AI Lab

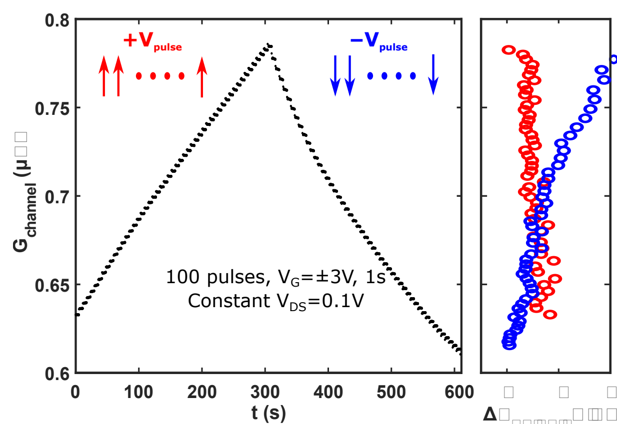
The success of deep learning in classifying and clustering representations of data at multiple levels of abstraction has fundamentally changed how information is processed. However, conventional digital architectures face increasing difficulties in supporting the heavy computational workloads required to train state-of-the-art deep neural networks. The pressing need for faster and more energy-efficient deep learning processors has therefore led to an intensive investigation of in-memory computation schemes using analog crossbar arrays.

The building block of analog crossbar arrays is the crosspoint element, which can be described as a programmable, non-volatile resistor. Ion intercalation-based programmable resistors have emerged as a potential next-generation technology for analog deep learning applications. Protons, being the smallest ions, are the most promising candidate to enable devices with high modulation speed, low energy consumption, and enhanced endurance. The main bottleneck with developing protonic programmable resistors has been the absence of a suitable solid-state electrolyte that conducts protons but blocks electrons. All designs so far have relied on approaches that either cannot be integrated and scaled down, such as using organic materials; use chemically and thermally sensitive polymers; or suffer from energy inefficiency such as high electric field-induced water hydrolysis.

In this work, we report on the first back-end complementary metal-oxide-semiconductor-(CMOS) compatible protonic programmable resistor enabled by the integration of phosphosilicate glass (PSG) as the proton electrolyte layer. PSG is an outstanding electrolyte material that displays both excellent protonic conduction and electronic insulation characteristics. Moreover, it is a well-known material within conventional Si fabrication that enables high deposition control and scalability. Our scaled three-terminal devices show desirable modulation characteristics in terms of symmetry, retention, endurance, and energy efficiency. Protonic programmable resistors based on PSG, therefore, represent promising candidates to realize nanoscale analog crossbar processors with monolithic CMOS-integration.



▲Figure 1: Top view scanning electron microscope image of a protonic programmable device.



▲Figure 2: Basic modulation characteristics of protonic programmable resistor.

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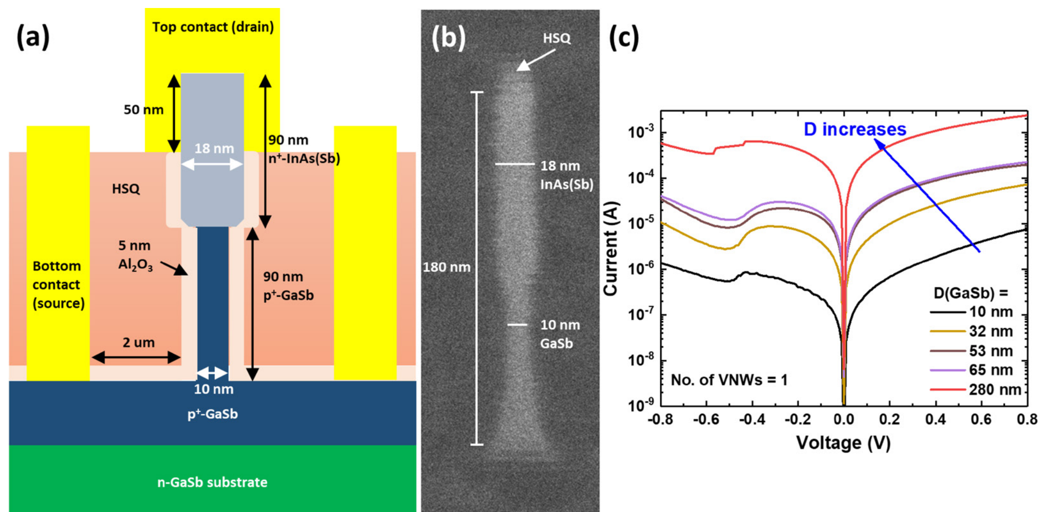
III-V Broken-Band Vertical Nanowire Esaki Diodes

Y. Shao, J. A. del Alamo
Sponsorship: Intel

Further reducing transistor power consumption of metal-oxide-semiconductor field-effect transistors (MOSFETs) in logic applications requires transport mechanisms other than thermionic emission over an energy barrier. Among all possible mechanisms, quantum tunneling emerges as one of the most promising. Therefore, the design and demonstration of tunnel field-effect transistors (TFETs) have received much attention recently. In spite of intense research, the results to date have been disappointing.

In our research, we aim to utilize the unique broken-band alignment and the superior carrier transport properties in the GaSb/InAs material system to obtain high drive current with tunneling. In order to quantitatively evaluate the quality of the tunneling junction, GaSb/InAs(Sb) vertical nanowire (VNW) Esaki diodes have been fabricated and electrically characterized.



▲ Figure 1: (a) Cross-sectional schematics of a VNW Esaki diode. (b) SEM image of a fabricated 10-nm-diameter VNW. (c) Electrical characteristics of VNW Esaki diodes with different diameters.

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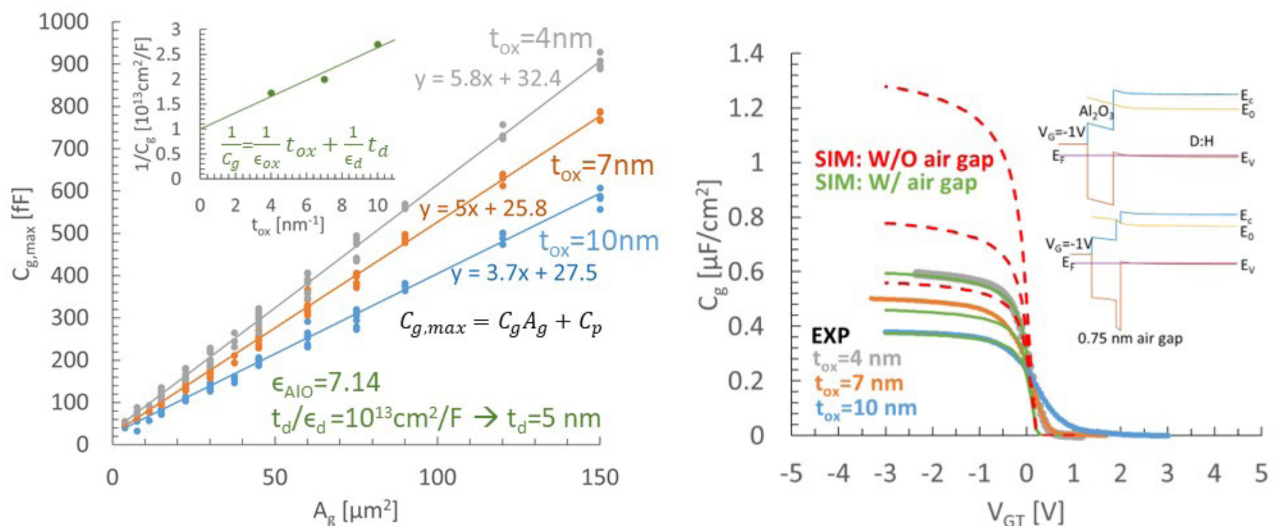
Mysterious Layer on a Hydrogen-Terminated Diamond Surface

A. Vardi, M. Tordjman, R. Kalish, J. A. del Alamo
Sponsorship: U.S Israel Binational Science Foundation, Bose, DARPA

The surface conductivity of H-terminated diamond (D:H) is usually explained by the transfer doping model. The model assumes a surface dopant layer is formed on the D:H surface that generates a two-dimensional hole gas (2DHG) in the diamond. The dopant layer is typically assumed to be of atomic dimensions. However, since the D:H surface is almost perfectly passivated, there are no chemical bonds out of the surface, and the dopants are weakly held by van der Waals forces. Consequently, analysis of the capacitance of MOSFETs built on D:H show it to be much smaller than expected. To study the nature of this interfacial layer, we have analyzed the scaling properties of the gate capacitance of Al/Al_2O_3/D:H MOS structures. A comparison of the obtained results against Poisson-Schrodinger simulations suggests the existence of an "air gap" of 0.5-1 nm in thickness at the Al_2O_3/D:H interface. If confirmed, this gap will have important implications for the current drivability of diamond MOSFETs.



▲ Figure 1: (Left) Scaling of gate capacitance with gate area for MOS capacitors with different Al2O3 thickness. From the slope of the lines, the intrinsic gate capacitance per unit area, Cg, is extracted. Inset: 1/Cg vs. Al2O3 thickness. From the slope, the Al2O3 dielectric constant is extracted (7.1); the intercept is the semiconductor density of states capacitance found to be unrealistically small. Comparison (right) of experimental CV data and P-S simulations with a 0.75-nm "air gap" provides a good explanation for our findings.

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Impact of Ionizing Radiation on Superconducting Qubit Coherence

A. Vepsäläinen, A. Karamlou, J. Orrell, A. Dogra, B. Loer, F. Vasconcelos, D. Kim, A. Melville, B. Niedzielski, J. Yoder, S. Gustavsson, J. Formaggio, B. VanDevender, W. D. Oliver
Sponsorship: LPS, ARO

The practical viability of technologies that rely on qubits requires long coherence times and high-fidelity operations. Superconducting qubits are a promising platform for achieving these objectives. However, their coherence is affected by broken Cooper pairs, referred to as quasiparticles. The experimentally observed density of quasi-particles is orders of magnitude higher than the value predicted at equilibrium by the Bardeen-Cooper-Schrieffer theory of superconductivity. Our results suggest that ionizing radiation from cosmic rays and from environmental radioactive materials contribute to the observed difference.

In this work, we use a radioactive 64Cu source to measure the impact of ionizing radiation on superconducting qubits under controlled levels of radiation. While the activity of the source decayed over time, we observed an increase in the coherence of the qubits, see Figure 1. From independently measured level of naturally occurring background radiation, we can extrapolate the impact of ionizing radiation on quasi-particle generation and the qubit coherence. We predict that the ionizing radiation would limit the coherence times of superconducting qubits of the type we measured to the millisecond regime.

Next, we demonstrate that shielding the qubits with lead can mitigate the impact of radiation on the qubits, see Figure 2. We continuously raised and lowered the shield and measured the corresponding change in the qubit energy-relaxation rate. Albeit a small effect in today's qubits, the change in the relaxation time positively correlated with the increased shielding, confirming our hypothesis that naturally occurring ionizing radiation affects the qubit coherence.

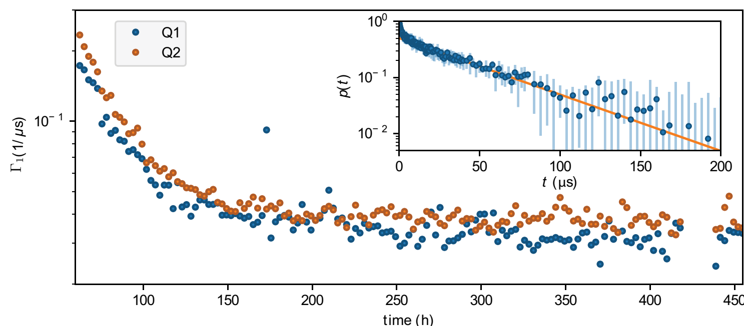
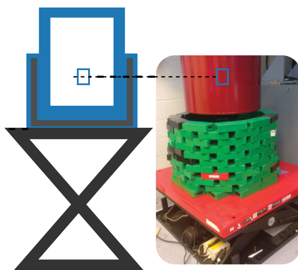
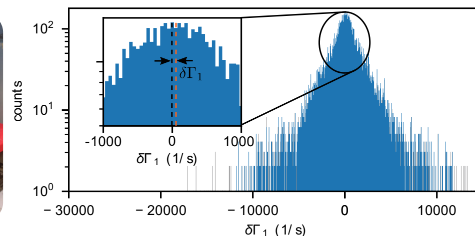


Figure 1: Energy-relaxation rate (Γ1) of the qubits as a function of time from the installation of the radioactive source. The inset shows an example of the measurement used to extract the energy-relaxation rate.

Figure 2: The lead shield used to mitigate the impact of ionizing radiation (left). The histogram of the measured differences in the energy relaxation rates of the qubits when the shield was in up or down positions (right).





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NbN-Gated GaN Transistor Technology for Applications in Quantum Computing Systems

Q. Xie, N. Chowdhury, A. Zubair, M. Sánchez Lozano, J. Lemettinen, M. Colangelo, O. Medeiros, I. Charaev, K. K. Berggren, T. Palacios
Sponsorship: IBM

High-performance and scalable cryogenic electronics is an essential component of future quantum information systems, which typically operate below 4K. Superconducting qubits need advanced radio-frequency (RF) and pulse-shaping electronics, which typically occupies large instrumentation racks operating at room temperature. This approach is not scalable to the millions of qubits needed in future quantum systems.

This work explores the use of wide band gap heterostructure electronics, specifically the AlGaN/GaN high electron mobility transistor (HEMT), for cryogenic low-noise applications. These structures take advantage of the polarization-induced two-dimensional electron gas to create a high mobility channel, hence eliminating the heavy doping needed in the other semiconductor technologies. Epitaxially-grown GaN-on-Silicon wafers have been demonstrated in large (12 inch / 300 mm) substrates, therefore making the technology an excellent candidate for scalable RF electronics in quantum computing systems.

Furthermore, the use of electrodes of superconducting materials is proposed to significantly reduce the parasitic components and therefore push the RF performance of cryogenic devices. Short-channel transistors with NbN gates of length 250 nm have been demonstrated with promising performance.

The next step will study the effect of the superconducting gate on RF characteristics of the transistors, with the eventual goal of pushing the frequency performance of these transistors to new limits. These transistors will be integrated into low-noise amplifier circuits for applications in readout and control electronics at cryogenic temperature. Furthermore, the demonstrated NbN-gated GaN transistor paves the way for the application of high-frequency GaN technology in cryogenic electronics, notably in scalable quantum computing systems. When combined with other highlights in GaN electronics, e.g., a GaN complementary metal-oxide-semiconductor (CMOS) platform, the reported technology brings us one step closer to an all-nitride integrated electronics-quantum device platform.

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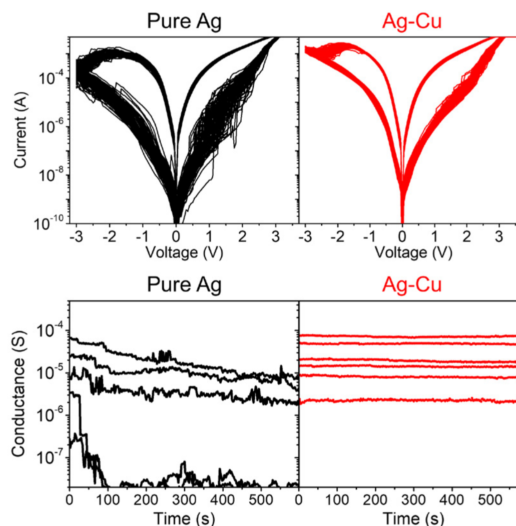
Metal Alloy Enables Reliable Silicon Memristor Synapses

H. Yeun, P. Lin, C. Choi, J. Kim
Sponsorship: Samsung Global Research Laboratory, MIT-IBM Watson AI Lab, NSF-SRC-E2CDA

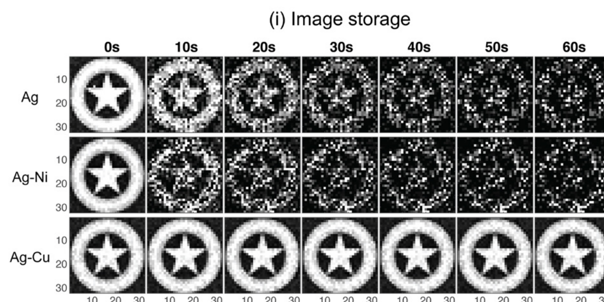
In the age of artificial intelligence (AI), memristors have emerged as an artificial synapse for neuromorphic computing, overcoming the limitations of conventional silicon (Si)-based digital synapses. Interestingly, Si has also been utilized to develop memristor synapses via combination with a silver (Ag) electrode. An electrical conductance of Si medium is reversibly modulated by Ag injection, corresponding to the synaptic weight changes. Owing to the thermodynamic instability of Ag in Si medium (Ag is immiscible in Si), injected Ag exhibits high mobility, resulting in a high-weight modulation ratio and high switching endurance. Unfortunately, large switching variations and poor weight stability occur at the devices and are also induced by the thermodynamic instability. Thus, to mitigate such dilemmas in performance, the regulation of thermodynamic stability of Ag in Si medium would be the fundamental strategy.

Here we have developed Ag alloy for precision tuning of thermodynamic interactions of Ag and Si, thereby achieving highly balanced synaptic performance. We selected copper (Cu) as an alloying element due to its (1) high diffusivity into Si and (2) favorable thermodynamic interactions with both Ag and Si. Our hypothesis was that Cu would migrate into Si simultaneously with Ag and enhance thermodynamic stability of Ag in Si (i.e., be a stabilizer). The device's performance results clearly confirm our metallurgical strategy that switching uniformity and weight retention are significantly enhanced by a Ag-Cu alloyed electrode (Figure 1). It should be noted that other alloying elements such as Ni cannot improve the synaptic performance due to their repulsive interactions with Ag.

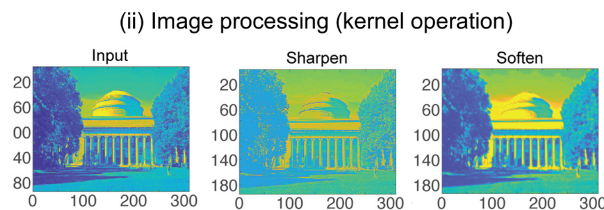
With promising device performance test results, we have demonstrated 32 × 32 Si memristor array and successfully performed image storage (Figure 2) and image processing (Figure 3), which are only enabled by Ag-Cu active electrode (Figure 3). We believe our alloying strategy can be expanded to other memristive synapses to resolve performance issues in neuromorphic computing applications.



▲ Figure 1: Switching performance of Si memristors. Switching uniformity during 100 cycles (top) and weight retention properties with multi-conductance levels (bottom).



▲ Figure 2: Image storage in 32 × 32 silicon memristor array with respect to active electrodes: Ag, Ag-Cu, and Ag-Ni.



▲ Figure 3: Image processing (convolutional kernel processing) in Si memristor array with Ag-Cu alloy.

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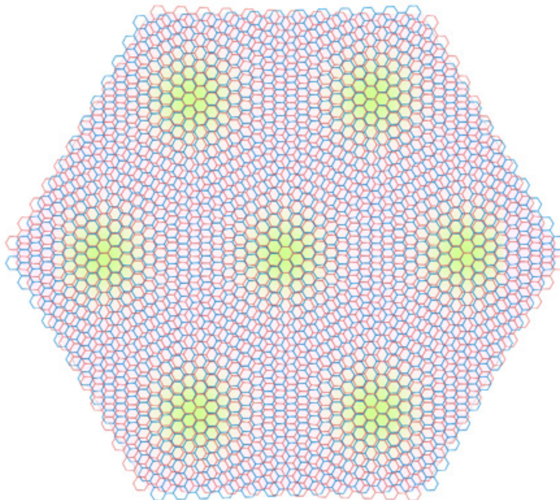
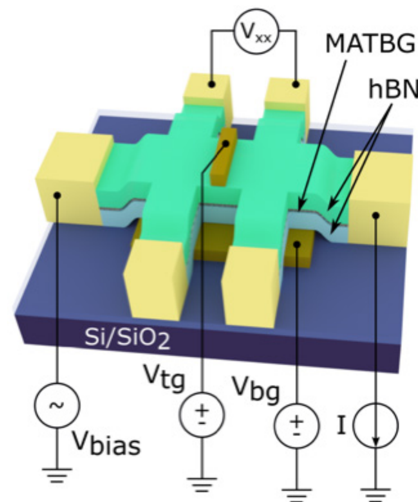
Highly Tunable Junctions in Magic Angle Twisted Bilayer Graphene Tunneling Devices

D. Rodan-Legrain, Y. Cao, J. M. Park, S. C. de la Barrera, M. T. Randeria, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero
Sponsorship: NSF, CIQM, DOE, BES, US Army Research Office, Fundación Bancaria 'la Caixa', Gordon and Betty Moore Foundation, Fundación Ramón Areces, MEXT.

The recent observation of superconductivity and correlated insulating states in "magic-angle" twisted bilayer graphene (MATBG) featuring nearly flat bands at twist angles close to 1.1 degrees presents a highly tunable two-dimensional material platform capable of behaving as a metal, an insulator, or a superconductor. Local electrostatic control over these phases may enable the creation of versatile quantum devices that were previously not achievable in other single material platforms. Our research shows how we can exploit the electrical tunability of MATBG to engineer Josephson junctions and tunneling transistors all within one material, defined solely by electrostatic gates. Our multi-gated device geometry offers complete control over the Josephson junction, with the ability to independently tune the weak link, barriers, and tunneling electrodes. Utilizing the intrinsic bandgaps of MATBG, we also demonstrate monolithic edge tunneling spectroscopy within the same MATBG devices and measure the energy spectrum of MATBG in the superconducting phase. Furthermore, inducing a double barrier geometry permits the devices to be operated as a single-electron transistor, exhibiting a Coulomb blockade. These MATBG tunneling devices, with versatile functionality encompassed within a single material, may find applications in graphene-based tunable superconducting qubits, on-chip superconducting circuits, and electromagnetic sensing in next-generation quantum nanoelectroni



▲Figure 1: Illustration of the moiré pattern in twisted bilayer graphene near the magic angle.



▲Figure 2: Schematic illustration of the device structure.

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Electronic Cells: Autonomous Micromachines from 2D Materials

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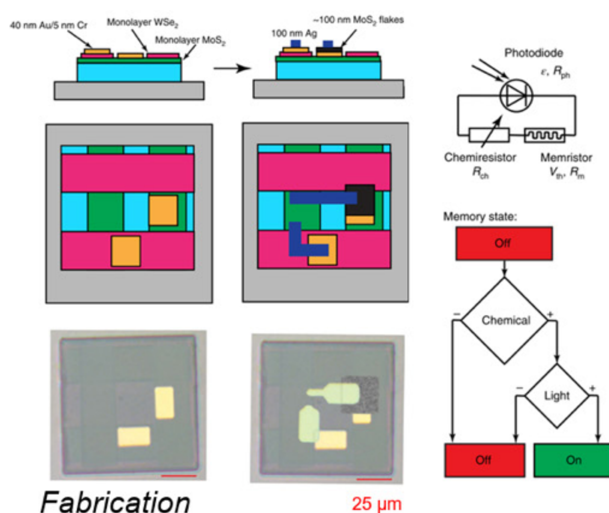
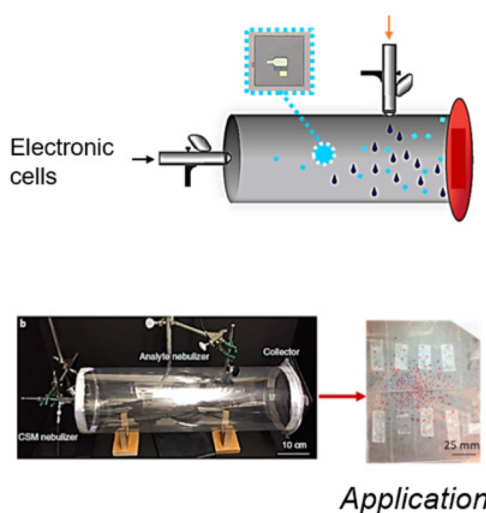
Sponsorship: 2015 US Office of Naval Research Multi University Research Initiative (MURI) grant on Foldable and Adaptive Two-Dimensional Electronics (FATE) at MIT, Harvard and University of Southern California

Electronic cells are micromachines encompassing autonomous on-board functions such as sensing, computation, communication, locomotion, and power management. Akin to their biological counterparts, electronic cells bring specialized capabilities to previously inaccessible locations. Here, we present the design and fabrication of the first-of-its-kind electronic cell composed of the nanoelectronic circuit on top of an SU-8 particle. Powered by a 2D material-based photodiode, the on-board circuit connects a chemiresistor element and a memristor element, enabling on-board detection and storage capabilities. We demonstrate how our cells sense and record information about the presence of ammonia and dispersed soot when aerosolized in the enclosed tubes, dispersed in a hydrodynamic flow of pipelines, or sprayed over large surfaces. Electronic cells may find widespread application as probes in confined environments, such as the human digestive tract, oil and gas conduits, chemical and biosynthetic reactors, and autonomous environmental sensors.



▲ Figure 1: (left) Summary of electronic cell fabrication steps as well as its electrical circuit diagram.



▲ Figure 2: (right) Aerosolizable electronics as an application of electronic cells. Schematic and its experimental implementation.

FURTHER READING

- V. B. Koman, P. Liu, D. Kozawa, A. T. Liu, A. L. Cottrill, Y. Son, J. A. Lebron, M. S. Strano, "Colloidal Nanoelectronic State Machines Based on 2D Materials for Aerosolizable Electronics", *Nature Nanotechnology*, vol. 13, pp. 9:819-827, Sep. 2018.

Decoding Complexities in Relaxor Ferroelectrics Using Electron Microscopy

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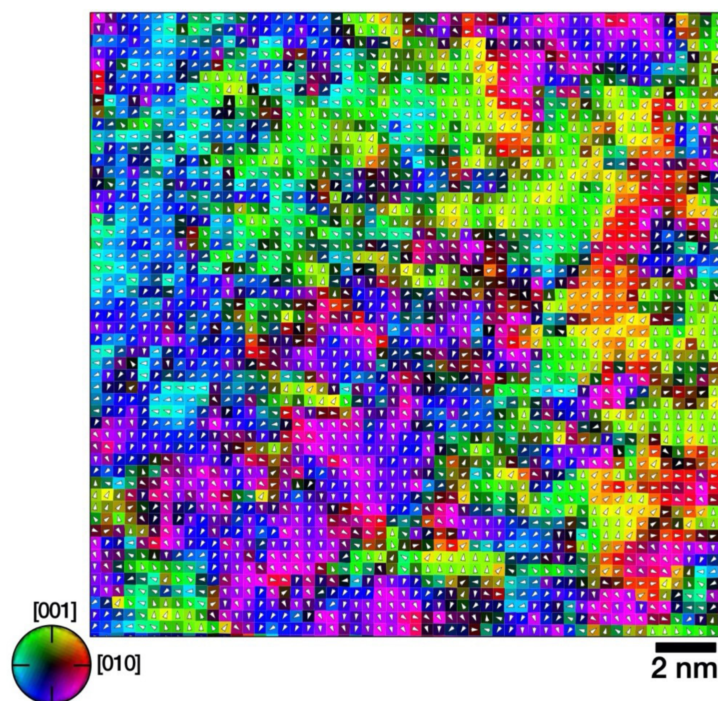
Sponsorship: Center of Dielectrics and Piezoelectrics (CDP) and Collaborative Hierarchical and Agile Responsive Materials (CHARM)

Relaxor ferroelectrics show slim hysteresis loops, low remanent polarization, high saturation polarization, and exceptional electromechanical coupling, finding applications in ultrasound imaging and energy storage devices. Developing a structure-property relationship in relaxors has been a seemingly intractable problem due to the presence of nanoscale chemical and structural heterogeneities. We have employed aberration-corrected scanning transmission electron microscopy (STEM) to quantify the various contributions of nanoscale heterogeneity to relaxor ferroelectric properties in a PMN-PT system. Specifically, we found three main contributions-- chemical ordering, oxygen octahedral tilting and oxygen octahedral distortion--that are difficult to otherwise differentiate. STEM reveals the elusive connection between chemical and structural heterogeneity and local polarization variation. Further, the effects of strain and thickness on PMN-PT thin films has been examined. These measurements elucidate the design principles for next-generation relaxor material.



▲ Figure 1: Projected polarization map calculated in relaxor ferroelectric, PMN-PT thin film, showing nanoscale domain structure.

FURTHER READING

- A. Kumar, J. N. Baker, P. C. Bowes, M. J. Cabral, S. Zhang, E. C. Dickey, D. L. Irving, J. M. LeBeau, "Atomic-resolution Electron Microscopy of Nanoscale Local Structure in Lead-based Relaxor Ferroelectrics," *Nature Materials*, vol. 20, pp. 62–67, 2021.