Electronic, Magnetic, Superconducting, and Quantum Devices

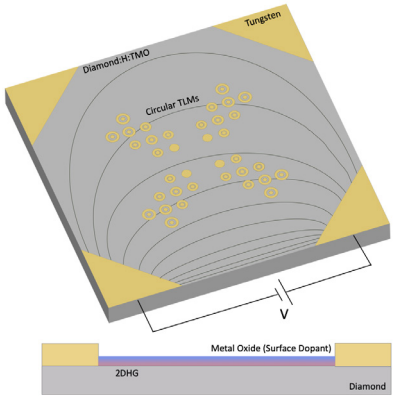
Engineering a 2D Hole Layer in Hydrogen-terminated Diamond Using Transition Metal Oxides

E. Al Johani, A. Vardi, J. A. del Alamo
Sponsorship: DARPA

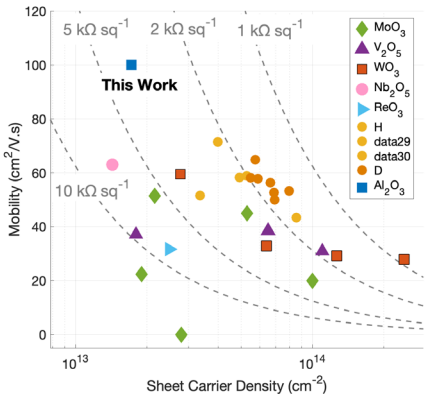
The quest for a suitable wide-bandgap semiconductor for high-power and high-frequency applications is well motivated; wide-bandgap semiconductors generally exhibit a high breakdown field and can therefore support a high voltage over short distances. Diamond (5.5 eV) in particular is an attractive prospect since its thermal conductivity and radiation hardness far surpass that of other wide-bandgap semiconductors. However, practical transistors require the ability for the charge density to be engineered through substitutional doping, which has proven to be difficult considering the strong covalent bonds that make up bulk diamond.

We use an alternative doping mechanism, surface transfer doping; it takes advantage of the unformed bonds at the diamond surface and generates a highly conductive 2D hole sheet at the surface with carrier densities up to 1014 cm-2. Surface transfer doping using stable high electron affinity transition-metal oxides (TMO) such as WO3 along and the novel contact-first process explored in this work shows great promise to advance process stability while maintaining the high current densities desired for future power diamond transistors.

We are exploring various methods to reproducibly achieve high values of sheet hole concentration and hole mobility on the diamond surface that can be incorporated into a transistor fabrication process. Our proposed design for characterizing mobility and surface conductivity combines a transmission line and Van der Pauw test structures simultaneously, as shown in Figure 1. We chose tungsten as the ohmic contact for its thermal stability and attractive process characteristics. We are examining different H-plasma processes for diamond surface bond passivation and the use of the hydrogen isotope deuterium. Preliminary results show increased carrier concentration and mobility with Al2O3 as the surface dopant, as in Figure 2. The methods explored in this work show promise towards the enhancement of diamond conductivity and reproducibility.



▲Figure 1: TMO on diamond mobility against carrier concentration with corresponding sheet resistance values and comparison to literature values using spontaneous surface doping.



▲Figure 2: Design of test structures for characterizing the 2D conductive hole layer using Van der Pauw and circular TLM structures. Tungsten is used for contacts.

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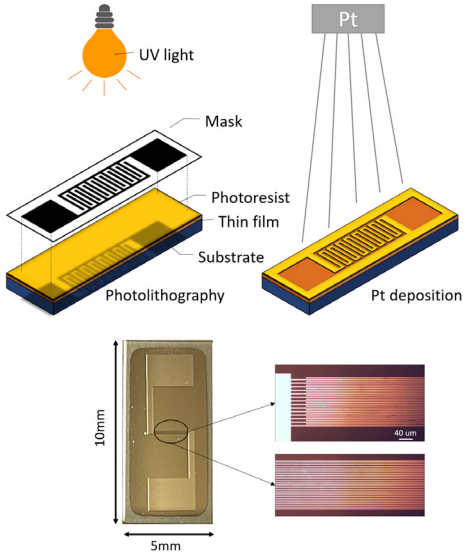
Dynamic Approach to Quantifying Strain Effects on Ionic and Electronic Defects in Functional Oxides

Y.-T. Chi, T. Defferriere, H. L. Tuller, B. Yildiz, K. Van Vliet
Sponsorship: DoE, Basic Energy Sciences

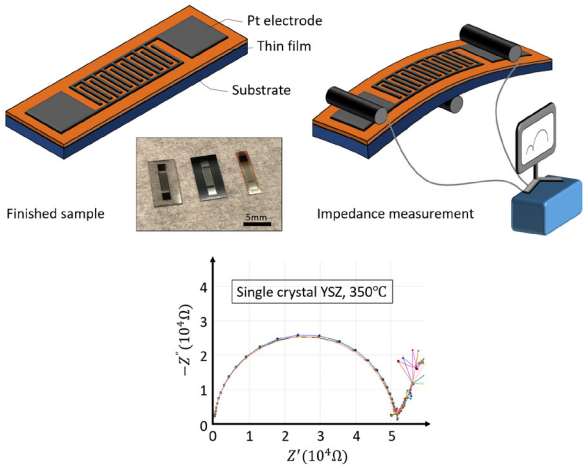
The search for novel electronic and magnetic properties in functional oxides has generated a growing interest in understanding the mobility and stability of ionic and electronic defects in these materials. Instead of altering material content, most research views mechanical strain as a lever for modulating defect concentration and mobility more finely and continuously in both semi-conductors and functional oxides. Previous studies also proposed that strain may increase ionic mobility by orders of magnitude, which is crucial for lowering the operation temperature of solid oxide fuel cells.

However, experimental and computational results from research groups differ significantly due to the convoluted effect of mechanical strain and film/substrate interface on defect content and mobility. Such reliance on substrate selection to induce strain in the oxide thin film also limits the range of strain accessibility, with limited data available to date

We have developed an experimental technique that facilitates application of in-plane strain to functional oxide thin films continuously on the same substrate. First, we combine photolithography and metal sputtering in MIT Nano to deposit an interdigitated Pt electrode down to a 2-micrometer finger distance on our sample (Figure 1). Next, we conduct 3- or 4-point bending and concurrent conductivity measurement of the thin film-on-substrate device (Figure 2). This approach is accessible to a wide temperature range and has precise gas control relevant to mixed ionic-electronic conducting oxides with extremely high reproducibility (error < 3%) over a long period of time. We can strain and measure the transport properties of the same functional oxide thin film at high temperature in situ, over a range of strains applied to a single system. Combining these experiments with our ab initio computational simulations and predictions of carrier dominance over a range of strains and temperatures, we also aim to measure the carrier mobility in Nb-doped SrTiO3 as a function of applied strain, to observe the sudden change of carrier mobility and temperature dependency. We believe this will also be a powerful technique for studying the strain effect on surface reactions like exsolution or catalytic reaction.



▲Figure 1: Photolithography for interdigitated electrode pattern on photoresist, followed by Pt deposition using sputtering. OM pictures of Pt interdigitated electrode on single crystal YSZ with 2-um finger distance.



▲Figure 2: Finished sample with interdigitated Pt electrode. Y2O3-doped zirconia, Nb-doped SrTiO3, and Pr-doped CeO2 (left to right). Schematic of impedance measurement with 3-point bending on sample. Impedance reproducibility showcase on single-crystal YSZ at 350C for 10 measurements over 5 hrs with < 3% error.

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First Demonstration of GaN CMOS Logic on Si Substrate Operating at 300 Degrees C

N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

The power density (and form-factor) of power electronic circuits is mostly dominated by the size of the passive energy storage components like inductors and capacitors, which depend on the switching frequency. Increasing the switching frequency of power electronic circuits can significantly reduce the energy storage requirement of these components to allow for smaller components. However, the maximum operating frequency of state-of-the-art GaN transistors, promising candidates for high-voltage compact switches, is usually limited by the gate inductance between the gate electrode and the driver circuit. Monolithically integrating the GaN-based driver circuit with that of the GaN power transistor on the same chip can significantly reduce this inductance.

To increase the efficiency of such GaN-based integrated circuits, a CMOS-like circuit technology is needed. Major benefits of such a technology include zero/negligible static power dissipation, higher noise immunity, and linearity. However, the lack of high-performance GaN p-FETs and the challenges of their monolithic integration with E-mode n-FET devices are major roadblocks towards achieving such a technology. This work demonstrates a new GaN-based complementary circuit platform on 6-inch Si substrate.

Figure 1(a) shows the voltage transfer characteristics (VTC) of the inverter for a VDD of 5 V along with output current. The inverter shows a record voltage gain of 27 V/V for a voltage switching of 0-to-5 V. Figure 1(b) shows the VTC of the same inverter for VDD=3 V, exhibiting excellent inverting behavior with Vswing=2.91 V and maximum gain of ~15 V/V. The dynamic switching of the inverter was characterized by connecting the inverter input to a pulse generator and the output to the high impedance port of an oscilloscope. The VDD was kept at 3 V because of the high gate leakage in the p-GaN gated n-FET above that voltage. The voltage of the input pulses varied from −0.2 V to 3 V with a ramp time of 100 ns. Figure 1(c)-(d) presents measured waveforms of the input and output signals. The output signal showed a voltage swing close to 0~3 V. The fall time was 1 µs; the rise time was 20 µs. It should be noted that these times represent an upper bound on the fall and rise times, as the very high input capacitance of the oscilloscope port (~ 350 pF) limits the measurements.

High-temperature measurement of the inverter shows a reduction in the voltage gain, as shown in Figure 2. The maximum available voltage swing at the output is also reduced due to the rise of low-level Vout, which can be attributed to the reduction in ON-OFF current ratio of the p-FET at high temperature. At high temperature, because of the higher activation of Mg dopants, the threshold voltage of p-FET moves towards the positive zone, making it D-mode, which in turn reduces the ON-OFF current ratio.

While room exists for significant performance improvement, this demonstration opens a number of application domains for GaN such as integrated CMOS driver circuits, CMOS logic, logic, and signal conditioning under harsh environment operation, among many others.

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100-nm Channel Length E-mode GaN p-FET on Si Substrate

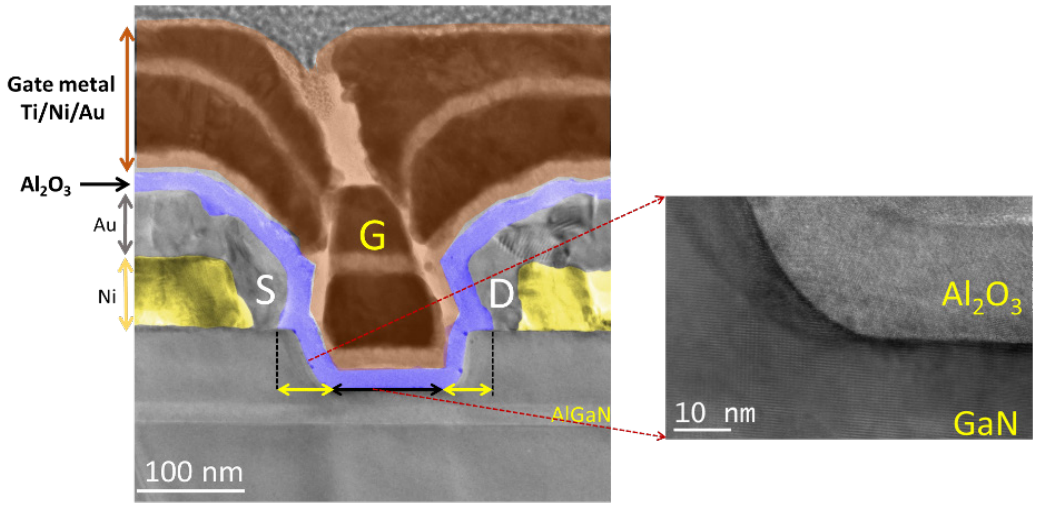
N. Chowdhury, Q. Xie, M. Yuan, T. Palacios
Sponsorship: Intel Corporation

GaN-CMOS-technology could be instrumental towards realizing high-power-density, high-speed, low-form-factor, and highly-efficient power electronic circuits, which sparked many efforts to develop a high performance GaN p-FET. However, most of these demonstrations show normally-ON operation with ON-resistance over 1 kΩ·mm. GaN/AlInGaN heterostructure-based p-FET shows low ON-resistance because of higher 2-DHG density and hole mobility but with D-mode operation. A GaN/AlN heterostructure based p-FET shows E-mode operation with RON of 640 Ω·mm. However, n-FET integration with this p-FET requires regrowth.

In this work, we demonstrate a self-aligned p-FET with a GaN/Al0.2Ga0.8N (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on Si substrate. The utilization of GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionality.

While most of the GaN p-FET demonstrations so far in the literature mainly focused on recessed gate MISFET structure, we choose to develop a self-aligned structure (see Figure 1 for the device structure) as it offers the following advantages over a recessed gate MIS p-FET: (1) the shortest possible source to the drain distance, cutting down the access region; (2) low ON-resistance because of negligible access resistance: and (3) easier gate alignment.

Our 100-nm channel length self-aligned device with recess depth of 70 nm exhibits a record ON-resistance of 400 Ω·mm and ON-current over 5 mA/mm with ON-OFF ratio of 6×105 when compared with other p-FET demonstrations based on a GaN/AlGaN heterostructure (see Figure 2 for benchmarking of our device with other p-FET demonstrated in the literature). The device shows E-mode operation with a threshold voltage of −1 V, making it a promising candidate for a GaN-based complementary circuit that can be integrated on a Si platform. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated.



▲ Figure 1: Transmission electron microscopy (TEM) image of the fabricated self-aligned p-FET with 100-nm channel length. TEM image showing the smooth interface between the GaN and gate dielectric attesting to the high quality of gate recess process with low surface roughness.

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Characterizing and Optimizing Qubit Coherence Based on SQUID Geometry

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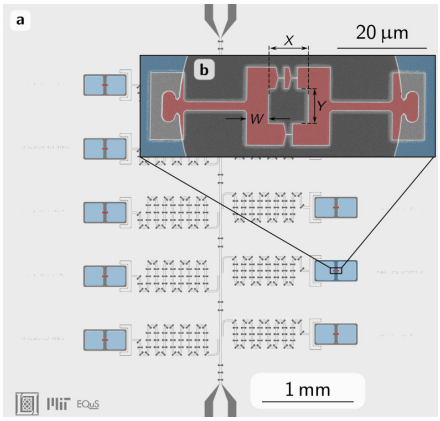
Superconducting qubits are leading candidates to implement quantum hardware capable of performing certain computational tasks more efficiently than their classical counterparts. A prerequisite for scalable quantum computation is a sufficiently low noise level in the participating qubits. The dominant source of decoherence in frequency tunable superconducting qubits is 1/f flux noise, presumably originating from magnetic defects located at the interfaces of their SQUID loops.

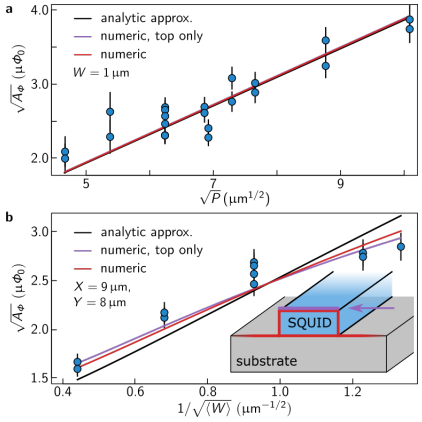
Here, we measure the flux noise amplitudes of more than 50 capacitively shunted flux qubits and study their dependence on geometric parameters of their SQUID loops. Each of six chips (Figure 1) holds ten capacitively shunted flux qubits, featuring two copies of five different SQUID loop geometries, respectively. Dispersive readout of each qubit is performed using a common transmission line and individual readout resonators. We perform a series of spin-echo measurements in the vicinity of the flux sweet spot of the qubits, showing that the pure dephasing rate is proportional to the slope of the qubit spectrum, which is in turn related to the flux noise amplitude for each qubit.

Our data (Figure 2) show good agreement with a previously presented microscopic model for independent spin impurities, which has so far eluded experimental verification. Due to a limited applicability of the proposed model for superconducting films of finite thickness, we provide numerical simulations of the current distribution in our SQUIDs, which extend and refine the considered model. Our improved model is in excellent quantitative agreement with our data both in terms of absolute numbers and geometry dependence (Figure 2b).

Our results demonstrate that flux noise is suppressed in SQUIDs with small perimeters, fat wires, and thick superconducting films therefore serve as a guide for minimizing the flux noise susceptibility in future circuits.



▲Figure 1: Noise spectroscopy device. (a) Optical micrograph of one of the utilized samples. (b) Electron microscopy image of a fabricated SQUID loop with labeled geometry parameters.



▲Figure 2: Flux noise amplitudes √(A_Φ) as a function of SQUID geometry parameters for (a) constant wire width W and (b) constant inner perimeter 2X + 2Y. Each line corresponds to an independent two-dimensional fit to basic and extended versions of the model using a single free parameter.

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Control of Conducting Filaments Properties in TiO2 by Structural and Chemical Disorder for Neuromorphic Computing

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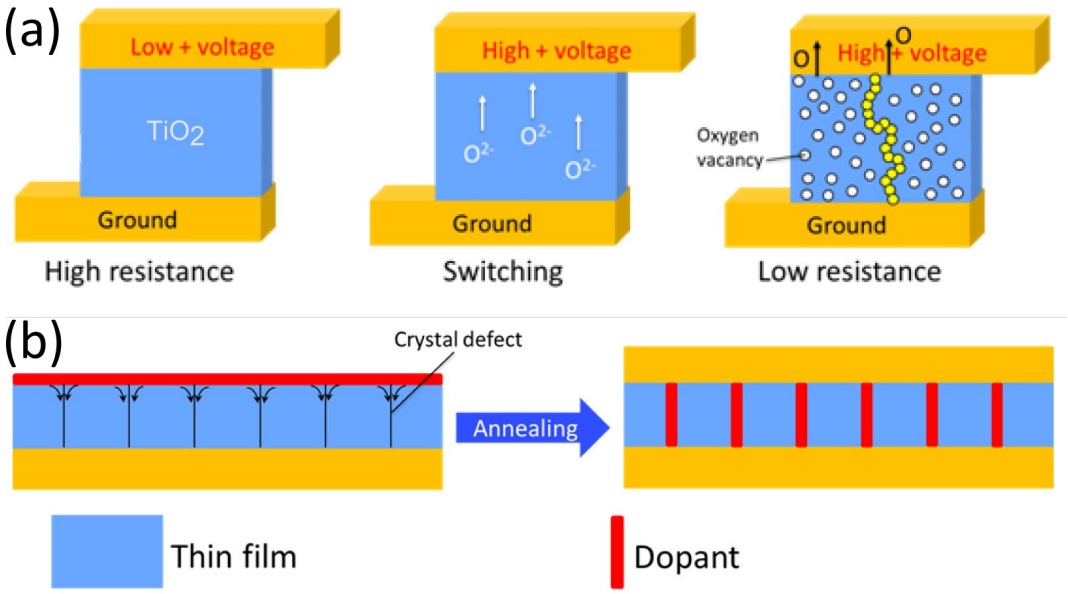
Sponsorship: Fonds de Recherche du Québec - Nature et Technologies (FRQNT)

Resistive switching (RS) random access memories are considered as possible artificial synapses in next-generation neuromorphic networks, mostly due to their predicted high memory density, energy efficiency and scalability. Integration of these devices in a neuromorphic computing system could allow solving intensive computing tasks actually only handled by the human brains such as speech and character recognition as well as grammar and noise modeling. Within their architecture, redox-based RS memory devices store binary code information using the electric field-induced resistance change of an oxide layer by conductive filament (CF) formation and rupture (Figure 1a). Nevertheless, a lack of control on the properties of CFs, which mainly forms at chemical and structural defects, causes detrimental cycle-to-cycle and device-to-device variations.

We are therefore studying the effect of strain on the microstructure, chemistry and RS properties of TiO2 thin films to get insights into defects formation with the objective of selectively doping along these defects (Figure 1b). We found that the microstructural properties of pulsed laser deposited epitaxial TiO2 films depend on both the film thickness and the nature of the bottom electrode, suggesting a potential method to better control defects properties and improve consistency in RS.



▲ Figure 1: (a) Resistive switching mechanism in a TiO2 thin film by formation of conductive filaments and (b) its control by selective doping at microstructural defects.

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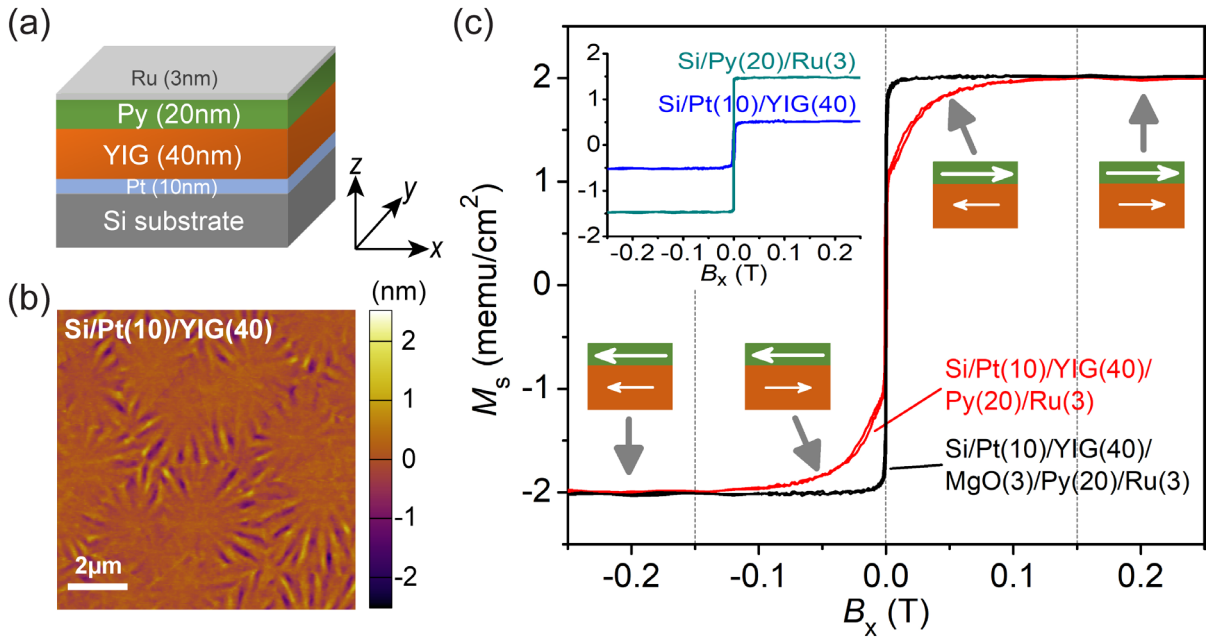
Manipulation of Coupling and Magnon Transport in Magnetic Metal-insulator Hybrid Structures

Y. Fan, J. Finley, J. Han, L. Liu
Sponsorship: NSF, SRC-NRI, NSF-MRSEC

Ferromagnetic metals and insulators are widely used for generation, control, and detection of magnon spin signals. Most magnonic structures are based primarily on either magnetic insulators or ferromagnetic metals, while heterostructures integrating both of them are less explored. Here, by introducing a Pt/yttrium iron garnet (YIG)/permalloy (Py) hybrid structure grown on Si substrate (Figure 1(a)), we studied the magnetic coupling and magnon transmission across the interface of the two magnetic layers. After the film growth by magnetron sputtering, atomic force microscopy (AFM) measurements were performed (Figure 1(b)) to characterize the film quality, which indicates a surface roughness of approximately 1 nm. Moreover, we found that within this structure, Py and YIG exhibit an antiferromagnetic coupling field as strong as 150 mT, as evidenced by both the vibrating-sample magnetometry (VSM) (Figure 1(c)) and polarized neutron reflectometry measurements. By controlling individual layer thicknesses and external fields, we realize parallel and antiparallel magnetization configurations, which are further utilized to control the magnon current transmission. We show that a magnon spin-valve with an ON/OFF ratio of ~130% can be realized out of this multilayer structure at room temperature through both spin pumping and spin Seebeck effect experiments. Owing to the efficient control of magnon current and the compatibility with Si technology, the Pt/YIG/Py hybrid structure could potentially find applications in magnon-based logic and memory devices.



▲ Figure 1: (a), Schematic of the Pt/YIG/Py/Ru hybrid structure grown on the Si/SiO2 substrate. (b), AFM image of the YIG surface for the Si/Pt/YIG film, indicating a roughness of around 1 nm. (c), VSM measurements of the Si/Pt/YIG/Py/Ru sample and Si/Pt/YIG/MgO/Py/Ru sample. Inset shows results from control samples of Si/Py/Ru and Si/Pt/YIG. The schematics show the magnetization orientation of the YIG and Py layers in the Si/Pt/YIG/Py/Ru hybrid structure in different magnetic field regions.

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Nonvolatile Control of Long-distance Spin Transport in an Easy-plane Antiferromagnetic Insulator

J. Han, P. Zhang, Y. Fan, T. S. Safi, J. Xiang, R. Cheng, L. Liu
Sponsorship: NSF, NIST

How an antiferromagnet transmits spin angular momentum by the quanta of spin-wave excitations, viz. magnons is one of the core topics of antiferromagnetic magnon spintronics. It is generally believed that only easy-axis antiferromagnets can support spin transmission, a natural inference of the fact that the circularly polarized magnons there have finite spin angular momentum. In contrast, easy-plane antiferromagnets would destroy spin transport due to the vanished angular momentum carried by their linearly polarized magnons.

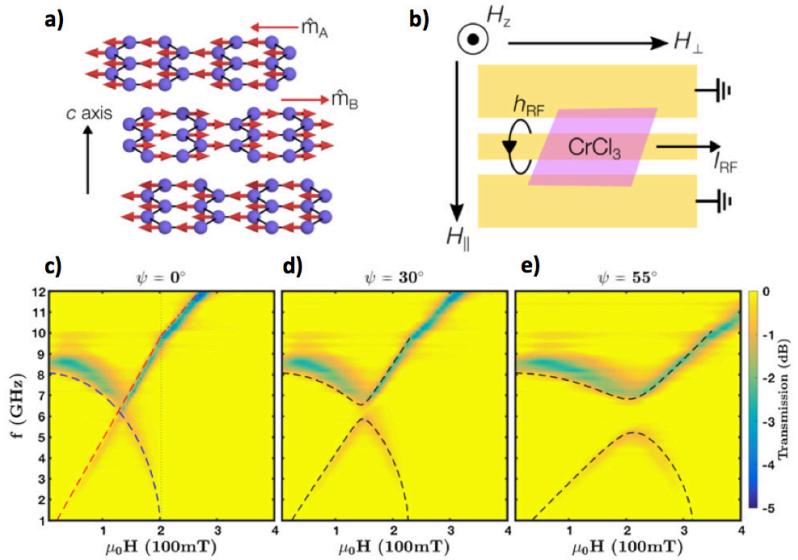
In this work we show that contrary to this traditional picture, spin transmission over micrometer distance indeed happens in an easy-plane insulating antiferromagnet, α-Fe2O3 thin film. A model involving superposition of linearly polarized propagating magnons is proposed to account for the observations. Enabled by this physical insight, our work opens up additional possibilities for nonvolatile, low magnetic field control of spin transmission, where a spin-current switch with a 100% on/off ratio is realized.

Gigahertz Frequency Antiferromagnetic Resonance and Strong Magnon-magnon Coupling in the Layered Crystal CrCl3

J. T. Hou, D. MacNeill, D.R. Klein, P. Zhang, P. Jarillo-Herrero, L. Liu
Sponsorship: NSF

Antiferromagnetic spintronics is an emerging field with potential to realize high-speed memory devices. Compared to ferromagnetic materials, antiferromagnetic dynamics are less well understood, partly due to their high intrinsic frequencies that require terahertz techniques to probe. Here, we introduce the layered antiferromagnetic insulator CrCl3 as a tunable platform for studying antiferromagnetic dynamics. Because of weak interlayer coupling, the antiferromagnetic resonance (AFMR) frequencies are within the range of typical microwave electronics (<20 GHz). This allows us to excite different modes of AFMR and to induce a symmetry-protected mode crossing with an external magnetic field. We further show that a tunable coupling between the optical and acoustic magnon modes can be realized by breaking rotational symmetry. Recently, strong magnon-magnon coupling between two adjacent magnetic layers has been achieved, with potential applications in hybrid quantum systems. Our results demonstrate strong magnon-magnon coupling within a single material and therefore provide a versatile system for microwave control of antiferromagnetic dynamics. Furthermore, CrCl3 crystals can be exfoliated down to the monolayer limit, allowing device integration for antiferromagnetic spintronics.

We transferred layered bulk CrCl3 onto a coplanar waveguide (CPW) and secured it with Kapton tape. The crystal c-axis is normal to the CPW plane. We measure microwave transmission in a cryostat by fixing the excitation frequency and sweeping the applied magnetic field. When the field is applied in-plane and parallel to the in-plane radio frequency field, both acoustic and optical modes of AFMR are observed. The mode frequency evolutions are well-described by theoretical formulas. When the field is canted out-of-plane, two magnon modes hybridize because of rotational symmetry breaking, and the coupling strength is tunable by rotation angle. Our results demonstrate that CrCl3 serves as a convenient platform for studying AFMRs in microwave frequencies and shows the possibility to realize magnon-magnon coupling utilizing van der Waals assembly.



▲ (a) Magnetic structure of CrCl3 below Neel temperature. (b) CPW with CrCl3 with field along H||. (c)(d)(e) Microwave transmission as functions of frequency and applied field at 1.56K, with field at 0o, 30o, and 55o from sample plane, respectively.

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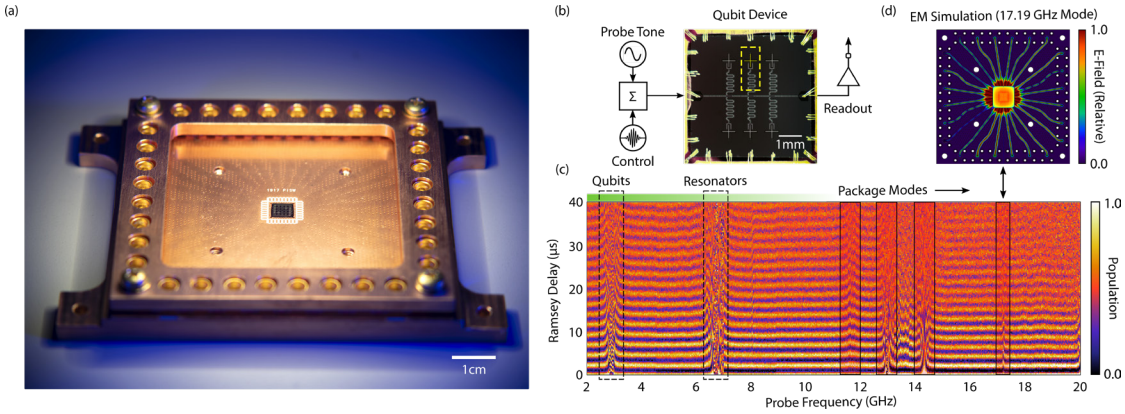
High-density Microwave Packaging for Superconducting Quantum Information Processors

S. Huang, B. Lienhard, T. P. Orlando, S. Gustavsson, W. D. Oliver
Sponsorship: ARO grant No. W911NF-18-1-0411; Office of the Director of National Intelligence (OD-NI), Intelligence Advanced Research Projects Activity (IARPA) under Air Force Contract No. FA8721-05-C-0002

Quantum information processors hold the promise to solve specific computational problems much faster than classical computers. Superconducting qubits are among the leading candidates for realizing near-term quantum processors. Beyond lithographic scalability, superconducting qubits offer long computational operation windows–coherence times–relative to short operational gate times that have enabled the demonstration of the first practical quantum algorithms. Despite this progress, engineering challenges must be met to further scale these devices. In particular, qubits require a precisely engineered microwave environment to suppress energy decay and corresponding information loss. For instance, the corruption of information can occur due to lossy package modes interacting with the qubit electric field. As the number of qubits increases, qubit packages must be adapted to support an increasing number of input/output ports without adding additional loss channels.

Our qubit package, shown in Figure 1 (a), provides a well-defined electromagnetic (EM) environment. It consists of an aluminum-coated copper cavity and a microwave interposer with 32 waveguides. We performed full-wave simulations of the signal launches, the package cavity, and superconducting wirebonds to establish principles needed to construct larger packages. We evaluated the presence and absence of lossy package modes using high-coherence qubits as sensors, illustrated in panel (b).

A weakly driven package mode causes EM-field enhancement with increased microwave photon number fluctuations, which, when coupled to the qubit, shifts its energy levels. The resulting qubit energy fluctuations result in qubit dephasing inferable via Ramsey interferometry. Sweeping a probe tone in frequency while monitoring the coherence time reveals the presence of parasitic package modes. Panel (c) exhibits a mode-free operating environment up to 11 GHz. Our EM model can reproduce the observed package modes, shown in panel (d). Current work focuses on the design of packages to support more complex qubit chips and modular interconnects to facilitate fast chip exchange.



▲ Figure 1: (a) Microwave package with 32 signal lines to control 16-qubit chip mounted in package center. (b) Measurement setup to probe electromagnetic modes in qubit environment. Measured qubit is indicated with yellow dashed box. (c) Continuous coherence time measurements via Ramsey interferometry at probe tone frequencies between 2 and 20 GHz. Frequency range relevant to qubit is indicated by green horizontal bar. (d) EM simulation (COMSOL) of package resonance mode that corresponds to feature measured at 17.19 GHz.

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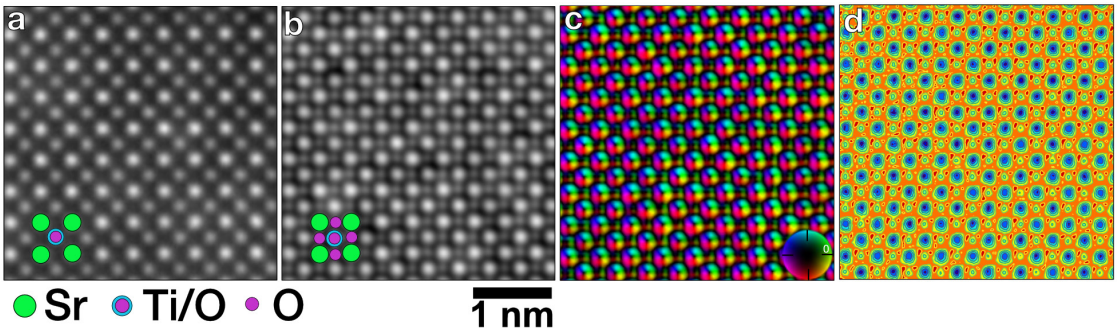
Scanning Transmission Electron Microscopy Imaging of Materials

A. Kumar, X. Chen, M. Xu, M. Hauwiller, A. Kaleta, A. Penn, J. LeBeau
Sponsorship: AFOSR

Properties of materials are controlled by the arrangement and type of atoms in the structure. Many characterization techniques can provide information about the crystal structure and micro scale features, but atomic scale information is critical for fully understanding a material system. Through advanced scanning transmission electron microscopy (STEM) techniques, atomic column intensity and positions can be extracted to provide useful information about ordering, local distortions, and defects.

Materials such as strontium titanate, $SrTiO_3$, demonstrate the capabilities of this powerful imaging technique. Annular dark field (ADF) STEM imaging shows atom column contrast from Sr and Ti cations, as expected from the crystal structure, but no contrast from the oxygen anion atom columns due to the low atomic number of oxygen (Figure 1 a). Integrated differential phase contrast (iDPC) imaging in the STEM mode makes the lighter oxygen atoms visible (Figure 1 b). Additionally, the electric field vector map in projection can be found from the differential phase contrast data acquired from a four-segment detector (Figure 1 c). Projected charge density maps obtained from differential phase contrast imaging clearly show symmetrical charge contours revealing non-polar behavior in the $SrTiO_3$ sample (Figure 1 d). Such a projected charge density imaging technique is useful in studying polar functional material.

The positions and intensity of each atom column can be extracted from the STEM images using image analysis techniques. Detailed, quantitative analysis of bond lengths, bond angles, and atomic contrast can be used to find regions of order, local distortions, and defects. Structural nanoscale features such as ferroelectric/ferromagnetic domains or chemical/distortion-ordered regions can be correlated with the electrical, mechanical, ferroelectric, magnetic, and other properties of the material to elucidate the nanoscale origin of macroscale properties.



▲ Figure 1: (a) ADF STEM image, (b) iDPC image, (c) projected electric field vector map, and (d) projected charge density map from $SrTiO_3$.

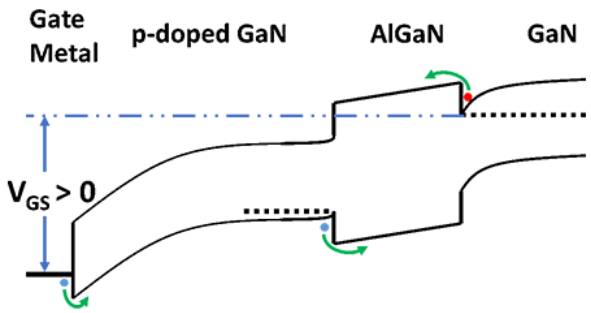
Degradation Under Forward Bias Stress of Normally-off GaN High Electron Mobility Transistors

E. S. Lee, J. A. del Alamo
Sponsorship: Texas Instruments

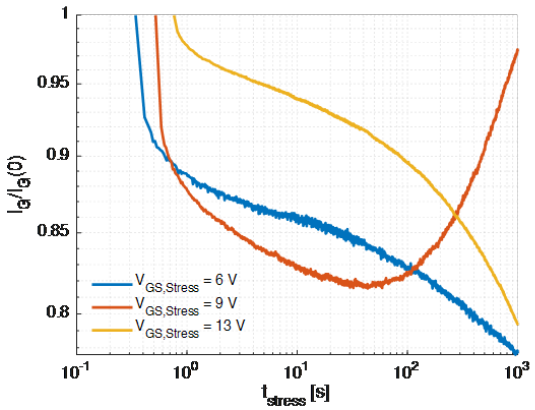
Energy-efficient electronics have been gaining much attention as a necessary path to meet the growing demand for energy and sustainability. GaN field-effect transistors (FETs) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry a high current with minimum losses. For best circuit reliability and performance, a normally-off transistor is highly desirable. An attractive design is the p-doped gate AlGaN/GaN high electron mobility transistor (p-GaN HEMT).

Our research aims to better understand the reliability issues impeding widespread adoption of p-GaN power HEMTs for power management applications. One key issue is device degradation under electrical stress, where key device performance figures such as the threshold voltage and the gate leakage current change with electrical stress.

Understanding reliability issues of p-GaN power HEMTs is obstructed by the complex gate stack of the devices. First, both holes and electrons are present in the gate stack: holes in the p-doped GaN region and electrons in the 2-dimensional electron gas at the AlGaN/GaN interface. Furthermore, holes and electrons encounter several barriers (shown in the energy band diagram of Figure 1), obfuscating understanding of the electrostatics and transport physics under forward-bias stress. Coupled with the often time-dependent nature of degradation, p-GaN power HEMT reliability remains difficult to fully understand. For instance, Figure 2 shows the time evolution of the gate leakage with different constant gate voltage stress. As can be easily seen, the gate leakage current decreases with time at lower biases and high biases but increases with time at intermediate biases, showing a complex multi-regime behavior. Nevertheless, an on-going reliability analysis such as breakdown voltage indicates that p-GaN HEMTs show great promise as robust and efficient next-generation power transistors.



▲ Figure 1: Schematic energy band diagram of gate stack at forward bias, indicating location of various barriers for hole and electron current flow.



▲ Figure 2: Gate leakage current with VGS = 6 V, 9 V, and 13 V, showing the complex time dependent behavior with continued stress.

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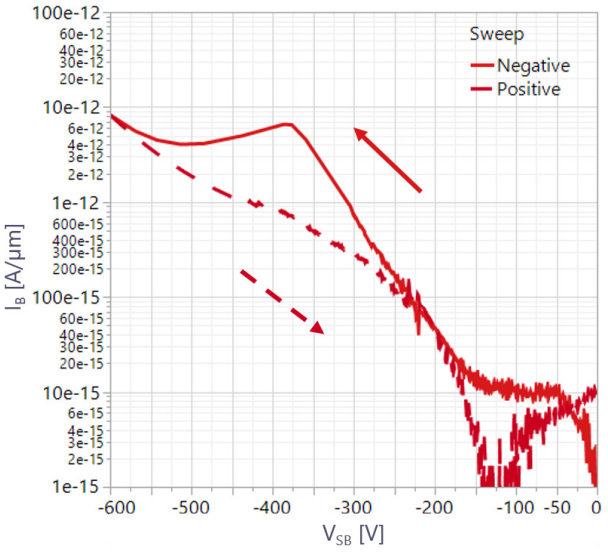
Vertical Leakage Characteristics of GaN Power Transistor

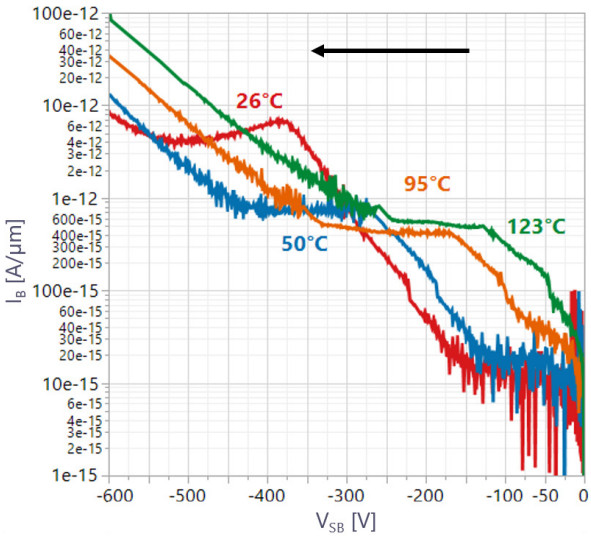
A. Massuda, J. A. del Alamo

The great promise of Gallium Nitride Metal-Insulator-Semiconductor High Electron Mobility Transistors (GaN MIS-HEMTs) in the growing power electronic market has rapidly positioned these devices at the forefront of a new technology wave. This has triggered a vast amount of worldwide research and yielded continuous improvements in device performance and electrical reliability. Regarding reliability, a key consideration in any new device technology, the maximum breakdown voltage is ultimately limited by the vertical breakdown of the drain-body junction. This is particularly a concern for devices with conductive substrates.

A way to mitigate premature drain-body breakdown under high positive drain voltage consists of applying a positive voltage to the body with respect to the source so that the drain-body voltage can be reduced. A potentially problematic consequence of this is excessive source-body leakage current under off conditions. This is undesirable. In this work, we study the source-body leakage in commercially prototype devices for negative voltage at the source with respect to the body. Figure 1 shows the body current as the source is swept negative and then positive at 26. The different paths that are followed and the "eye" that appears could be due to trapping or a floating-body effect. Figure 2 shows the temperature dependence of the negative sweep. The sharp corner in the characteristics that coincides with the maximum widening of the "eye" opening appears to have a negative temperature coefficient of -0.13 eV. These and other interesting features are critical to understanding the origin of the reverse bias source-body current so that it can be suppressed.



▲Figure 1: I-V characteristics between source contact and the substrate. During the measurement, the drain and gate terminals are floating, the substrate is kept at 0V and the source is swept down from 0V to -600V (solid line) and then back to 0V (dashed line).



▲Figure 2: Temperature dependence of negative sweep of I-V characteristics between source contact and the substrate. During the measurement, the drain and gate terminals are floating, the substrate is kept at 0V and the source is swept down from 0V to -600V.

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Quantum Landscape Engineering of Superconducting Circuit Ground States for Higher-order Coupler Design

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Sponsorship: Office of the Director of National Intelligence, IARPA, Assistant Secretary of Defense for Research & Engineering under Air Force

Superconducting circuits provide a versatile engineering platform for the study of quantum systems and their use as a computational resource. Their application ranges from studying fundamental principles such as the physics of quantum entanglement to the demonstration of large-scale control of quantum bits simulating spin models in solid state physics. Many-body interactions of multiple spins simultaneously are one aspect of spin models that has not been demonstrated to date.

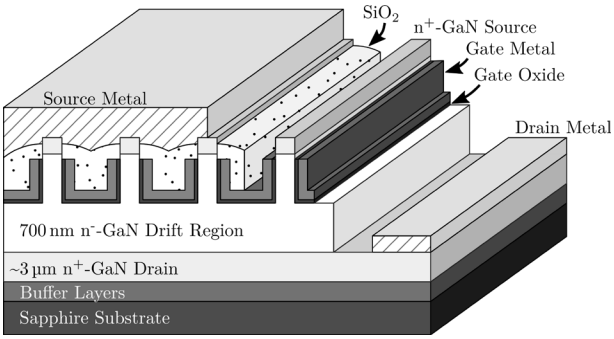
In this work, we exploit that the response of the quantum ground state energy of a superconducting circuit to external magnetic flux can be shaped by design to engineer artificial spin couplers. We propose a methodology for adding higher-order polynomial terms into the ground state energy versus flux by strongly coupling a series of rf SQUIDs. The fundamental instance of two rf SQUIDs generating a ground state with 4th-order terms is implemented experimentally. Probing this circuit with a sensor flux qubit, the qubit's transition frequency maps the derivative of the quartic ground state in accordance with simulation. Modest levels of qubit coherence are maintained despite the relatively strong inductive coupling. These results demonstrate the viability of this design for use as a 4-local coupler and show promise for extending it to higher polynomial order.

Vertical Gallium Nitride FinFETs for RF Applications

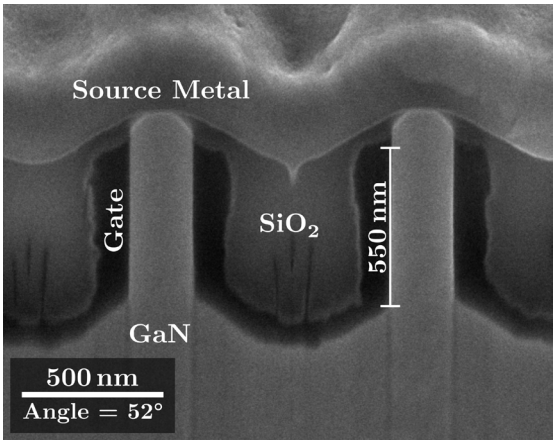
J. Perozek, A. Zubair, T. Palacios
Sponsorship: DARPA DREaM Project, GaN Energy Initiative

From wireless communication systems like the 4G and 5G cellular services that enable 4K video streaming, to the high-resolution radars that are vital to national defense, radio frequency (RF) systems have become a ubiquitous part of modern life. A fundamental building block within these systems is the RF power amplifier. As amplifier technology progresses, the relentless demand for improved performance necessitates development of new transistor technologies that can operate at higher power levels and over larger bandwidths. While traditional planar processing techniques have led to countless successful RF amplifiers, the fact that all conduction takes place very near the wafer's surface fundamentally limits their performance. If instead we utilize a compact vertical transistor design, the bulk material can be used to withstand large voltages in the vertical direction as opposed to lateral designs, which need large device areas. Additionally, bulk conduction improves thermal spreading, thereby reducing cooling needs, and vertical gate patterning techniques trade expensive high-resolution lithography for relatively easy control of etch depth.

This work presents novel vertical GaN RF transistors. As the cross-sectional diagram in Figure 1 shows, the vertical GaN RF finFET consists of narrow fins to confine the current and has sidewall gates to modulate the conductivity within the fins. To enable high-frequency system integration, these devices were fabricated on sapphire, a highly insulating substrate, with a top-side drain contact to remove the need for through-wafer vias. To reduce costs and allow easier integration with existing technology, the same devices can be fabricated on GaN on Si as well. Figure 2 shows a scanning electron microscope (SEM) cross section of a fabricated device. These devices achieve a current density of over 7 kA-cm-2 and a power gain cut-off frequency, fmax, of 5.9 GHz, demonstrating a promising first step toward vertical GaN transistors in RF applications.



▲ Figure 1: Cross-sectional schematic of the vertical GaN RF FinFET.



▲ Figure 2: SEM cross-section of the fabricated devices taken in a focused ion beam system.

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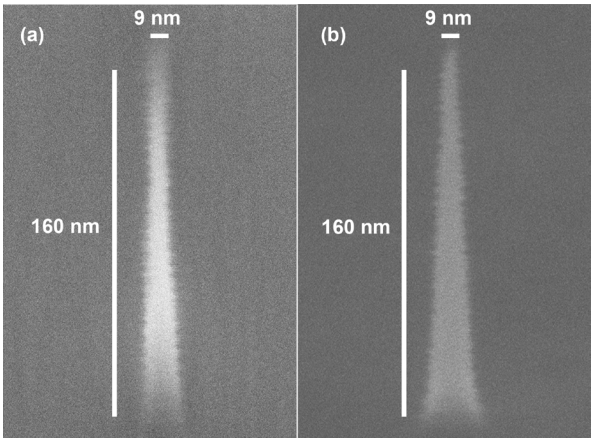
Towards Sub-10-nm-Diameter Vertical Nanowire III-V Tunnel FETs

Y. Shao, J. A. del Alamo
Sponsorship: Intel

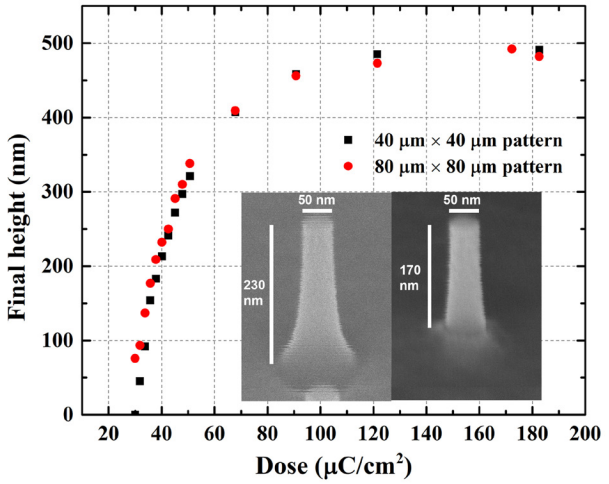
Recently, III-V compound semiconductors have emerged as a promising family of materials for future complementary metal-oxide semiconductor (CMOS) technology, thanks to their superior electron transport properties. To enable continued scaling, a high aspect-ratio vertical nanowire (VNW) transistor geometry with a gate-all-around (GAA) structure is highly favorable due to effective charge control and robustness to short-channel effects. Another big advantage of the vertical nanowire geometry is that it allows engineering of the energy band structure along the transport direction, enlarging the device design space. In particular, device structures that potentially break the thermal limit of the subthreshold behavior become possible.

In our research, we are pursuing the demonstration of broken-band GaSb/InAs vertical nanowire tunnel field-effect-transistors (TFETs) with sub-10-nm diameter for ultra-low power logic applications. We aim to exploit the recent demonstration of high-quality III-V MOS interface characteristics using in-situ thermal atomic-layer etching in combination with atomic layer deposition of the gate stack.

In our work, we have developed a top-down approach for sub-10-nm VNW fabrication, as shown in Figure 1. Hydrogen silsesquioxane (HSQ) hardmask is patterned by electron beam lithography (EBL), followed by Cl-based reactive-ion-etching (RIE) and alcohol-based digital etch (DE). Planarization is another critical step, in which insulating layers are formed around the VNWs with good vertical location control. We have developed a method to accurately control the thickness of an HSQ film using EBL with different electron doses. Figure 2 shows the final height of HSQ as a function of e-beam dose. The insets in Figure 2 show an example of a 60- nm-thick planarized HSQ spacer formed around a 230-nm-high InAs VNW.



▲Figure 1: Sub-10-nm diameter (a) InGaAs VNW and (b) GaSb VNW fabricated by RIE and DE techniques. HSQ is on top of the VNWs.



▲Figure 2: Final height of HSQ film vs. e-beam dose with initial HSQ thickness of 490 nm. The insets show a 60-nm-thick planarized HSQ film (right) fabricated around a 230-nm-high InAs VNW (left).

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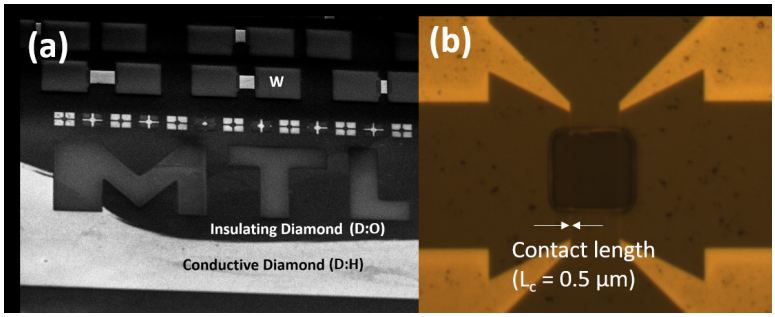
W Contacts to H-terminated Diamond

A. Vardi, M. Tordjman, R. Kalish, J. A. del Alamo
Sponsorship: Bose, DARPA

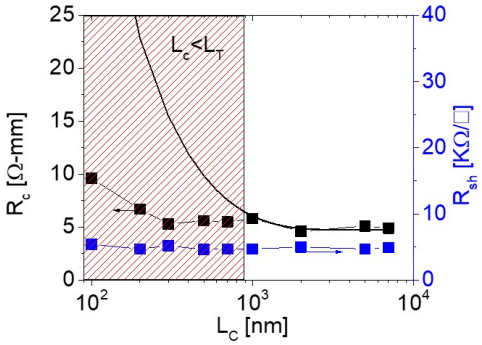
Diamond is considered a leading candidate for harsh environment high-power electronics due to their extraordinary thermal and electrical properties. One of the many challenges facing diamond electronics is creating reliable and stable ohmic contacts to hydrogen-terminated diamond (D:H). In this work we explored a novel approach for scalable and self-aligned ohmic contacts to D:H. Our results show that using this approach stable ohmic contacts can be obtain with state-of-art contact resistance.

The diamond surface conductivity is governed by its surface termination. H-termination leads to a conductive surface, while O-termination (D:O) results in insulating diamond. The different terminations are typically obtained by exposing the diamond surface to H or O plasma (fig. 1). Since in D:H all the dangling bonds are practically passivated, it is typically hydrophobic and suffers from poor adhesion to most materials which are only weakly attached by Van der Waals forces. D:O however, is hydrophilic and can provide good adhesion. This create a problem for ohmic contacts which usually need to be laid over a conductive surface. To overcome this issue in our approach we first pattern W contact on D:O providing good adhesion. After this, the diamond surface is exposed to the H plasma. We use W in this approach since it is one of the few metals that can withstand prolongued exposure to H plasma at elevated temperature without being damaged or go through embrittlement.

To test our approach, we fabricated four terminal TLM test structures with nano contacts. From the analysis of the data (Fig. 2), we extract the contact resistance (black markers), as well as the D:H (blue markers) as a function of contact length Lc (Fig. 1 right). Since this is a 'side contact', it does not follow the classical transfer length behavior obtained when Ohmic contacts are overlapping a conductive surface (Fig. 2, full line). Rather, the contact resistance is insensitive to the contact length. Notably, the sheet and contact resistance are in par with other approaches to obtain ohmic contacts to D:H.



▶ Figure 1: (a) SEM image of Diamond resistor test structure. Black area is D:O, white is D:H and the patterned W contacts are also shown. (b) microscope image of four terminals nanocontact TLM test structure.



◀ Figure 2: The contact resistance (black markers, left scale) and D:H sheet resistance (blue markers, right scale) as a function of contact length (Lc) defined in Fig. 1.

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Cryogenic GaN HEMT Technology for Application in Quantum Computing Electronics

Q. Xie, N. Chowdhury, M. Sánchez Lozano, A. Zubair, J. Lemettinen, I. Charaev, M. Colangelo, O. Medeiros, K. K. Berggren, T. Palacios
Sponsorship: IBM

High performance and scalable cryogenic electronics is an essential component of future quantum information systems, which typically operate below 4K. Current electronics rely on technology like CMOS (Si), or heterojunction bipolar transistor (e.g. SiGe, InP).

This work explores the use of wide band gap heterostructure electronics, specifically the AlGaN/GaN high electron mobility transistor (HEMT), for cryogenic low-noise applications. These structures take advantage of the polarization-induced two-dimensional electron gas to create a high mobility channel, hence eliminating the use of heavy doping as in the other semiconductor technologies. Epitaxially-grown GaN-on-Silicon wafers are available in large (8 inch / 200 mm) substrates, therefore making the technology an excellent candidate for scalable RF electronics in quantum computing systems.

Furthermore, the use of electrodes using superconducting materials is proposed to significantly reduce the parasitic components and therefore push the RF performance of cryogenic devices. Short-channel transistors with NbN gates of length 100 nm have been demonstrated with promising performance.

In the next step, the effect of the superconducting gate on RF characteristics of the transistors will be studied, with the eventual goal of pushing the frequency performance of these transistors to new limits. These transistors will be integrated into low noise amplifier circuits for applications in readout and control electronics at cryogenic temperature. Furthermore, the developed cryogenic GaN HEMT technology would bring us one step closer to an all-nitride integrated electronics-quantum device platform.

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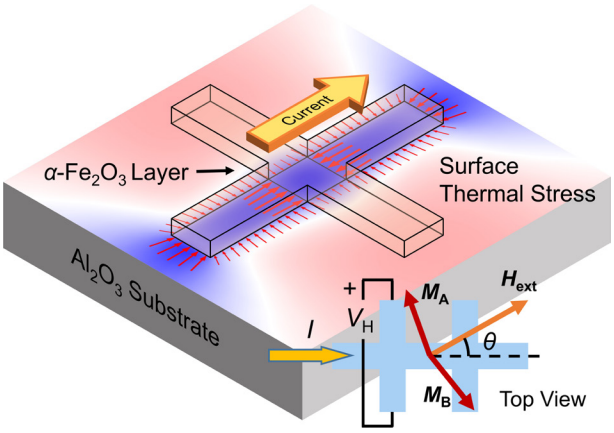
Quantitative Study on Current-induced Effects in an Antiferromagnetic Insulator/Pt Bilayer Film

P. Zhang, J. Finley, T. Safi, L. Liu
Sponsorship: NSF, National Institute of Standards and Technology

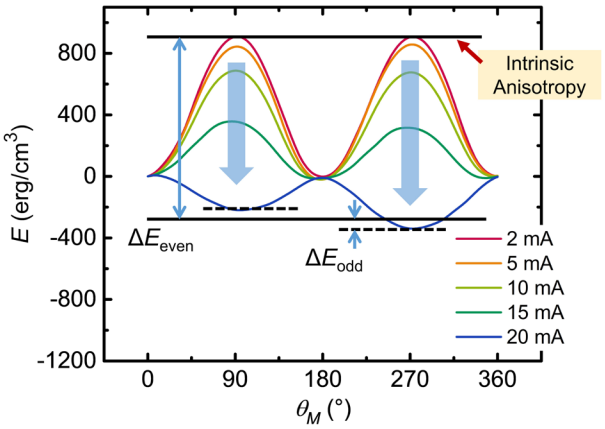
Electrical control and detection of magnetic ordering inside antiferromagnets have attracted considerable interests, for making next generation of magnetic random access memory with advantages in speed and density. However, a full understanding of the recent prototypical spin-orbit torque antiferromagnetic memory devices requires more quantitative and systematic study.

Here we study the current-induced switching in a canted antiferromagnetic insulator α-Fe2O_3, similar to previous demonstrations of antiferromagnetic memories, but make good use of its uniquely small spin flop field. We compare the current-induced Hall resistance to the field-induced one, and look into the nature of the switching. We raise the concern that the signal in these memory devices can be complicated by two neglected sources that are unrelated to spin-orbit torques, while the contributions from spin-orbit torques are much smaller than expected. This work provides a pathway towards the clear realization of a spin-orbit torque antiferromagnetic insulator memory device.

We epitaxially grew the α-Fe_2O_3 (0001) film on α-Al_2O_3 substrate. In Pt/α-Fe_2O_3 bilayer, we found a typical antiferromagnetic spin Hall magnetoresistance (SMR). We performed the conventional current-induced switching in the Hall cross devices and obtained a sawtooth-like behavior. However, it remained almost unchanged under magnetic field, which means a purely resistive switching. To exclude that, we measured the angle-dependent SMR curve subject to an in-plane rotating field when applying different sensing currents. The current always tilts the Néel vector towards itself, which is quantified by two effective magnetic energy changes, with 180° and 360° angle period, respectively. Macrospin simulation based on the conventional damping-like torque cannot reproduce the results, while a newly-proposed thermo-magnetoelastic effect well explains the data. The 360° period energy change, instead, can be explained by a field-like spin-orbit torque.



▲Figure 1: The dominant cause of magnetic switching in the α-Fe_2O_3 Hall bar device is the thermo-magnetoelastic effect. The Joule heating in the adjacent Pt layer induces a thermal stress on the substrate surface and switches the magnetic order of α-Fe_2O_3.



▲Figure 2: The current-induced magnetic order switching is quantified by rotating an in-plane field and measuring the angle-dependent magnetic energy. The even (180° period) term and the odd (360° period) term are attributed to the thermo-magnetoelastic effect and the field-like torque, respectively.

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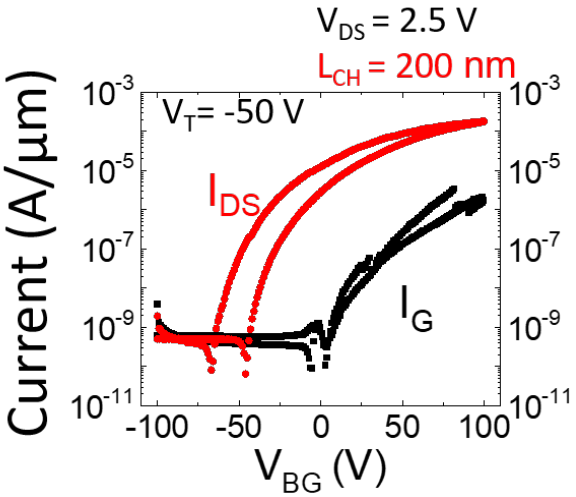
High-performance 2D Material Devices for Large-scale Integrated Circuits and Power Electronic Applications

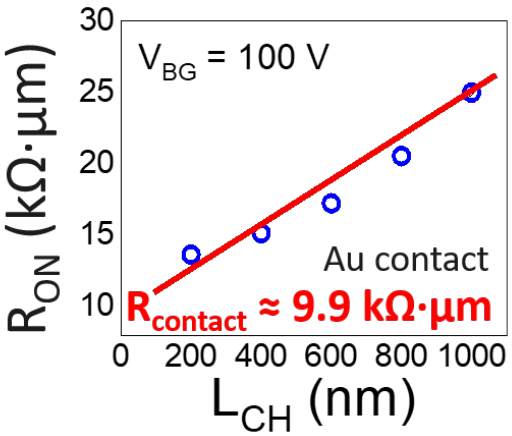
J. Zhu, M. Xue, T. Palacios
Sponsorship: SRC

Among all the possible back-end-of-line (BEOL) solutions to improve the integration density and functionality of conventional silicon circuits, 2D material devices are believed to be very promising, due to their high mobility, relatively large band gaps, and atom-level thickness. These devices are beneficial for both logic integrated circuits and power electronic applications. However, the large area growth of high quality 2D material thin films and 2D material devices and achieving low contact resistance have always been challenging and hinder the development of 2D material devices and circuits.

Recently, by using Au contacts and MOCVD technique, we have fabricated back-gated MoS2 transistors on 4-inch MoS2 wafer with 200-nm channel length and have obtained excellent device performance, i.e., high on-state current of around 220 μA/μm (Figure 1) and low contact resistance of around 9.9 kΩ·μm (Figure 2). In order to have larger scale 2D materials with better quality, we are currently building a MOCVD system in EML labs to grow 2D materials, e.g., MoS2 and WSe2, on 6-inch wafers. We are also using Li-induced phase transition in the source/drain regions to further reduce the contact resistance of 2D material transistors. Moreover, top-gated MoS2 transistors with a multilayer hBN gate dielectric are also being investigated to improve the gate controllability and the mobility of the channel materials. In the very near future, we hope to demonstrate 2D material circuits, such as multiplexers, and DC-DC converters with high performance 2D material devices.



▲ Figure 1: Measured transfer characteristic of a back-gated MoS2 transistor with Au source/drain contacts and 285-nm SiO2 gate dielectric. The source/drain current reaches 220 μA/μm in the on-state.



▲ Figure 2: Measured on-state resistance (Ron) of back-gated MoS2 transistors with Au source/drain contacts, 285 nm SiO2 gate dielectric, and channel lengths (LCH) from 200 nm to 1 μm. The extrapolated contact resistance in this case is about 9.9 kΩ·μm.

FURTHER READING

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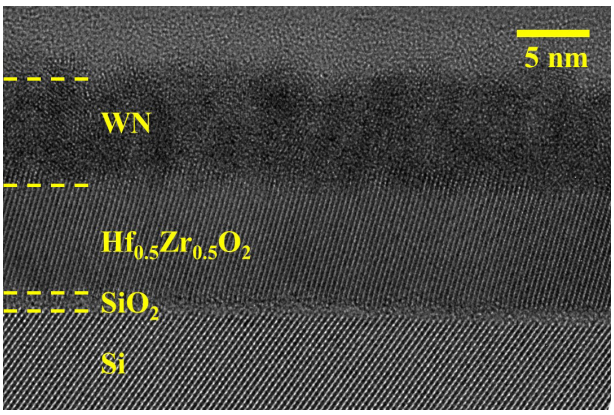
Polarization Switching in Highly Scaled Ferroelectric MOS Capacitor

A. Zubair, W. Chern, N. Rajput, K. Limanta, T. Palacios

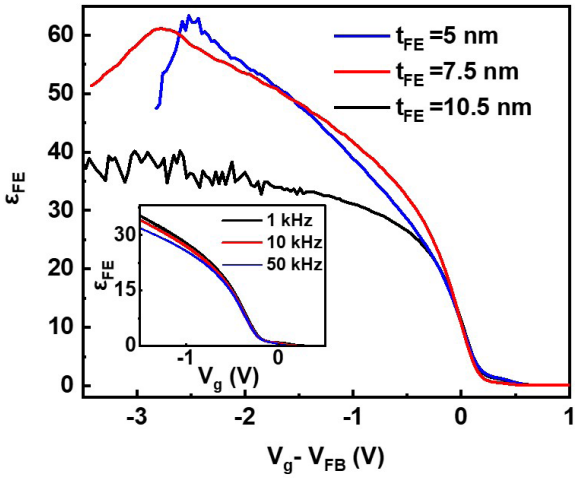
Ferroelectric FETs (FeFET) are promising candidates for low-power, scalable, and non-volatile memory-enabling applications such as in-memory computing, artificial intelligence (e.g., analog synapses, coupled oscillator networks, spiking neurons) and quantum computing (i.e., cryogenic memory). Ultra-thin doped HfO2 based thin-films have emerged as an attractive option for FeFETs due to precise thickness control through atomic layer deposition (ALD) and Complemnetary Metal Oxide Semiconductor(CMOS) compatibility. However, the design space of a FeFET-based memory that operates with a low supply voltage, a sufficient memory window, and high endurance is not well understood. In this work, we systematically investigate ferroelectric $Hfo_{.5}Zro_{.5}O_2$ MOS capacitors to study the electrostatics of the device, which solidifies the design criteria for low voltage FeFETs.

In this study, MOS capacitors (Figure 1) are fabricated on p-Si wafers using standard CMOS processing with different ferroelectric thicknesses. The dielectric constant, k, of the annealed $Hf_{0.5}Zr_{0.5}O_2$ film is higher than those of HfO_2 and ZrO_2(k = 25) for all thicknesses, as observed in the small signal capacitance-voltage (C-V) characteristics (Figure 2) due to the film's orthorhombic phase. At low gate biases, the HZO film is hysteresis-free (Figure 2 inset) and shows negligible frequency dispersion, indicating a high-quality interface. At high gate bias, the thinner films show rapid increase of the capacitance, resembling the peak of butterfly-like behavior of standard ferroelectric capacitors as the net charge exceeds the critical charge required to achieve the coercive field. However, this behavior is absent in the thick HZO film, where the coercive field is higher than the breakdown field. The high dielectric constant and relatively low effective charge of the ferroelectric thin film, in combination with the ultrathin SiO_2 interlayer, enables the polarization switching of the thinner dielectrics. This is the first observation of polarization switching ferroelectric MOS capacitors using small-signal measurement.

These results indicate that our technology can enable FeFETs operating at 2.5 V with highly scaled dielectrics (t_{FE} =5 nm) that are required for a future transistor topology. This is a significant improvement compared to state-of-the-art flash memory. However, to enable lower switching voltage FeFET, additional materials and device engineering would be required as the switching voltage weakly scales with ferroelectric thickness.



▲ Figure 1: Cross section transmission electron micrograph of fabricated MOS capacitor with 10Å amorphous interfacial SiO_2 deposited through ozone and crystalline $Hf0_{.5}Zr0_{.5}O_2$ (HZO), in this case 7.5 nm, capped with WN deposited by plasma-assisted ALD.



▲ Figure 2: Small-signal C-V characteristics of MOS capacitor with different ferroelectric layer thicknesses. Inset shows the frequency-dependent bi-directional C-V of 10.5-nm ferroelectric MOS capacitor for a low bias range.

First Demonstration of GaN Vertical Power FinFETs on Engineered Substrates

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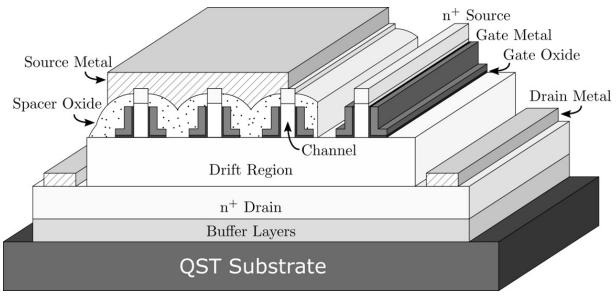
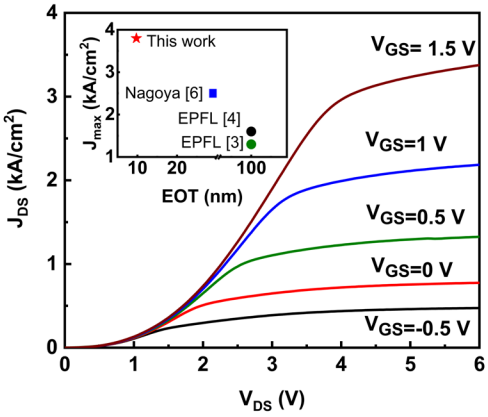
Sponsorship: Samsung Advanced Institute of Technology

GaN vertical power Fin Field Effect Transistors (FinFET) are promising high-voltage switches for the next generation of high-frequency power electronics applications. Thanks to a vertical fin channel, the device offers excellent electrostatic and threshold voltage control, eliminating the need for epitaxial regrowth or p-type doping, unlike other vertical GaN power transistors. Vertical GaN FinFETs with 1200 V breakdown voltage (BV), 5 A current rating and excellent switching figures of merit have been demonstrated recently on free-standing GaN substrates. Despite this promising performance, the commercialization of these devices has been limited by the high cost ($50-$100/cm2) and small (~ 2 inch) diameter of free-standing GaN substrates. The use of GaN-on-Si wafers could reduce the substrate cost by 1000; however, the growth of the thick (~10 µm or thicker) drift layers required for kV class applications is extremely challenging on Si. Alternatively, GaN grown on engineered substrates (QST®) with a matched thermal expansion coefficient could enable low-cost vertical GaN FinFETs with thick (>10 µm) drift layers and large wafer diameters (8-12 inch). In this work, we have demonstrated a quasi-vertical GaN FinFET on engineered QST® substrates for the first time.

A conformal oxide-based planarization and etch-back technology was used for gate etching and source-to-gate spacer etching. The device demonstrates a current density of JDS=3.8 kA/cm2 at VGS= 1.5 V and VDS= 4 V (Figure 2), and a maximum gm = 2 kS/cm2 at VDS= 4 V when normalized with respect to the total device area (fin width and spacing between fins), a record for vertical and quasi-vertical MOSFETs on non-GaN substrates. The current density in each fin is higher than 30 kA/cm2 at the same bias condition. The on-resistance is currently limited by non-ideal source contacts, as is evident in the Schottky-like behavior of the drain current at low VDS. The source contact resistance can be improved by either higher doping density or rapid thermal annealing of the metal stack after contact formation. The results are very promising for large wafer scale manufacturing and commercialization of vertical GaN power FinFETs.



▲ Figure 1: Schematic diagram of the quasi vertical Fin-FET on QST® substrate.



▲ Figure 2: Output characteristics of fabricated GaN power FinFET at different gate bias. Current is normalized to total active device area. Inset shows benchmarking of current work against state-of-the-art vertical GaN transistors on non-GaN substrate.

FURTHER READING

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