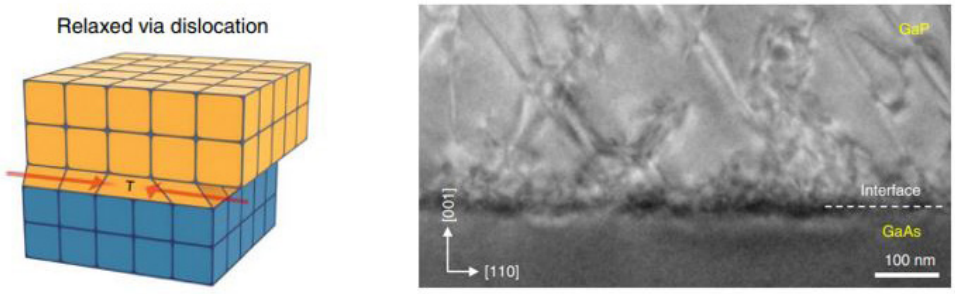
Nanotechnology, Nanostructure, Nanomaterials

Spontaneous Relaxation towards Dislocation-free Heteroepitaxy

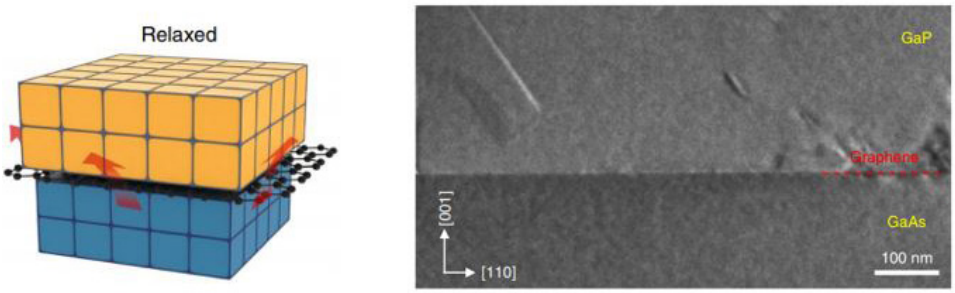
S.-H. Bae, K. Lu, S. Kim, K. Qiao, C. Choi, H. Kim, H. S. Kum, W. Kong, J. Shim, J. Kim
Sponsorship: DARPA

Epitaxy laid a foundation for conventional electronic systems as it produces high-quality single crystalline materials. To grow various materials through epitaxy, heteroepitaxy is required as a limited set of available substrates exists. However, a lattice-mismatched issue in heteroepitaxy leads to degradation in the materials' quality by introducing dislocations to release accumulated strain energy due to the lattice-mismatch. Here, we report a unique approach to release the accumulated strain energy in heteroepitaxy by coating graphene on substrates. As graphene provides a slippery nature on substrates, deposited particles are easily moved around to have energetically favorable atomic lattice. Thus, inserted graphene allows us to grow strain-free single-crystalline materials, a process named spontaneous relaxation. We expect this spontaneous relaxation will be useful to realize the monolithic integration of various lattice-mismatched systems.

Figure 1 shows a mechanism of strain relaxation in conventional epitaxy. GaP was grown on GaAs substrate that has 3.7 % misfit strain. Because of the lattice-mismatch, a substantial number of dislocations was introduced to release the accumulated strain energy above a critical strain level. This energy is known as a source to degrade the material's properties. On the other hand, Figure 2 shows a scenario of strain relaxation through spontaneous relaxation. GaP was grown on a graphene-coated GaAs substrate. As graphene has lattice transparency and provides a slippery surface on top of the substrates, strain-released GaP was obtained. These results demonstrate the feasibility of another strain relaxation pathway on graphene-coated substrates, which will broaden the materials set available for heteroepitaxy.



▲ Figure 1: Strain relaxation through introduction of dislocation.



▲ Figure 2: Strain relaxation through spontaneous relaxation.

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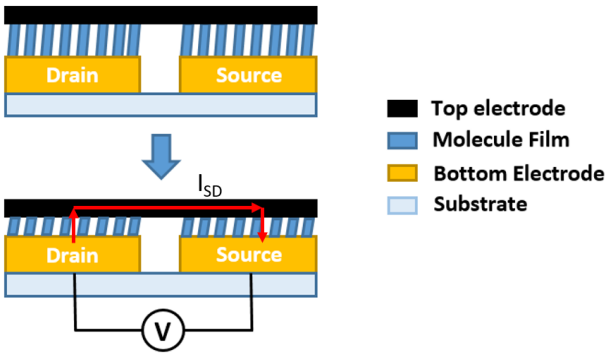
Graphene-based Tunneling Nanoelectromechanical Switch

M. Gao, F. Niroui, V. Bulovic, J. H. Lang
Sponsorship: NSF Center for Energy Efficient Electroics Sciences (E3S)

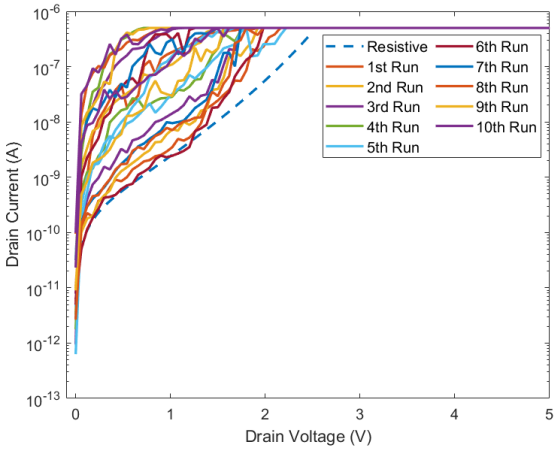
Nanoelectromechanical (NEM) switches are considered to be a promising complementary technology for conventional logic switches because of their zero static power consumption and potential for low-voltage operation. However, they can suffer from stiction caused by significant van der Waals forces acting on their nanoscale structures. Such stiction can easily lead to the permanent failure of a conventional NEM switch and generally prevents miniaturization, leading to a high actuation voltage. Therefore, for NEM switches to be competitive, it is necessary to develop a NEM switch with high switching reliability, low-voltage operation, and ultra-low power consumption. The fabrication of such a switch should also be scalable to enable its popularization within the digital integrated-circuit industry.

This work advances the development of a novel squeezable NEM switch, called a squitch. To fabricate the squitch as shown in Figure 1, a pair of nanometer-smooth gold electrodes are fabricated via electron beam lithography and transferred to a glass substrate. A monolayer of polyethylene glycol (PEG)-thiol is then deposited on electrodes via a self-assembly process. Finally, a single layer of graphene is patterned and transferred onto the bottom part of the squitch. Varying the voltage applied between the gold electrodes can electrostatically modulate the thickness of the compressible PEG-thiol monolayer, enabling an exponential change of the current tunneling through it.

At this point, as shown in Figure 2, an on/off current ratio of 100:1 with sub-1 V actuation has been achieved. The devices can also survive 10 to 100 cycles of operations, showing observable durability. The fabrication yield is up to ~ 40% and can be further improved by modifying the methods of transferring graphene and exploring new molecules with the appropriate mechanical properties. In the future, we plan to design a squitch based completely on graphene while keeping the current structure to avoid the potential effect of electromigration.



▲ Figure 1: Working principle of the squitch; in the off-state, the PEG-thiol layer is thick enough (~5nm) to prevent the tunneling current; applying voltage between the source and drain compresses the PEG-thiol layer, leading to the non-linear increase of the tunneling current.



▲ Figure 2: I-V Characteristics of a squitch over multiple testing cycles; the actuation voltage is estimated to be 1.3V.

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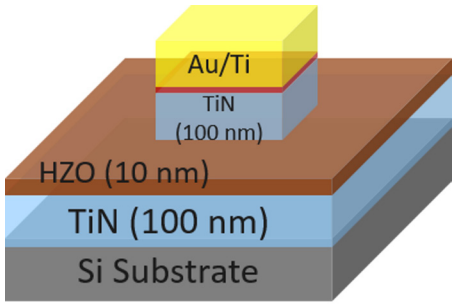
Low-temperature Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for InGaAs-channel Negative Capacitance Field-effect-transistors

T. Kim, D. A. Antoniadis, J. A. del Alamo
Sponsorship: Semiconductor Research Corporation, Samsung Electronics

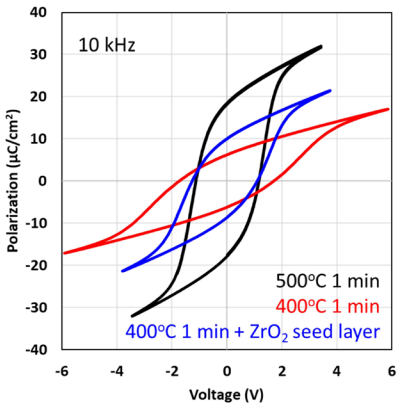
Negative capacitance (NC) MOSFETs by integrating ferroelectric (FE) hafnium zirconium oxide (HZO) film in the MOS gate stack have generated enormous interest due to its performance-boosting and CMOS process compatibility. Stable ferroelectricity in the HZO film is usually obtained after a rapid thermal annealing (RTA) step at 500°C. This is because film crystallization under the right conditions is crucial for the formation of the FE orthorhombic phase. However, in order to achieve NC InGaAs-channel MOSFETs, as is our goal, a low-temperature process is essential to preserve the integrity of the gate oxide/InGaAs channel interface. This is also needed for precise capacitance matching. In our work, we have focused our attention towards enabling a low thermal budget process for FE formation of HZO film.

After optimization of the HZO atomic layer deposition (ALD) process, Metal – FE – Metal (MFM) capacitors were fabricated to characterize the FE properties, as shown in Figure 1. To provide higher tensile stress and promote the formation of the orthorhombic phase in the HZO film during RTA, 100 nm-thick TiN as electrode was introduced. Figure 2 shows the polarization – voltage characteristics of MFM capacitors annealed at 500°C and 400°C. The result demonstrates that the HZO film attains FE properties with a 400°C thermal process. This is also confirmed by the strong FE switching current peaks observed in Figure 3.

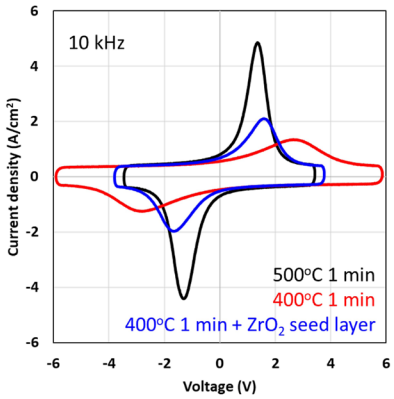
We are in addition exploring the further decrease of process temperature of HZO crystallization through the introduction of a ZrO_2 seed layer under the HZO film (Figures 2 and 3). This has been shown to boost orthorhombic phase formation. Going beyond, we have observed that HZO film deposited by plasma-enhanced ALD (PE-ALD) yields ferroelectric behavior with a 350°C thermal process. Our research will continue by integrating the optimized gate stack with our established InGaAs MOSFET platform for developing InGaAs NCFETs.



▲Figure 1: Schematic of MFM capacitor to characterize FE properties of HZO.



▲Figure 2: Polarization – voltage characteristics of HZO MFM capacitors annealed at 500°C (black), 400°C (red), and 400°C with ZrO2 seed layer (blue).



▲Figure 3: Current-voltage characteristics of the capacitors on the left, showing clear FE switching current peaks.

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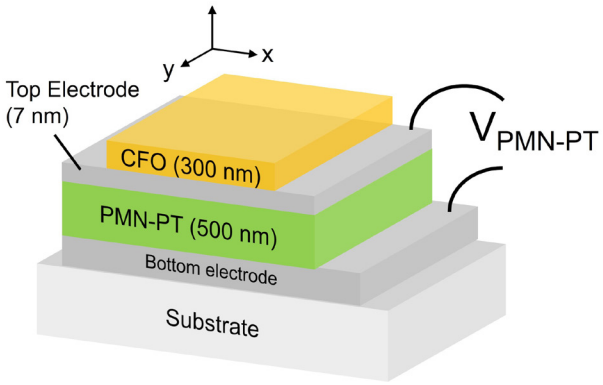
Artificial Heterostructuring of Single-crystalline Complex-oxide Membranes

H. S. Kum, W. Kong, K. Qiao, S.-H. Bae, J. Kim
Sponsorship: DARPA

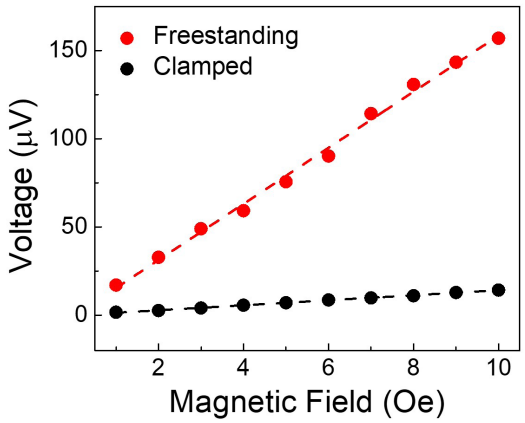
Epitaxial heterostructures are the backbone of many important electrical and photonic devices used today. Although many dissimilar crystals can be utilized, epitaxy is limited by the choice of substrates. In other words, the epitaxial film must be similar to the crystal structure of the host wafer. Such limitations impede the advancement of heterostructure engineering and prevent many novel physical phenomena from being discovered because they prevent epitaxial growth of dissimilar materials on a single substrate.

To overcome this limitation, we have developed a method to easily remove the epitaxial layer and transfer it onto any arbitrary substrate by using graphene as a release platform in a method called remote epitaxy. By extending this method to complex-oxide material systems, we have, for the first time, artificially created a complex-oxide membrane heterostructure by stacking piezoelectric PMN-PT and magnetostrictive $CoFe_2O_4$ (CFO) and hybridizing their properties. Both membranes were released from the substrates and were manually stacked by hand, with the PMN-PT membrane having a thickness of 500 nm and CFO having a thickness of 300 nm. The multiferroic heterostructure was fabricated into a device that allowed measurement of the voltage generated across the PMN-PT membrane (Figure 1).

The device was measured by applying a magnetic field across the entire heterostructure and measuring the resulting voltage generation across the PMN-PT membrane. In this device, the magnetic field strains the CFO membrane, and that strain is transferred to the PMN-PT, generating voltage (i.e., magnetoelectric coupling). We noticed that completely freestanding devices generated higher voltages by several factors than devices still clamped to the substrate (Figure 2). These results demonstrate the feasibility of creating novel heterostructures that have never been possible before using remote epitaxy and show the advantages of utilizing freestanding membranes as opposed to those still stuck on their substrates.



▲Figure 1: Schematic of an artificially created heterostructure consisting of single-crystalline magnetostrictive CoF_2O_4 and piezoelectric PMN-PT membranes exhibiting large magneto-electric coupling effect.



▲Figure 2: Voltage generation across the PMN-PT membrane shown in Figure 1 as a function of applied magnetic field across the CFO membrane. A large difference in voltage generation exists in totally freestanding films vs. devices clamped to the substrate.

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Morphological Stability of Nanometer-scale Single-crystal Metallic Interconnects

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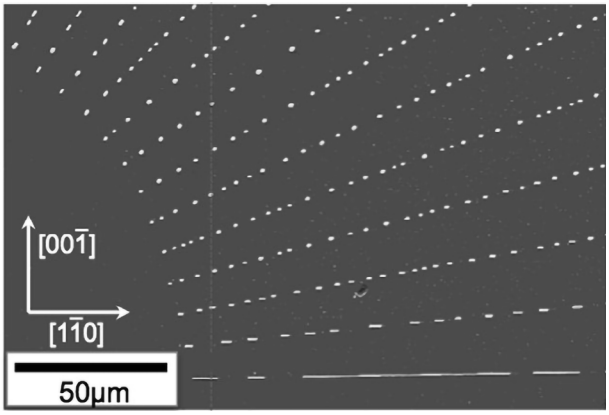
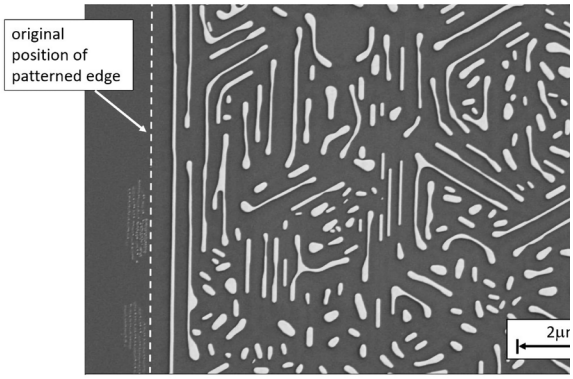
Sponsorship: Semiconductor Research Corporation, NSF

Continued IC scaling requires interconnects with cross-sectional dimensions in the <10nm range. At these dimensions the resistance of interconnects increases dramatically due to surface and grain boundary electron scattering. The reliability of interconnects with nanoscale dimensions is also expected to be compromised by reduced morphological stability. As a part of a collaborative program focused on ballistic conduction and morphological stability of single-crystal nanometer-scale interconnects, we are investigating the crystallographic dependence of the morphological stability of Ru wires.

Thin single-crystal films agglomerate into small particles via capillary driven surface diffusion in a process known as solid-state "dewetting." With decreasing film thickness, the temperature at which dewetting occurs is well below the constituent materials melting temperature. However, previous work on single-crystal (FCC) Ni films has demonstrated that crystalline anisotropy gives rise to special crystallographic orientations along which single-crystal wires are kinetically stable (Figure 1). Interconnects composed of such wires should have decreased vulnerability to morphological instabilities during processing and circuit operation. These wires will have strongly faceted surfaces which are predicted to reduce electron scattering and decrease interconnect resistance. Ru is a candidate material for future interconnects, and exploratory work with single-crystal (0001) films suggests that wires oriented along directions will be particularly stable (Figure 2). Work on patterning and testing of such wires is currently underway. In addition to this experimental work, we are working toward accurate simulations of anisotropic solid-state dewetting. These simulations reproduce the dramatic effect that stable surfaces can have on wire stability and provide an opportunity to systematically probe the effects of individual material properties. Combining the results of these experiments and simulations with those of past work on Ni will provide insights that will enable optimization of interconnect structural and crystallographic factors for design of morphologically stable nanowires with cross-sectional dimensions significantly below 10nm.



▲Figure 1: Lithographically patterned single-crystal lines of Ni on MgO demonstrating the enhanced stability of a wire aligned along a crystallographic directions with planar surface facets.



▲Figure 2: Stable wires spontaneously forming near edge of 10nm thick single-crystal Ru film with lithographically patterned edge aligned along stable direction.

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Modern Microprocessor Built from Complementary Carbon Nanotube Transistors

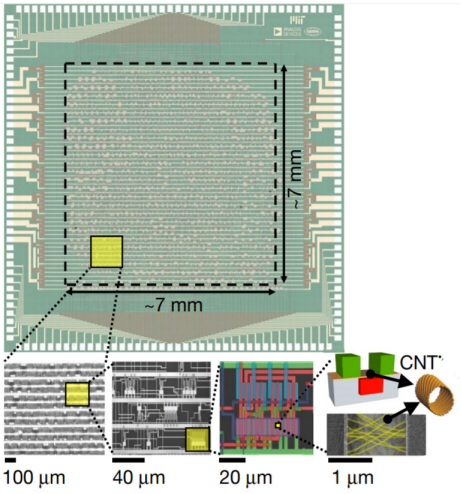
G. Hills, C. Lau, A. Wright, S. Fuller, M. D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, D. Murphy, Arvind, A. P. Chadrakasan, M. M. Shulaker
Sponsorship: Analog Devices, DARPA 3DSoC, NSF

Electronics is approaching a major paradigm shift because silicon transistor scaling no longer yields historical energy-efficiency benefits, spurring research towards beyond-silicon nano-technologies. In particular, carbon nanotube field-effect transistor (CNFET)-based digital circuits promise substantial energy-efficiency benefits, but the inability to perfectly control intrinsic nanoscale defects and variability in carbon nanotubes has precluded the realization of very-large-scale integrated systems. Here we overcome these challenges to demonstrate a beyond-silicon microprocessor built entirely from CNFETs: RV16X-NANO. This 16-bit micro-processor is based on the RISC-V instruction set, runs standard 32-bit instructions on 16-bit data and addresses, comprises more than 14,000 complementary metal–oxide–semiconductor CNFETs and is designed and fabricated using industry-standard design flows and processes. We propose a manufacturing methodology (MMC) for carbon nanotubes, a set of combined processing and design techniques for overcoming nanoscale imperfections at macroscopic scales across full wafer substrates. The key elements of MMC are:

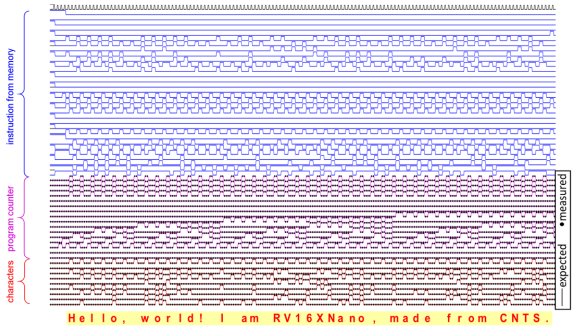
(1) RINSE (removal of incubated nanotubes through selective exfoliation). We propose a method of removing CNT aggregate defects through a selective mechanical exfoliation process. RINSE reduces CNT aggregate defect density by >250× without affecting non-aggregated CNTs or degrading CNFET performance.

(2) MIXED (metal interface engineering crossed with electrostatic doping). Our combined CNT doping process leverages both metal contact work function engineering as well as electrostatic doping to realize a robust wafer-scale CNFET CMOS process. We experimentally yield entire dies with >10,000 CNFET CMOS digital logic gates (2-input 'not-or' gates with functional yield 14,400/14,400, comprising 57,600 total CNFETs), and present a wafer-scale CNFET CMOS uniformity characterization across 150-mm wafers.

(3) DREAM (designing resiliency against metallic CNTs). This technique overcomes the presence of metallic CNTs entirely through circuit design. DREAM relaxes the requirement on metallic CNT purity by about 10,000× (relaxed from a semiconducting CNT purity requirement of 99.999999% to 99.99%),



▲Figure 1: Image of a fabricated RV16X-NANO chip. The die area is 6.912 mm × 6.912 mm, with in-put/output pads placed around the periphery. Scanning electron microscopy images with increasing magnification are shown below.



▲Figure 2: Experimentally measured waveform from RV16X-NANO, executing the 'Hello, World' program. The waveform shows the 32-bit instruction fetched from memory, the program counter stored in RV16X-NANO, as well as the character output from RV16X-NANO. Below the waveform, we convert the binary output (shown in red in hexadecimal code) to their ASCII characters.

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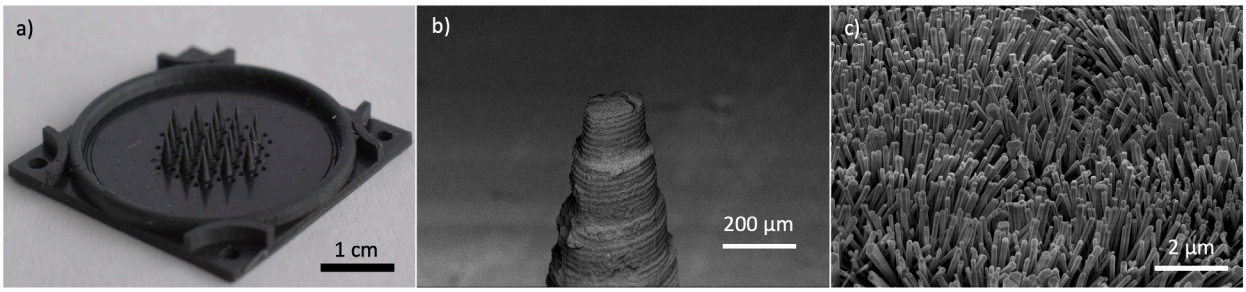
Nanostructured, Additively Manufactured, Miniature Ionic Liquid Ion Sources

D. V. Melo-Máximo, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

Electrospraying is a high-electric field physical phenomenon that transforms electrically conductive liquids into fine, uniform streams of micro/nanoparticles; the applications of electrospraying include mass spectrometry, nanosatellite propulsion, combustors, and agile manufacturing. Unfortunately, electrospray emitters have very low throughput; consequently, several research groups have investigated, for about two decades, greatly increasing the electrospray source's throughput via emitter multiplexing, using micro- and nanotechnology to attain lower startup voltage and denser emitter arrays. Although successful, the reported implementations harness cleanroom microfabrication, which has an associated high cost that is incompatible with many applications of electrospraying. In this project, we explore the use of additive manufacturing to create, at a very low cost, monolithic arrays of electrospray emitters capable of ion emission.

We have succeeded at demonstrating the first additively manufactured ionic liquid electrospray sources in the literature; our devices produce per-emitter current comparable to that produced by silicon microfabricated counterparts, at a small fraction of their fabrication cost. The devices are diodes composed of an emitting electrode and an extractor electrode: the emitting electrode is a monolithic array of digital light projection (DLP)-printed solid, conical, polymeric needles covered by a conformal layer of hydrothermally grown zinc oxide (ZnO) nanowires as a wicking material (Figure 1), while the extractor electrode is a laser-cut SS 316L plate with an array of apertures that matches the pattern of the array of needles. Characterization of the devices in vacuum using the ionic liquid EMI-BF_4 demonstrates bipolar, uniform array emission of solvated ions—in agreement with the literature on ionic liquid ion sources. Current research efforts focus on increasing the number of emitters per unit of area and on exploring other materials and designs for implementing the devices.



▲ Figure 1: Selected views of an additively manufactured electrospray source with 19 emitters in 1 cm^2 of active area: a) emitting electrode made in DLP-printable resin; b) close-up SEM image of one tip of the array, showing conformal growth of a ZnO nanowire forest; c) close-up SEM of ZnO nanowire forest (the material that transports the ionic liquid from the reservoir to the emission sites at the tips of the emitters), showing that the forest is composed of uniform, 150 nm-diameter nanowires.

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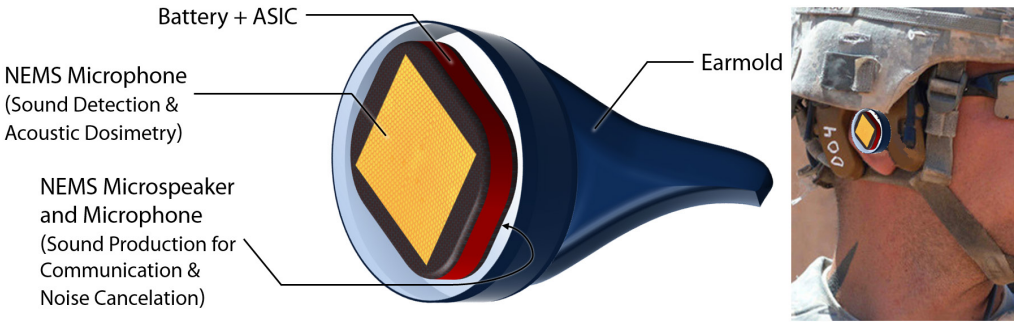
Soldiers' Hearing Health Protection and Auditory Augmentation Using Electrostatic NEMS

A. Murarka, J. H. Lang, V. Bulović
Sponsorship: ISN

Our work on acoustic nanomembrane electromechanical transducers (NEMS) that can safely fit and operate inside an ear is motivated by the desire to improve U.S. soldiers' auditory health. From the time soldiers set foot on training grounds to their deployment in war zones, they are consistently exposed to deleterious noise from rapid gunshots, friendly fire, explosions, jet engines, and armored personnel carriers. Noise levels from these sources often exceed safe hearing thresholds and can inflict irreversible ear trauma and hearing loss. Existing hearing protection solutions that attempt to mitigate tactical noise are often insufficient and compromise communication, combatant response time, and response accuracy. Indeed, it is recognized that hearing loss resulting from military service is a massive financial and clinical burden, which needs a technical solution that can protect soldiers and assist veteran civilians.

To simultaneously provide hearing protection, effective tactical communication, and situational awareness, an in-the-ear acoustic system is needed, one that can operate at low power with distortion-free acoustic output over the entire human auditory range. Scalable versions of such systems do not yet exist, which motivates us to suggest that the design of our electrostatic NEMS enables them to operate as ultra-low-power microspeakers. The low weight, the material composition, and the geometry of our NEMS membranes ensure linear and near-uniform acoustic output in the human auditory range. Hence, if integrated with earmolds, our NEMS could be used as high-fidelity microspeakers for speech enhancement in communication and noise attenuation. The same transducers can also act as acoustic dosimeters and as ambient-facing microphones for sensing acoustic signals. This composite reversible device is designed to attenuate harmful sounds while enhancing verbal communication and maintaining acoustic transparency with the surroundings. Leveraging our nanomembrane transducer technology, we aim to reach superior size, weight, and power consumption specifications, with no compromise in performance.



▲ Figure 1: Proposed tactical communication and hearing protection device that utilizes our electrostatic NEMS as reversible acoustic transducers for efficient, high-fidelity sound production and sound detection. A NEMS microspeaker, multiple microphones, a signal processing integrated circuit (ASIC), and batteries are integrated into a personalized earmold. This device would be capable of attenuating deleterious continuous and impulse noises while enhancing verbal communication and maintaining acoustic transparency with surroundings at safe levels.

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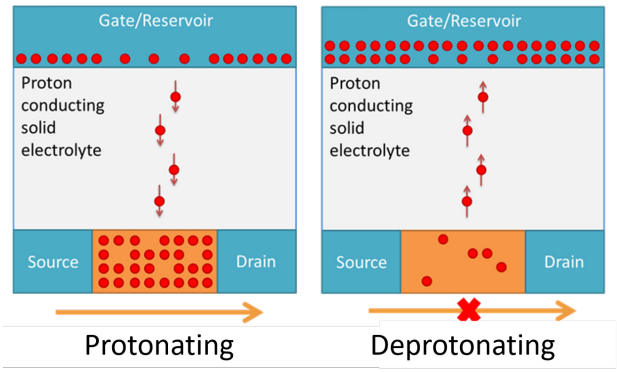
Proton-based Resistive Memory for Analog Computing Applications

M. Onen, X. Yao, W. Lu, S. Ryu, N. Emond, J. Li, B. Yildiz, J. A. del Alamo
Sponsorship: MIT-IBM Watson AI Lab

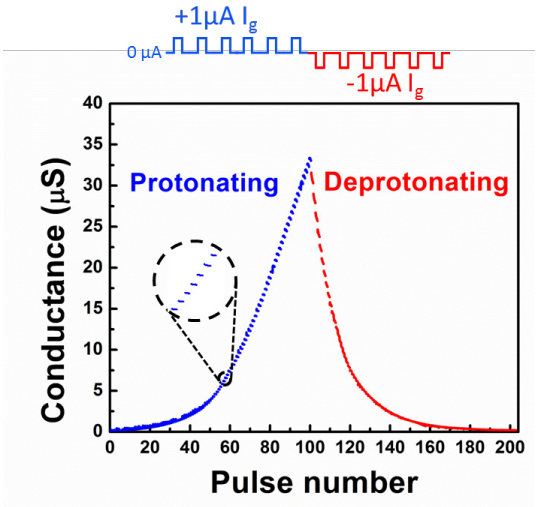
The size of state-of-the-art deep neural networks (DNNs) and consequent computation load have been increasing ever since the beginning of their outbreak. Since bigger and deeper neural networks trained with larger data sets generally provide better performance, this trend is expected to accelerate in the future. However, this poses as a significant problem for conventional digital architectures as the energy and time consumption for training DNNs have become unmanageable.

The idea of using analog resistive crossbars to do parallel vector-matrix multiplications based on Ohm's and Kirchhoff's Laws have been known since 1960s. It was recently discovered that rank-one outer product-based updates can also be performed in parallel using pulse-coincidence for multiplication and incremental conductance change of devices for accumulation. These advancements have fueled the investigation of various non-volatile analog resistive memory technologies to realize fast, energy-efficient and versatile platforms for deep learning.

In this work we implement a three-terminal electrochemical (i.e. battery-like) resistive memory device, employing the smallest ion, the proton. The conductance of the device is determined by the proton concentration intercalated inside the channel material. Electrical pulses applied to the gate enable protons to drift between the reservoir and the channel through the solid electrolyte as electrons move through the external circuit in the same direction (Fig. 1). When the gate is electrically open, proton movement through the electrolyte is forbidden since electrons cannot flow through the outside circuit, enabling non-volatile memory. We have demonstrated this concept on devices composed of a WO_3 channel, Nafion electrolyte and Pd as hydrogen reservoir (Fig. 2) Devices have very low energy consumption (18 aJ/(μm2 x nS), nearly symmetric modulation characteristics and long cycling lifetime. Future work will involve optimizing the material stack, scaling and integration of these devices ultimately realizing a full-scale DNN training accelerator



▲Figure 1: Working principle of the designed electrochemical device, with proton as the intercalation cation to tune the conductivity of the channel material.



▲Figure 2: Demonstration of reversible, multi-state conductance modulation by protonating/deprotonating a metal-oxide channel using identical current pulses.

FURTHER READING

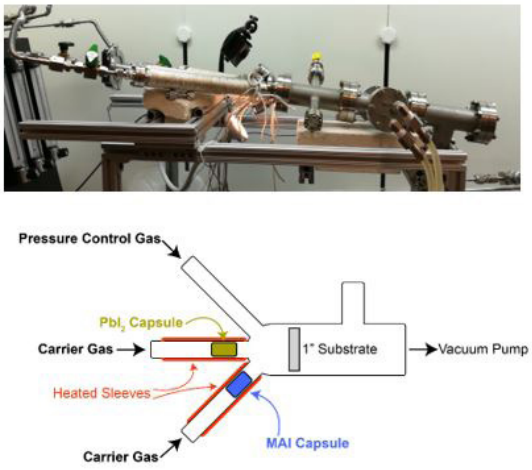
- X. Yao, K. Klyukin, W. Lu, M. Onen, S. Ryu, D. Kim, N. Emond, I. Waluyo, A. Hunt, J. A. del Alamo, J. Li, B. Yildiz, "Protonic Solid-state Electrochemical Synapse for Physical Neural Networks," under review.

High-throughput Vapor Transport Deposition of Organic-inorganic Perovskite Films

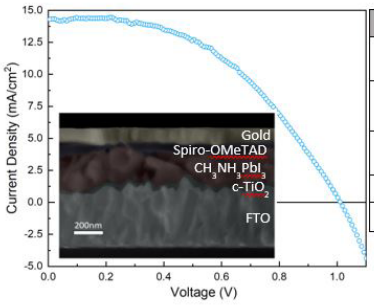
A. Panda,* E. Wassweiler,* Vladimir Bulović
(*Equal Contributors)
Sponsorship: Tata Trusts

Vapor transport deposition (VTD) is a promising technique for enabling high-throughput large-area deposition of next-generation perovskite solar cells. VTD uses a carrier gas to transfer sublimed salts from source to substrate, where they react to form perovskite films. Unlike vapor thermal evaporation, VTD decouples the material deposition rate from material temperature, allowing for high-throughput deposition. VTD allows independent control of chamber pressure and deposition rate, parameters which can be tuned to change the film crystallization kinetics. Like thermal evaporation, VTD permits precise control of thickness and eliminates hazardous solvents from device fabrication, allowing facile growth of complex multi-layer device structures such as tandem solar cells. The high throughput deposition coupled with low vacuum operation reduces the capex requirement for VTD deposition tools and has led to commercialization of the technique for CdTe and organic semiconductor materials manufacturing.

Through the use of a custom home-built VTD setup, we study perovskite solar cell active-layer film formation via co-evaporation of lead iodide and methylammonium iodide (MAI). We determined parameters and deposition conditions necessary to form high-quality methylammonium lead iodide films. We found that control of MAI degradation and its deposition rate during VTD is a critical challenge that must be overcome. Last, we developed numerical simulations of material diffusion and gas flow necessary to narrow the VTD design parameter space. We are assembling the next-generation VTD reactor to study the impact of critical parameters such as substrate temperature, carrier gas flow rate, chamber pressure, and deposition rate on film formation kinetics by examining metrics such as photoluminescence, x-ray diffraction, morphology, and device efficiency. We aim to demonstrate VTD to be a viable new deposition method for large-area high-throughput manufacturing of perovskite solar cells.



▲ Figure 1: Photograph of the first-generation VTD reactor and its schematic diagram with the labeled components.



Metric	Value
Power Conversion Efficiency (PCE)	6.9 %
Short Circuit Current (J_{sc})	14.2 mA/cm^2
Open Circuit Voltage (V_{oc})	1.01 V
Fill Factor (FF)	0.48
Device Area	0.15 cm^2

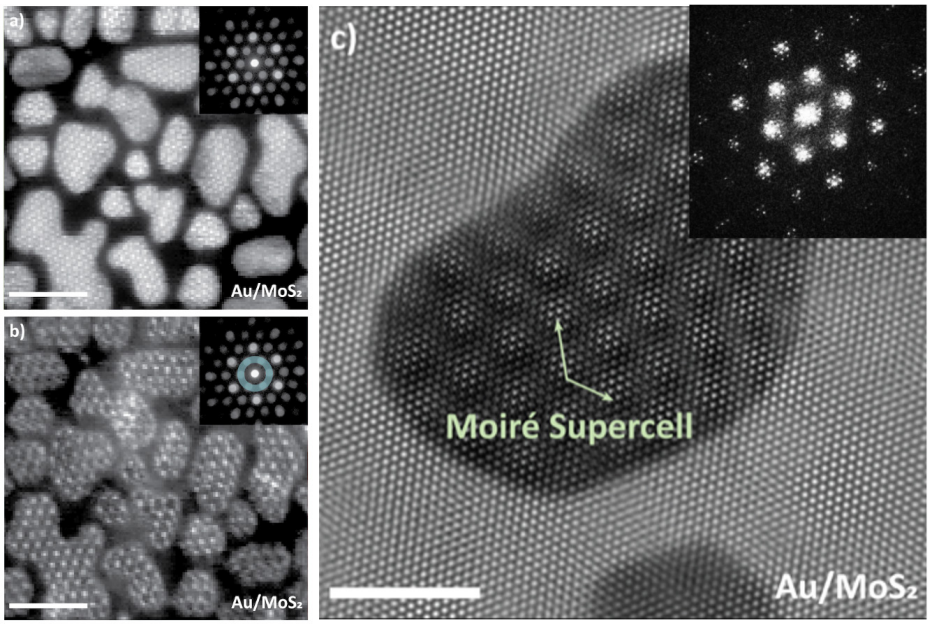
▲ Figure 2: Device structure, current density vs. voltage characteristic, and device parameters of champion device made with the first-generation VTD reactor.

Imaging Moiré Periodicities at the 2D/3D Interface Using 4D STEM

K. Reidy, G. Varnavides, J. D. Thomsen, A. Blackburn, J. M. LeBeau, F. M. Ross
Sponsorship: Thomas Lord Foundation

Structure and defects at the interface between 2D materials and their 3D bulk adjuncts greatly influence nanoscale device properties, such as contact resistance, photo-response, and high-frequency performance. Knowledge of fundamental charge transfer at this interface is critical for the continued and rapid development of devices that utilize 2D materials. Recent advances in scanning transmission electron microscopy (STEM), such as aberration correction and 4D STEM, allow analysis of interface growth, structure, and ordering. In this work, we use 4D STEM to directly image hidden moiré periodicities arising from epitaxial growth of nanoislands on 2D materials in ultra-high vacuum.

Epitaxial growth creates moiré patterns arising from rotation and lattice mismatch between the nanoisland and underlying 2D material substrate. We use 4D STEM to directly image these periodic superlattices, which are not visible in conventional TEM or STEM and often can result in strong electron correlations. DFT calculations show that this moiré is directly responsible for a periodic modulation of electronic structure in the 2D material. Our work illustrates the essential role of emerging microscopy techniques to unveil the mechanisms of moiré superlattices, and we explore the implications of these on physical properties at the 2D/3D interface, such as enhanced charge transfer and moiré-modulated local interactions.



▲Figure 1: 4D STEM image showing the a) bright 18-Å- period moiré and b) ADF 4D STEM image highlighting weaker 32-Å-period moiré. Scale bars 20 nm. Inset shows the 4D STEM DP, alongside the ADF annulus used to reconstruct image. c) Higher resolution TEM image showing moiré supercell of Au nanoisland on MoS_2 substrate as well as atomic lattice positions, with the moiré unit cell highlighted. Scale bar 5 nm. Inset: Fourier transform of image showing moiré peaks.

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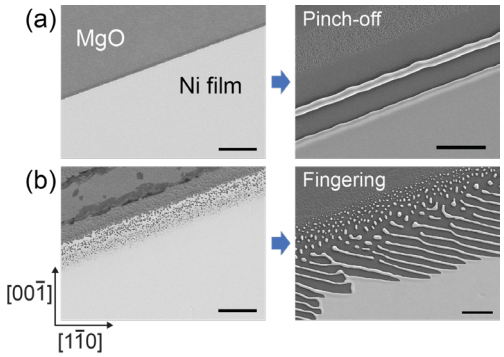
- K. Reidy, G. Varnavides, et al, "Forbidden Reflection Moiré Patterns in Metal-2D Material Interfaces," *Microscopy and Microanalysis*, 2020.
- P. Periwal, J. D. Thomsen, K. Reidy, et al, "Catalytically Mediated Epitaxy of 3D Semiconductors on van der Waals Substrate," *Appl. Phys. Rev.* (Submitted), 2020.
- J. D. Thomsen, K. Reidy, T. Pham, and F. M. Ross, "Nucleation and Growth of Metal Thin Films and Nanocrystals on Two-dimensional Materials," *Microscopy and Micoanalysis*, 2020.

Templated Solid-state Dewetting of Single-crystal Thin Films

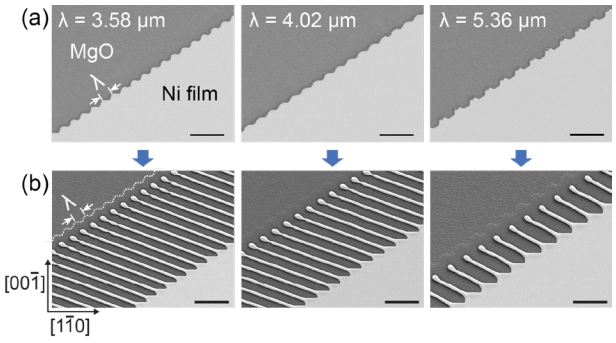
Y. A. Shin, M. L'Etoile, M. Dubrovsky, and C. V. Thompson
Sponsorship: NSF

Solid-state dewetting of single-crystal thin films leads to an ordered array of particles that align along a few specific crystallographic orientations due to crystalline anisotropy. When single-crystal thin films are pre-patterned and then subjected to dewetting, which is known as templated dewetting, a regular array of complex features can be fabricated. The features that result from templated dewetting are affected by various instabilities that develop at the retracting edges of pre-patterns and the characteristics they produce. One instability that retracting edges can develop is pinch-off (see Figure 1a), which leads a wire parallel to the retracting edge; this process can occur repeatedly to form multiple wires . Alternatively, retracting edges can be subject to fingering instability (see Figure 1b), which leads to an array of wires aligned along the finger propagation direction. Understanding and controlling whether pinch-off or fingering occurs is important for controlled pattern formation.

In the past year we have demonstrated that the initial roughness of a film edge determines whether pinch-off or fingering occurs, with rough edges leading to fingering (Figure 1). To further understand this phenomenon and to control it, we patterned large rectangular patches, with edges having controlled patterned roughness to template the fingering instability (Figure 2a). The edges of the patches were also aligned along various in-plane crystallographic orientations to study the effects of crystalline anisotropy on the templated fingering instability. We have found that templating of edge roughness can cause a fingering instability, with a very narrow distribution of the width and period of the fingers and wire, and that the wavelength of patterned roughness can control the steady-state finger period (Figure 2b). We further found that t the period of fingers affects the steady-state finger propagation velocity, so we developed a kinetic model that predicts steady-state finger propagation velocity as a function of the finger period. Strong effects of crystalline anisotropy on the templated fingering instability were observed. We found that edges that were aligned along a kinetically stable orientation resisted development of a fingering instability, even with the templating, and the patterned roughness disappeared as they retracted and became straight. Edges with orientations other than a kinetically stable orientation all developed fingering instabilities, but the finger propagation orientation was affected by the initial edge orientation; as a result, the steady-state finger period and propagation velocity were also affected. Furthermore, we studied effects of initial film thickness on the templated fingering instability using the same range of wavelengths of patterned roughness and the same range of in-plane orientations of the edge. During this study we found that the steady-state finger propagation velocity increases as film thickness decreases and that width of the wires that form due to propagation of the fingers decreases with film thickness, while the wavelength of patterned roughness still controls the finger period. Through these studies, we are developing techniques through which templated dewetting can be used as a patterning method.



▲ Figure 1: (a) Wire formed due to pinch-off during retraction of a well-defined straight edge (b) Wires formed due to a fingering instability during retraction of a rough edge. Scale: 10 μm



▲ Figure 2: Templated fingering instability (a) Edges having controlled patterned roughness (b) Controlled wire pattern formation through a templated fingering. Scale: 10 μm

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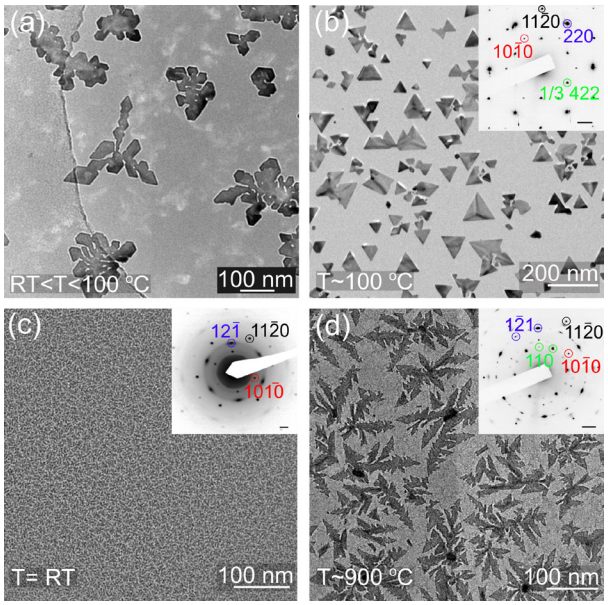
Nucleation and Growth of Metal Thin Films and Nanocrystals on Two-dimensional Materials

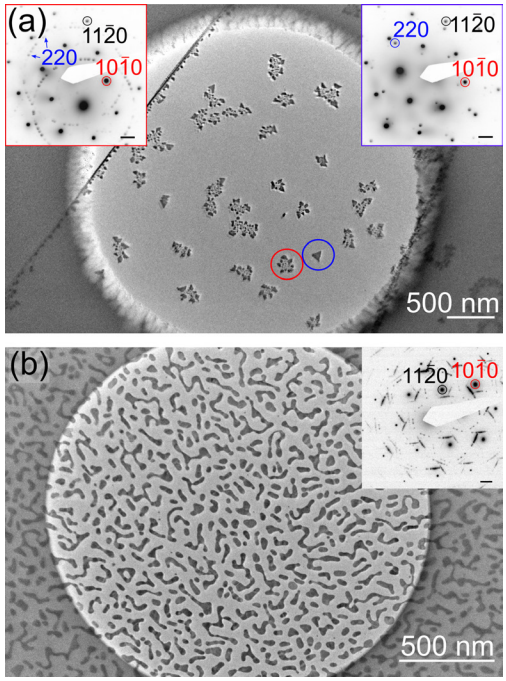
J. D. Thomsen, K. Reidy, T. Pham, F. M. Ross
Sponsorship: Independent Research Fund Denmark

The interface between metals and 2D materials (2DMs) influences device properties such as contact resistance, photoresponse, and high-frequency performance. In this project, we study the nucleation and growth of a variety of metals, including Ag, Au, Ti, Cr and Nb, on 2DMs (graphene, hexagonal boron nitride (hBN), WSe2, MoS2). We use transmission electron microscopy (TEM) to provide direct insight into crystal size, shape and orientation, epitaxy, and diffusivity. Besides the basic parameters that affect growth mode and epitaxy such as diffusivity, binding, and cohesive energies, we also explore the effects of 2DM thickness, temperature during deposition, and substrate (SiO2, hBN, or suspended). Combining the knowledge of deposition conditions, templating, and nucleation control greatly enhances routes towards tailored interface design for emerging 2DM device applications.

Temperature during deposition greatly affects the diffusivity of metal atoms on the 2D surface. As expected from crystal growth models, temperature determines whether the crystal morphology is dendritic or compact and faceted on 2DMs (Figure 1). The effect of the substrate on the epitaxy and crystal morphology is relatively unexplored, and we find suspended 2DMs exhibit the largest epitaxial alignment (Figure 2). This is seen even for relative thick 2DMs, suggesting that substrate effects such as surface charges play little role in the crystal growth. Rather, 2DM roughness may be a determining parameter, which is decidedly lower for suspended 2DMs. In suspended layers, we also find that diffusion distance depends on 2DM thickness, with longest diffusion distances (>2 μm) on suspended Gr >8 monolayers thick. This project aims to contribute to the emerging field of 2D material devices through atomic scale characterization of metal nanocrystal growth on 2DMs, facilitating the design of contacts, heterostructures, and coupled materials for future 2DM dimensional devices.



▲ Figure 1: (a, b) Au deposited on graphene at T ~ 50 °C and 100 °C, respectively. (c, d) Nb deposited on graphene at room temperature and 900 °C, respectively. Insets in (b, c, d) show diffraction patterns of the approximate regions in the main images, with scale bar 2 nm^{-1}.



▲ Figure 2: TEM images of Au deposited on (a) suspended hBN, and (b) hBN while the hBN was supported on a Si/SiO_2 substrate and subsequently transferred to a TEM sample carrier. Insets: diffraction patterns of the samples, scale bar 2 nm^{-1}.

FURTHER READING

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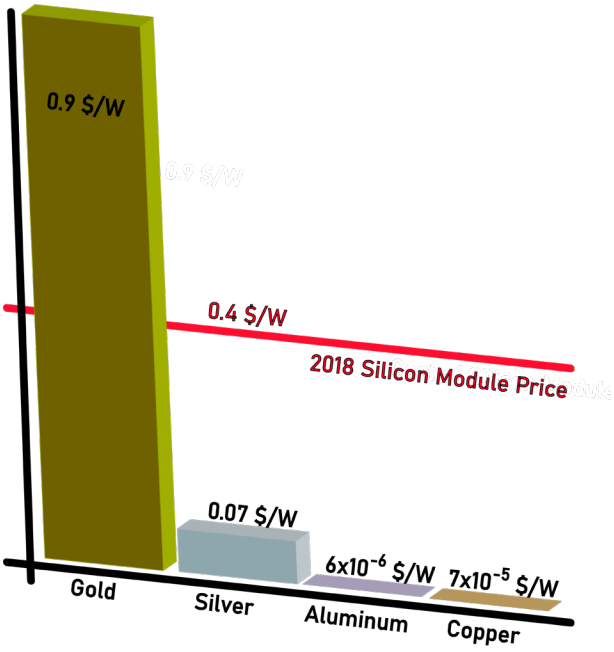
Enabling Low-cost Electrodes in PbS Solar Cells through a Nickel Oxide Buffer Layer

E. Wassweiler, M. Sponseller, J. Jean, A. Osherov, M. Bawendi, V. Bulović
Sponsorship: NSF GRFP, Tata-GridEdge Solar

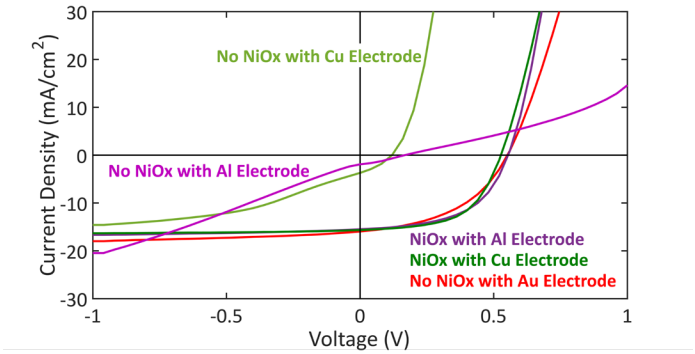
The versatile characteristics of lead sulfide quantum dots (PbS QD) make them an attractive material to develop high-efficiency, low-cost, and flexible photovoltaics (PVs). Hole transport layers (HTLs) and electron transport layers are essential building blocks in these solar cell architectures. PbS QDs with an EDT ligand are widely used as an HTL in high-efficiency QDPVs. However, the limited compatibility of the EDT with different electrode materials prevents the continued development of QDPVs into manufacturing capable device architectures. Specifically, the dependence on gold electrodes is cost-prohibitive for depositing QDPVs on a large scale.

While gold cannot be used on a commercial scale, less expensive but more chemically reactive materials can be used. Replacing gold with aluminum or copper would cut material costs by a factor of at least 1,200. Through the use of a nickel oxide (NiOx) buffer layer, these devices become compatible with lower-cost electrodes. As a p-type metal oxide, NiOx is a favorable HTL material with a high work function, large band gap, and film stability.

In fact, through the use of a NiOx buffer layer, power conversion efficiencies for devices with lower-cost electrodes are equivalent to their gold electrode counterparts. However, even though NiOx buffer layer devices show improved performance and stability compared to devices without NiOx buffer layers, the power conversion efficiency drops after a couple of months due to a new barrier within the device stack. Current research focuses on improving the stability of QDPVs with low cost electrodes through identifying and mitigating the barrier formation.



▲ Figure 1: Cost associated with different electrode materials.



▲ Figure 2: Comparison of JV curves between solar cells with gold and aluminum electrodes.

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