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I am happy to bring to you the 2018 Annual Research Report of the Microsystems Technology Laboratories. It highlights the research and educational activities of faculty, staff, students, postdocs, and visitors associated with MTL during MIT Fiscal Year 2018.

MTL is predicated on the notion that nanoscale science and technology can help solve some of the world’s greatest problems in areas of energy, communications, water, health, information, and transportation, among others. In this regard, MTL’s mission is to foster world-class research, education, and innovation at the nanoscale. In all these and other important areas of human concern, as showcased in this report, researchers at MIT are carrying out fundamental research and engineering in materials, structures, devices, and circuits and systems using MTL’s facilities and CAD services, in search of new solutions to persistent problems. MTL’s activities encompass integrated circuits, systems, electronic and photonic devices, MEMS, bio-MEMS, molecular devices, nanotechnology, sensors, and actuators, to name a few. MTL’s research program is highly interdisciplinary. MTL’s facilities are open to the entire MIT community and the outside world. Nearly 600 MIT students and postdocs from 23 different Departments, Laboratories, or Centers carried out their research in MTL’s facilities in the last fiscal year. In addition, researchers from several companies, as well as government research laboratories and domestic and international universities, use MTL’s facilities annually.

To accomplish its mission, MTL manages a set of experimental facilities in buildings 39 and 24 that host more than 150 fabrication and analytical tools. We strive to provide a flexible fabrication environment that is capable of long-flow integrated processes that yield complex devices while, at the same time, presenting low-barrier access to fast prototyping of structures and devices for users with very different levels of experience. Our fabrication capabilities include diffusion, lithography, deposition, etching, packaging, and many others. Our lab can handle substrates from small, odd-shaped pieces to 6-inch wafers. The range of materials continues to expand well beyond Si and Ge to include III-V compound semiconductors, nitride semiconductors, graphene and other 2D materials, polymers, glass, organics, and many others.

MTL also manages an information technology infrastructure that supports state-of-the-art computer-aided design (CAD) tools and process design kits for device, circuit, and system design. Together with a set of relationships with major semiconductor manufacturers, MTL makes available to its community some of the most advanced commercial integrated circuit fabrication processes available in the world today.

MTL could not accomplish its mission without the vision, commitment, and generosity of a number of companies that comprise the Microsystems Industrial Group (MIG). The MIG supports the operation of MTL’s facilities, and it also advises the faculty on research directions, trends, and industrial needs. The list of current MIG members can be found in the ‘Acknowledgments’ section of this report.

The research activities described in these pages would not be possible without the dedication and passion of the fabrication, IT, and administrative staff of MTL. Day in and day out, they strive to support MTL users in the pursuit of their dreams. They do this in a professional and unassuming manner. Their names do not usually end up in the research papers, but that does not diminish the significance of their contributions. To them and to all of you who support in your own way the activities of MTL, a most sincere thank you!

Jesús A. del Alamo
Director, Microsystems Technology Laboratories
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MEMS, Field Emitter, and Thermal Devices, and Structures

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A Four-terminal Nanoelectromechanical Switch Based on Compressible Self-assembled Molecules

J. Han, F. Niroui, J. Patil, T. M. Swager, J. H. Lang, V. Bulović
Sponsorship: NSF

Nanoelectromechanical (NEM) switches are under investigation as complements to, or substitutes for, CMOS switches owing to their intrinsic quasi-zero static leakage, large ON-OFF conductance ratio, and high robustness in harsh environments. For most NEM contact switches, a trade-off between high actuation voltage and the risk of stiction failure seems inevitable due to the strong van der Waals attraction between contacts at the nanoscale. This attraction leads to unfavorable dynamic power consumption and decreased reliability. Through this research, we have developed a novel tunneling NEM switch, termed a “squitch”, based on a metal-molecule-metal junction whose tunneling gap can be modulated by compressing the molecule layer with electrostatic force created by a voltage applied between the metal electrodes. In contrast to conventional NEM contact switches, direct contact of squitch electrodes in the ON state is avoided by assembling a molecular spacer between the electrodes; the molecular spacer acts to hold the squitch together and helps reduce hysteresis and the possibility of stiction failure.

A multi-terminal squitch has been demonstrated using a chemically-synthesized Au nanorod as a floating top electrode, and bottom Au electrodes patterned with electron beam lithography. With the help of a peeling technique that we have developed, Au electrodes are created with sub-nanometer roughness. The electrodes include two actuation gates recessed by several nanometers via a graphene sacrificial layer. By choosing molecules with appropriate chain lengths, we are able to define nanometer-wide electrode-to-nanorod gaps, which can be subsequently adjusted by a bias voltage applied between the gate electrodes. With a proper bias voltage, we can exponentially modulate the conduction current through a small variation of the gating voltage. Our squitch has been experimentally demonstrated to exhibit low actuation voltage and hysteresis, which supports its prospects in ultra-low power logic applications.
Cold cathodes based on silicon field emitter arrays (FEAs) have shown promising potential in a variety of applications requiring high current density electron sources. However, FEAs face a number of challenges that have prevented them from achieving widespread use in commercial and military applications. One problem limiting the reliability of FEAs is emitter tip burnout due to Joule heating. The current fabrication process for FEAs results in a non-uniform distribution of emitter tip radii. At a fixed voltage, emitters with a small radius emit a higher current while emitters with a large radius emit a lower current. Therefore, emitters with a small radius reach their thermal limit due to Joule heating at lower voltages and consequently burnout. Previous solutions to mitigating tip burnout have focused on limiting the emitter current with resistors, transistors, or nanowires in order to obtain more uniform emission current.

In this project, we focus on increasing the uniformity of emitter tip radii as a means to reduce tip burnout. Figure 1 shows a typical distribution of emitter tip radii for FEAs. The non-uniform distribution of emitter tip radii first forms during the photolithography step that defines the array of “dots” which become the etching mask for the silicon tips. In our FEA fabrication process, we use a tri-level resist process that nearly eliminates the light wave reflected at the photoresist/silicon interface, and hence improves the uniformity of the dot diameter. Furthermore, we integrate the emitter tips with silicon nanowires to improve their reliability. Figure 2 shows a diagram of the fabricated structure. We expect our fabrication process to result in FEAs with more uniform emission current and potentially longer lifetime.

FURTHER READING

Magnetrons are a highly efficient (>90%), high-power vacuum-based microwave source. In a magnetron, free-electrons in vacuum are subject to a magnetic field while moving past open metal cavities, resulting in resonant microwave radiation to be emitted. Current state-of-art magnetrons use a heated metal filament to thermonically emit electrons into vacuum continuously and are not addressable. This work seeks to replace the heated metal filament as a source of electrons with silicon field emitter arrays in order to improve the efficiency and increase the power, especially when several sources are combined. Silicon field emitter arrays, schematically shown in Figure 1, are devices that are normally off and are capable of high current densities plus spatial and temporal addressing. These arrays consist of many sharp tips made of silicon sitting on long silicon nanowires that limit the current of the electron emission. Electrons from the silicon tip tunnel into a vacuum as a result of the high electric field of the applied bias on the polysilicon gate. Pulsing the electric field applied on the gate can turn the arrays on and off. The proposed use of silicon field emitter arrays in a magnetron will allow injection locking and hence phase control of magnetrons. Phase-controlled magnetrons have multiple applications in areas where high-power microwave sources are desired. Currently, Si field emitter arrays have been designed for the magnetron and are undergoing testing with collaborators at Boise State University.

![Figure 1: (Left) 3-D rendering of Si device structure. For clarity, layers have been omitted in different regions of the rendering to show detail. In the front, the bare silicon nanowires [200-nm diameter & 10-μm height] with sharp tips. (Right) Top-view of a fabricated device with 350-nm gate aperture and 1-μm tip-to-tip spacing.](image)

**FURTHER READING**

Silicon Field Ionization Arrays Operating > 200 V for Deuterium Ionizers

G. Rughoobur, A. I. Akinwande
Sponsorship: DARPA

Devices that can field-ionize gas molecules at low bias voltages are essential for many applications such as ion mobility spectrometry and highly selective portable gas sensing. Field ionization consists of a valence electron of a gas atom or molecule tunneling through a potential barrier, commonly into a vacant energy state of the conduction band of a metal at the anode. Classic ion sources require extremely high positive electric fields, of the order of $10^8$ volts per centimeter. Such fields are only achievable in the vicinity of very sharp electrodes under a large bias. Ion sources based on microwave plasma generation have demonstrated high currents and high current densities. Yet, they are bulky and require large magnetic fields. Alternatively, single or arrays of gated tip structures have been used as field ionizers, but they emit low currents (~10 nA). Early tip burn-out due to non-uniform tip distribution and low voltage breakdown are the two main causes of such low currents.

In this work, Si field ionization arrays (FIAs) with a unique device architecture that uses a high-aspect-ratio (~50:1) silicon nanowire current limiter to regulate electron flow to each field emitter tip in the array is proposed. The nanowires are 10 μm in height, 1 μm apart and 100-200 nm in diameter. A dielectric matrix of ($\text{Si}_3\text{N}_4/\text{SiO}_2$) supports a poly-Si gate while a 3 μm thick dielectric holds the contacts. Current densities >100 A/cm² and lifetime > 100 hours have already been reported. The tip radius has a log-normal distribution varying from 2 to 8 nm with a mean of 5 nm and a standard deviation of 1.5 nm, while the gate aperture is ~350 nm. Field factors, $\beta > 1 \times 10^6$ cm⁻¹ can be achieved with these devices implying that voltages of 250-300 V (if not less) can produce $\text{D}^+$ ions based on the tip field of 25-30 V/nm. Completed chips on a package are shown in Figure 1 together with a schematic of the test set-up for field ionization.

Breakdown at the mesa edge at voltages ~70 V was the reported by Guerrera, et al. However this has now been overcome by etching a vertical sidewall profile (Figure 2) with a combination of both SF₆ and C₄F₈ flowing simultaneously (Figure 2). I-V characterization in air demonstrates breakdown occurs within the active region (Figure 2) possibly due to the narrow gate apertures and the short oxide thickness from the tip to the poly-Si gate. Initial results show that further etching this oxide to expose the nanowire increases the oxide separation to the gate, which in turns increases the breakdown voltage (Figure 2), thus enabling the Si FIAs to be operated at voltages exceeding 200 V.

FURTHER READING

Cold electron sources have been identified as alternatives to thermionic emitters due to their lower operating temperature, instant response to the applied electric field, and their exponential current-voltage characteristics. With the advent of microfabrication, the generation of high electric fields around sharp emitters to tunnel electrons was made possible. Scalable and high-density field emitter arrays (FEAs) based on Si are advantageous due to compatibility with CMOS processes, maturity of technology, and the ease to fabricate sharp tips using oxidation. The use of a current limiter is necessary to avoid burning of the sharper tips; active method using an integrated MOSFET, or passive methods using a nanopillar (~200 nm wide, 10 µm tall) in conjunction with the tip has been demonstrated. Si FEAs reported by Guerrera, et al., exhibited high current densities exceeding 100 A/cm² and having lifetimes of over 100 hours.

The need for another gate (Figure 1) becomes essential to control the focal spot size of the beam as the tips become blunt with time and as a consequence, the turn-on voltage also increases (Figure 2). With the focus electrode, stray electrons extracted by the gate closest to the tip will be captured and only electrons emitted within a certain cone angle will reach the anode, thus achieving a narrower focal spot size compared to a single gated Si FEA. The voltage on the focus gate can be varied with time to maintain a fixed focal spot size or even as an electron control switch. Indeed having a high positive focus voltage pulls all the extracted electrons and can be used to prevent electrons reaching the anode. This also offers the opportunity for fast switching of these Si FEAs, which has been a limitation thus far of these devices. In this work we are optimizing the process steps to fabricate Si FEAs with the two integrated gates and current limiter, to characterize the effects of the focus gate on electron emission. These devices will find applications in flat panel displays, nanofocused X-ray sources, microwave tubes, and triodes.

**FURTHER READING**

In field emission, electrons are ejected from a solid surface via quantum tunneling due to the presence of a high local electrostatic field. Compared to state-of-the-art thermionic electron sources, field emission cathodes consume significantly less power, are faster to switch, and could operate at higher pressure. Field emission cathodes have a wide range of applications such as X-ray sources, flat-panel displays, and electron microscopy.

Several materials, e.g., Si, ZnO, and graphene, have been explored as field emission sources; however, carbon nanotubes (CNTs) are very promising to implement field emission cathodes due to their high aspect ratio, high electrical conductivity, excellent mechanical, and chemical stability, and high current emission density. Reported approaches for fabricating CNT field emitters include screen printing and direct growth of nanostructures (e.g., plasma-enhanced chemical vapor deposition) where a static stencil, i.e., mask, is involved to produce patterned structures in specific locations. These masks increase the time and cost needed to iterate the pattern, affecting the prototype optimization of the cathode. Ink direct writing (IDW), i.e., the creation of imprints by extrusion of liquid suspensions through a small nozzle, has emerged as an attractive maskless patterning technique that can accommodate a great variety of materials to create freeform imprints at low-cost (Figure 1). An imprint with CNTs protruding from the surface of the imprint (Figure 2), strongly adhered to the substrate can achieve stably high-current emission when an electric field is applied. We are currently working on the design and optimization of the formulation of a CNT-based ink, to eventually demonstrate low-cost field emission sources.

**FURTHER READING**

Mass spectrometry is widely used to quantitatively determine the composition of samples. However, the bulky size and high-power consumption of conventional mass spectrometry instruments limit their portability and deployability. One of the key components of a mass spectrometer (MS) is the ionizer. State-of-the-art electron impact gas ionizers use a stream of electrons produced by a thermionic cathode to create ions by fragmentation. Field emission cathodes, based on quantum tunneling of electrons triggered by high electrostatic fields, are a better alternative for portable mass spectrometry of gases compared to mainstream thermionic cathodes because they consume significantly less power, are faster to switch, and could operate at higher pressure.

In this project, we are developing a compact electron impact gas ionizer based on a cleanroom-microfabricated cathode and a 3-D printed ionization housing (Figure 1). The cathode is an array of nano-sharp silicon field emitters with proximal, self-aligned extractor gate, while the ionization housing is composed of an ionization region surrounded by an ionization cage, an anode electrode, a repeller electrode, and a dielectric structure that holds together the electrodes. To produce ions (i) a high enough bias voltage is applied between the extractor gate and the silicon tips, shooting electrons into the ionization region, (ii) the anode electrode attracts the emitted electrons, forcing them to interact with the neutral gas molecules within the ionization region, (iii) the bias voltage of the ionization cage maximizes the ionization yield of the interaction between the electrons and the neutral gas molecules, and (iv) the repeller electrode pushes ions out of the ionization cage. Figure 2 shows an assembled ionizer. Current work is focused on characterization of the field emission cathode and gas ionizer at various conditions.

**Figure 1:** Schematic of electron impact gas ionizer with field emission cathode. The ions produced by the device are fed to the rest of the MS.

**Figure 2:** Picture of implemented gas ionizer. The field emitter array chip is mounted between two printed circuit boards.

**FURTHER READING**

A general rule of thumb for new semiconductor fabrication facilities (fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build, this rule serves as a significant barrier to entry for research and development and for groups seeking to commercialize new semiconductor devices aimed at smaller market segments and requiring a dedicated process. To eliminate this cost barrier, we are working to create a suite of tools that will process small (~1”) substrates and cumulatively cost less than $1 million. This suite of tools, known colloquially as the 1” Fab, offers many advantages over traditional fabs. By shrinking the size of the substrate, we trade high die throughputs for significant capital cost savings, as well as substantial savings in material usage and energy consumption. This substantial reduction in the capital cost will drastically increase the availability of semiconductor fabrication technology and enable experimentation, prototyping, and small-scale production to occur locally and economically.

Our research in the last few years has been primarily focused on developing and characterizing tools for the 1” Fab. In previous years, we demonstrated a deep reactive ion etching (DRIE) tool and a corresponding modular vacuum tool architecture, and we are now working to develop a reactive magnetron sputtering tool and an inductively coupled plasma-based PECVD tool (ICP-CVD) for depositing a wide variety of materials. The reactive magnetron sputtering tools operates using a 2” target and a direct sputtering configuration and is fully integrable with the modular tool architecture of the 1” Fab. We have demonstrated the functionality of the tool with the depositions of copper, aluminum, and via reactive sputtering, aluminum nitride. The system has been characterized using a response surface methodology and consistent, uniform depositions with <6% variation across the wafer have been shown. The ICP-CVD tool has also been built within the modular tool architecture and is being tested with depositions of SiO₂, SiNₓ, and a-Si. The use of an ICP source allows depositions to occur at temperatures as low as 25°C, with low hydrogen incorporation, and quality approaching that of LPCVD depositions. Film stress and index of refraction are also controllable.

Figure 1: (a) 1” Fab Sputtering Tool; (b) Aluminum RSM for sputtering tool; (c) 1” Fab ICP-CVD tool; (d) ICP-CVD SiO₂ film on 2” wafer.
Piezoelectric components have found applications in a variety of fields including energy harvesting, biological and chemical sensing, and telecommunications. The creation of piezoelectric thin films has made possible the implementation of exciting devices that operate at higher frequency (a consequence of the reduction of the thickness of the piezoelectric material) including highly sensitive gravimetric biosensors and acousto-fluidic actuators. However, traditional manufacturing methods for piezoelectrics require a high vacuum, show low deposition rates, involve expensive and complex equipment, and require additional microfabrication processes to achieve the required geometries via patterning and lithography.

Electrohydrodynamic deposition harnesses the electrospray phenomenon to create ultrathin imprints from liquid feedstock (Figure 1). When the electrospray emitter operates in the cone-jet mode, stable jetting of the liquid feedstock allows for the direct writing of structures, thus, eliminating the need for steps for material removal, e.g., mask transfer and etching (Figure 2). In addition, electrohydrodynamic deposition can operate at room temperature without the need for a vacuum and can be scaled-up via electrospray emitter multiplexing.

This project aims to produce piezoelectric thin films suitable for acoustic resonators and actuators via electrospray jetting of nanoparticle-doped liquid feedstock. Initial work revolved around the optimization of the deposition parameters and formulation of the liquid feedstock for the reduction of the printed line’s width and thickness, elimination of the “coffee ring” effect, and analysis of the crystallographic orientation of the films. Current work focuses on improving the film’s homogeneity, increasing the crystal orientation towards a highly oriented film, and its piezoelectric characterization and application as a sensor.

**FURTHER READING**

Enhancement and estimation of critical heat flux (CHF) are two of the most important research areas of pool boiling. It is well-known that microstructured surfaces can extend the limit of CHF up to ~250% higher than that of a flat surface. The mechanism for this enhancement has generally been accepted as the wickability of structured surfaces originating from liquid propagation within the surface structures driven by capillary pressure. We investigated the applicability of this theory based on the accumulated data of previous studies and our experimental data. We first calculated capillary pressure and permeability of structured surfaces to characterize liquid propagation rate analytically. We then performed pool boiling experiments on silicon micropillar surfaces to measure CHF values.

We found that there is no distinct relationship between the CHF and wickability contrary to a general notion. Our results suggest that although liquid wicking has been found to be important, the parameter wickability defined by previous works alone is not sufficient to describe CHF. In addition to the wickability, we propose that there may be other important parameters that also change along with the surface structures, e.g., the diameter of vapor columns and bubble departure size, among others, which need further investigation.

**FURTHER READING**

Vapor condensation is routinely used as an effective means of transferring heat or separating fluids. Filmwise condensation, where the condensate completely covers the condenser surface, is prevalent in typical industrial-scale systems. Dropwise condensation, where the condensate forms discrete liquid droplets, can improve heat transfer performance by an order of magnitude compared to filmwise condensation; however, current state-of-the-art dropwise technology relies on functional hydrophobic coatings, which are often not robust and therefore undesirable in industrial conditions. Furthermore, low surface tension condensates, like hydrocarbons, pose a unique challenge since coatings used to shed water often do not repel these fluids.

We demonstrated a method to enhance condensation heat transfer using gravitationally-driven flow through a porous metal wick, which takes advantage of the condensate’s affinity to wet the surface and also eliminates the need for condensate-phobic coatings. The condensate-filled wick has a lower thermal resistance than the fluid film observed during filmwise condensation, resulting in an improved heat transfer coefficient of up to an order of magnitude and comparable to that observed during dropwise condensation. The improved heat transfer realized by this design presents the opportunity for significant energy savings in natural gas processing, thermal management, heating and cooling, and power generation.

**FURTHER READING**

We developed omniphobic, doubly reentrant surfaces fabricated with a simple method suitable for use with traditional microfabrication processes. Intrinsic stresses in deposited layers of silicon nitride induced bending of a singly reentrant microstructure, creating the doubly reentrant geometry. Due to the use of standard microfabrication processes, this approach may be extended to a variety of materials and feature sizes, increasing the viability of applying omniphobic doubly reentrant structures for use in areas such as superomniphobicity, anti-corrosion, heat transfer enhancement, and drag reduction.

Figure 1 shows the fabrication process, in which standard photolithography and etches used to create singly reentrant microstructures are adopted. However, due to the stresses in deposited layers of silicon nitride, the singly reentrant structure is bent into a doubly reentrant geometry that renders the surface omniphobic. Figure 2 shows the contact angle of water and FC 40 on the surface. FC 40 has a much lower surface tension than water, which typically makes it difficult to repel. However, due to the double reentrant geometry of this surface, it is repelled.

FURTHER READING

Micro-engineered Pillar Structures for Pool Boiling Critical Heat Flux Enhancement

M. M. Rahman, C. Wang, J. Ge, M. Bucci, J. Buongiorno
Sponsorship: Exelon Corporation, MISTI

Increasing the performance of phase-change heat transfer phenomena is key to the development of next-generation electronics, as well as power generation systems and chemical processing components. Surface-engineering techniques could be successfully deployed to achieve this goal. For instance, by engineering micro/nano-scale features, such as pillars, on the boiling surface, it is possible to attain 100% enhancement in pool boiling critical heat flux (CHF). Researchers have been working on several CHF enhancing micro- and nano-structured surfaces for years. However, due to the complexity of CHF phenomena, there is still no general agreement on the enhancement mechanism. An investigation of the effect of micropillar height on surface capillary wicking and the associated pool boiling CHF enhancement has been conducted. Several 1 cm × 1 cm silicon micropillar surfaces with different micro-pillar heights have been fabricated using MTL’s photolithography and DRIE facilities.

The surfaces were characterized using MTL’s Scanning Electron Microscope (SEM), as shown in Figure 1a. The surfaces were then characterized by measuring the capillary wicking rate using high-speed imaging and a custom-built capillary tube approach as presented in Figure 1b. The capillary wicking experimental results are presented in Figure 1c is demonstrating the increase in liquid transport capability by increasing the micropillar heights.

Finally, the performances of such structures were characterized through traditional pool boiling experiments and compared with a flat silicon heater (Figure 1d). The surfaces were tested at atmospheric pressure and saturation temperature using DI water as the working fluid. The results demonstrate the benefits of wicking promoted by these structures in terms of CHF enhancement.

▲ Figure 1: Microstructured surfaces for CHF enhancement. (a) SEM image of a fabricated surface, (b) schematic of wicking experiment, (c) experimental wicking results, and (d) pool boiling result of microstructured surfaces compared to flat silicon reference surface.
Overheating presents a major challenge in modern electronics industry due to the increasingly higher power density. High temperatures not only limit device performance, but also greatly reduce reliability and lifetime. To effectively dissipate heat from an electronic chip, materials with high thermal conductivity \((k)\) are crucial. Common electronic materials such as copper and silicon exhibit a room temperature (RT) \(k\) of 401 \(\text{Wm}^{-1}\text{K}^{-1}\) and 148 \(\text{Wm}^{-1}\text{K}^{-1}\), respectively. In comparison, diamond holds the current \(k\) record of about 2000 \(\text{Wm}^{-1}\text{K}^{-1}\) at RT. However, natural diamond is scarce, and synthetic diamond still suffers from slow growth, low quality, and high cost. In addition, significant thermal stresses can arise from the large mismatch in the coefficient of thermal expansion between diamond and common semiconductors.

Recently, first-principles calculations predicted a very high RT \(k\) of about 1400 \(\text{Wm}^{-1}\text{K}^{-1}\) for cubic boron arsenide (BAs), rendering it a close competitor for diamond. Our materials collaborators from the University of Houston and UCLA have grown samples of different sizes and qualities. We carried out thermal transport measurement of these sub-millimeter to millimeter-sized samples using time-domain thermoreflectance (TDTR) (Figure 1), among other methods. In some samples, we have reached thermal conductivity as high as 1200 \(\text{Wm}^{-1}\text{K}^{-1}\).

We have also carried out the first-principles calculation of electron and hole mobility in boron-based III-V materials. We predict that BAs has both high electron (1400 cm\(^2\text{V}^{-1}\text{s}^{-1}\) at RT) and hole (2110 cm\(^2\text{V}^{-1}\text{s}^{-1}\) at RT) mobility (Figure 2). These characteristics, together with the high thermal conductivity, make BAs attractive for microelectronics applications both as device materials and as heat sink materials.

**FURTHER READING**

Nanotechnology, Nanostructures, Nanomaterials

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Experimental Characterization and Modeling of Templated Solid-state Dewetting of Thin Single-crystal Films .... 40
Directed self-assembly (DSA) of block copolymer (BCP) thin films is a promising approach to enable next-generation patterning at increasingly smaller length scales. DSA uses a combination of physical and chemical constraints to force the BCP domains to self-assemble with the desired orientation with respect to the substrate. Physical constraints, such as holes and trenches, are formed using conventional lithographic techniques. Chemical constraints, or wetting layers, are thin films that are either sandwiched between the BCP film/substrate interface or coated on top of the BCP film. These wetting layers ensure the pattern formed upon self-assembly has the appropriate orientation with respect to the substrate. Controllable chemistry combined with facile processing is key to the integration of these wetting layers.

Here, we demonstrate that initiated chemical vapor deposited (iCVD) polydivinylbenzene (pDVB) ultra-thin films can direct the self-assembly of poly(styrene-block-methylmethacrylate) (PS-b-PMMA). iCVD allows for the simultaneous synthesis and formation of polymer thin films via a surface free radical polymerization. Additionally, methyl radicals formed at increased filament temperatures can change the chemical structure of the growing pDVB film in situ. By tuning the degree of backbone methylation, we systematically changed the wetting properties of iCVD pDVB from weakly PMMA preferential to complete PS preference. Conformal coatings of weakly preferential iCVD pDVB films on topographical line and space patterns produced self-assembled BCP films with both perpendicular orientation and long-range alignment (Figure 1a and 1b). Current research efforts aim to use iCVD pDVB films to enable contact hole shrinkage. To minimize the diameter of the template hole, the BCP should assemble with a central, cylindrical PMMA domain. Preliminary experiments examined the effects of strongly PS-preferential, conformal iCVD pDVB films on a contact hole shrink template. The dark spot within each hole in Figure 1c corresponds to the PMMA domain. These results indicate that iCVD pDVB films are a viable method to enable contact-hole shrinkage.

**Figure 1**: (a) SEM image line and space template conformally coated with iCVD pDVB. Green highlight is trench template. Orange highlight is pDVB film. Orange dots highlight interface between pDVB film and template. (b) SEM image of self-assembled PS-b-PMMA inside line and space template coated with iCVD pDVB. Inset shows PS domains highlighted in red and PMMA domains highlighted in blue. (c) pDVB coated hole shrink template (ø = 65 nm) with self-assembled PS-b-PMMA inside holes. Red arrow indicates PMMA domain (central dark spot).

**FURTHER READING**

Directed self-assembly of block copolymers can generate complex and well-ordered nanoscale patterns for lithography. Previously, self-consistent field theory has been commonly used to model and predict the block copolymer morphology resulting from a given template. In this work, we map block copolymer self-assembly onto an Ising model using a two-dimensional post lattice template. We describe a simple and fast Ising-model-based simulation method for block copolymer self-assembly. With the Ising lattice setup, we demonstrate Ising-model-based logic gates.

Figure 1 shows a diagram of the Ising lattice setup. To define the Ising lattice, we used a post lattice template with horizontal and vertical pitch equal to the equilibrium block copolymer periodicity, $L_0$. After block copolymer processing, we defined a binary state, +1 or −1, between each adjacent pair of posts. We assigned +1 to a state when two adjacent posts were connected by a block copolymer structure, and −1 otherwise. The Ising Hamiltonian is given by

$$H(\sigma) = -J \sum_{\langle i,j \rangle} \sigma_i \sigma_j - h \sum_{i} \sigma_i$$

where $J$'s and $h$'s were assumed to be independent of lattice location. We calculated the minimum Hamiltonian configuration using simulated annealing and compared the simulation results with previously reported results.

To perform Ising-model-based computation, we encoded Boolean operations into the ground states of Ising lattices by designing specific Hamiltonians. Figure 2 shows a template design for a buffer where a boundary was defined by incommensurate double posts. Inside the boundary, an input state and an output state were defined. Prior to block copolymer processing, the input state was determined by the orientation of double posts while the output state was undetermined. After block self-assembly, the output state was set equal to the input state, performing the buffer operation.

FURTHER READING
The programmability of DNA makes it an attractive structure-directing ligand for the assembly of nanoparticle superlattices that mimic atomic crystallization. However, synthesizing multilayer single-crystals of defined size remains a challenge. This work studies growth temperature and interfacial energetics to achieve epitaxial growth of single crystalline nanoparticle thin films over arbitrarily shaped 500 × 500 μm² areas on lithographically patterned templates. Both surface morphology and internal structure are examined to provide an understanding of particle attachment and reorganization (Figure 1).

Importantly, these superlattices utilize a “soft,” elastically malleable building block, resulting in significant strain tolerance when subjected to lattice mismatch. Calculations of interaction potentials, small-angle X-ray scattering data, and electron microscopy images show that the oligomer corona surrounding a particle core can deform to store seven times more elastic strain than atomic films. DNA-nanoparticles dissipate strain both elastically through coherent relaxation of mismatched lattice parameter and plastically (irreversibly) through formation of dislocations or vacancies (Figure 2). Additionally, the DNA cannot be extended as readily as compressed, and thus, the thin films exhibit distinctly different relaxation behavior in the positive and negative mismatch regimes. These observations provide a more general understanding of utilizing rigid building blocks coated with soft compressible polymeric materials to control nano- and microstructure through “soft heteroepitaxy.”

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**Figure 1:** Scanning electron microscopy (SEM) and small-angle X-ray scattering (SAXS) of a 10-layer DNA-nanoparticle thin film revealing near perfect, epitaxial alignment with the lithographically defined template. Scale bar is 500 nm.

**Figure 2:** SEM of cross-section following focused-ion-beam (FIB) milling of a DNA-nanoparticle thin film under negative lattice mismatch with respect to patterned lattice parameter exhibiting plastic strain dissipation through formation of a misfit dislocation.

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**FURTHER READING**

Patterning of superconducting thin films at the nanoscale has enabled numerous technologies used in signal detection and digital circuits. For instance, superconducting nanowire single photon detectors (SNSPDs) and, more recently, the nanocryotron (nTron) both make use of the ability to pattern niobium nitride films at dimensions < 100 nm. Electron beam lithography of these devices often employs the negative tone resist hydrogen silsesquioxane (HSQ) due to its high resolution and superior line edge roughness. Development of HSQ and adhesion promotion of HSQ to the substrate surface are both facilitated by tetramethylammonium hydroxide (TMAH), making it an integral chemical in the fabrication process. However, despite the prevalent use of TMAH in patterning superconducting films, its influence on the film itself has yet to be fully studied.

Here we have investigated the effects of exposing NbN thin films to 25% TMAH. We show that TMAH modifies the surface chemistry of the film by reacting with the NbN to form niobium-based clusters, which are visible by scanning electron micrograph inspection (Figure 1). In addition to thinning the overall NbN film and reducing its critical temperature, the formation of niobium clusters creates a barrier to reactive ion etching in CF₄, threatening the lithographic pattern transfer (Figure 2). While characterization such as FTIR has been employed to identify the compounds created by this reaction, future work is needed to study the mechanism through which the hexaniobate species interfere with the reactive ion etch chemistry.

**FURTHER READING**


▲ Figure 1: Effect of TMAH on the surface of NbN. SEMs reveal the difference in surface features between an NbN structure that has been submerged in 25% TMAH (top) and one that has been untreated (bottom).

▲ Figure 2: Impact of TMAH on the reactive ion etching of NbN. Plot shows the sheet conductance versus development time in 25% TMAH. Conductances were measured after 2.5 min and 3.5 min of reactive ion etching (RIE) in CF₄. Samples were rinsed in DI water for either 30 s (the standard process) or vigorously for 3 min. The data suggest that vigorous washing leads to roughly the same etch barrier thickness for each of the developed samples; however, the remaining NbN film thickness depends on the total time it has been developed. As a result, the resistance follows a directly proportional relationship with development time, since longer exposure to TMAH reduces the film thickness and increases the sheet resistance.
Semi-additive electro-chemical plating (ECP) is a common process for fabricating copper interconnects in many advanced packaging technologies, such as Wafer Level Integrated Fan Out (InFO) packaging. While cost efficient, this process suffers from thickness variations in the height of the plated copper. The most significant of these variations are layout dependent, where areas with dense interconnects plate slower than sparse areas (Figure 1). If left unchecked, these variations can lead to significant complications in later stages of the fabrication process, and ultimately to decreased electrical performance of the final packaged device. Previously, there were limited methods for predicting these variations, and foundries had to rely on experimentally determining which layouts would perform acceptably. Recently, we have developed a model that predicts these variations and allows errors to be predicted and corrected without the need to first fabricate the layout in question.

While a model based on fundamental physics could in principle be developed to predict these variations, we instead develop an empirical model based on experimental data. This approach is well suited for many industrial applications, as empirical models can often be developed more quickly, without a significant loss of accuracy, and can be rapidly tuned or adapted to accommodate effects whose causes are uncertain. Our ECP model is divided into four stages as summarized in Figure 2. First, the effective pattern density of each point on the layout is determined with a learned spatial filter. These pattern densities are then mapped to effective conductances using a ratio-of-polynomials approximation. Next, these conductances are masked with the original layout, as photoresist prevents copper from growing in unwanted areas. Finally, the current flowing through each point of the wafer is solved for, and these currents are then converted to the plating height at each point in the layout.

FURTHER READING

Additive Manufacturing of High-temperature Compatible Magnetic Actuators

A. P. Taylor, L. F. Velásquez-García
Sponsorship: Edwards Vacuum

Various MEMS devices require large displacement and large force actuation to be efficient, such as miniature pumps. Magnetic actuation delivers large displacement and large force in a compact form factor. Additive manufacturing has recently been explored as a processing toolbox for MEMS; researchers have reported additively manufactured microsystems with performance on par or better than counterparts made with standard microfabrication. In this work, miniature actuators are printed in pure Nylon 12 using the fused filament fabrication method where a thermoplastic filament is extruded from a hot nozzle to create layer by layer a solid object. The actuators have embedded magnets that are not demagnetized by the heated nozzle (@ 250 °C) while being sealed in place midstream in the printing process.

We have demonstrated the first miniature, additively manufactured, monolithic magnetic actuators compatible with high temperature (>200 °C) operation (Figure 1). The displacement of a 150 μm-thick, single-layer membrane actuator is characterized by various DC coil bias voltages, resulting in a maximum membrane displacement of 302 μm with 20V DC applied to the driving coil; in addition, the magnetic force is proportional to the square of the current drawn by the coil as expected from theory (Figure 2).

FURTHER READING


▲ Figure 1: (a) Cross-section of magnetic actuator with additively manufactured Nylon 12 body, embedded SmCo magnet, and off-the-shelf driving coil. (b) Photograph of a single-layer, 150 μm-thick membrane actuator while being tested (left) and close-up of the membrane showing the striations due to the rastering of the nozzle (right).

▲ Figure 2: (a) Membrane displacement vs. radial position from the edge for various DC bias coil voltages for an actuator with a 150 μm-thick single-layer membrane. The membrane sags at 0V due to the weight of the magnet. (b) Magnetic force acting on the SmCo magnet versus the square of the current drawn by the driving coil.
Electrospray-deposition (ESD) has recently gained attention as a manufacturing technology to develop novel nanomaterials composites to produce low-cost micro- and nano-devices. ESD is also a remarkably versatile printing technique due to its capability to create ultrathin films made from a great variety of liquid feedstock (e.g., suspensions of polymeric, dielectric, metallic particles) that can be doped with organic nanostructures to modulate the physical properties of the imprint. Notably, the resulting nanoreinforced composites might show enhanced transduction, which, in combination with printing on flexible substrates, might be relevant for exciting applications such as wearable biomedical devices.

This project aims to develop an additively manufactured, low-cost, flexible physical sensor based on an ultrathin nanocomposite film doped with functionalized carbon nanostructures. The Taylor cone on an electrospray emitter fed with nanocomposite feedstock is shown in Figure 1a, while an electrospray-deposited imprint on a substrate is shown in Figure 1b. Essentially, this project is divided into (i) down-selecting and optimizing the formulation of the liquid feedstock, (ii) optimizing the fabrication of the ultrathin (~100 nm) nanostructured composite, and (iii) demonstrating a flexible physical sensor with transducing component made of the optimized nanostructured composite (see Figure 2).

**Figure 1:** a) Taylor cone of nanocomposite solution (needle has 300 µm outer diameter). b) 150X scanning electron microscope image of a line of electrospray-deposited ultrathin nanocomposite film.

**Figure 2:** Schematic of flexible physical sensor.

**FURTHER READING**

Atmospheric Microplasma Sputter Deposition of Interconnects

Y. Kornbluth, R. Mathews, L. Parameswaran, L. M. Racz, L. F. Velásquez-García
Sponsorship: MIT Lincoln Laboratory

We have preliminarily developed an apparatus that allows for the continuous, direct writing of interconnect-quality conductive lines. An atmospheric-pressure microplasma obviates the need for a vacuum while allowing for fine resolution imprints. We tested and characterized a novel focusing mechanism in which collisions with the working gas are harnessed to transfer electrostatic force to neutral sputtered atoms. This method compresses the deposit’s width in one dimension while expanding its length in the perpendicular dimension. We find that for an ideal set of parameters, the imprint is narrower than the sacrificial sputtering target (i.e., 9 µm wide imprint from a 50 µm diameter target). Other sets of parameters lead to other results, as computer simulation predicted, ranging from an unfocused spot 400 µm in diameter to a narrow line with 20:1 compression in the direction of focus, i.e., width, and 20:1 expansion in length (Figure 1), as compared to the unfocused spot.

The microstructure of the deposit is of particular interest. As is typical of sputterers, the deposit could be smooth (55 nm roughness), and the resistivity can be as low as 1.1 µΩ·m (with no annealing). However, the resistivity greatly depends on the microstructure, which in turn depends on the deposition conditions. It is well known that sputtering at high-pressure results in a grain structure, as the early deposits shadow parts of the bare substrate, keeping sputtered material from fully coating the substrate. Traditionally, vacuum sputtering prevents this problem by allowing the sputtered material to impact the substrate normal to the surface; however, we sputter at atmospheric pressure, and thus, the sputtered material is redirected by random collisions. In our case, we use a combination of directed gas flow and electrostatic forces to prevent this shadowing effect (Figure 2).

![Figure 1: Height profiles of (a) partially focused and (b) well-focused deposits. The well-focused deposit is cracked, an artifact of the microscopy extends the crack into the substrate.](image1)

![Figure 2: SEM micrographs of deposits (a) without gas flow, (b) with gas flow but no electrostatic attraction, (c) with gas flow and electrostatic attraction, and (d) with gas flow and larger electrostatic attraction. Note how the microstructure improves from (a) to (c), and in (d), there is too much attraction for proper deposition.](image2)

**FURTHER READING**

Materials comprising carbon nanotubes (CNTs), such as hierarchical nanoengineered advanced composites for aerospace applications, are promising new materials thanks to their mechanical and multifunctional properties. We have undertaken a significant experimentally based program to understand both microstructures of aligned-CNT nanocomposites and hierarchical nanoengineered advanced composites macrostructures hybridized with aligned CNTs.

Aligned nanocomposites are fabricated by mechanical densification and polymer wetting of aligned CNT forests. Here the polymer is typically an unmodified aerospace-grade epoxy. CNT forests are grown to mm-heights on 1-cm² Si substrates using a modified chemical vapor deposition process. Following growth, the forests are released from the substrate and can be handled and infiltrated. The volume fraction of the as-grown CNT forests is about 1%; however, the distance between the CNTs (and thus, the volume fraction of the forest) can be varied by applying a compressive force along the two axes of the plane of the forest to give volume fractions of CNTs exceeding 20% (see Figure 1a). Variable-volume fraction-aligned CNT nanocomposites were characterized using optical, scanning electron (SEM), transmission electron (TEM) microscopy, 3-D TEM, and X-ray computed tomography (CT) to analyze dispersion and alignment of CNTs as well as overall morphology. Extensive mechanical property testing and modeling are underway, including 3-D constitutive relations and fracture toughness.

Nanoengineered hierarchical composites hybridized with aligned CNTs are prepared by placing long (>20 μm) aligned CNTs at the interface of advanced composite plies as reinforcement in the through-thickness axis of the laminate (see Figure 2). Three fabrication routes were developed: transplantation of CNT forests onto pre-impregnated plies ("nanostitching"), placement of detached CNT forests between two fabrics followed by subsequent infusion of matrix, and \textit{in situ} growth of aligned CNTs onto the surface of ceramic fibers followed by infusion or hand-layup. Aligned CNTs are observed at the composite ply interfaces and give rise to significant improvement in interlaminar strength, toughness, and electrical properties. Extensions of the CNT-based architectures to ceramic-matrix nanocomposites and towards multifunctional capabilities are being developed, including structural health monitoring and deicing.
Two-dimensional transition metal dichalcogenides (2-D TMDs) have shown great promise to be an ideal candidate for post-silicon technology. Their atomic thicknesses and large carrier effective masses can offer excellent electrostatic gate control, a reduced source-to-drain leakage current, and a higher on-current in the ballistic regime, potentially enabling ultra-scaled devices, tunnel field-effect transistors, and ballistic transistors. However, the intricacy and diversity of the structural defects in 2-D TMDs significantly affect their electrical and optical properties, in either beneficial or detrimental ways. In the case of monolayer MoS$_2$, several challenging issues including Fermi level pinning at metal/MoS$_2$ interface, unintentional n-type doping, and carrier scatterings, non-radiative excitonic recombinations, etc., have been attributed to a considerable amount of sulfur vacancy in monolayer MoS$_2$.

On the other hand, specific types of defects, if controlled carefully, also offer the access to engineer the nature of monolayer MoS$_2$, such as channel polarity modification for realization of low-power MoS$_2$-based CMOS integrated circuits, exciton reservoirs to prolong the excitonic lifetime for high-performance optoelectronic and photonic devices.

This work explores the correlation between the domain geometries and the presence of different types of defects in monolayer MoS$_2$ synthesized by chemical vapor deposition through transport and spectroscopy measurements. We show that the shapes of MoS$_2$ domain can modulate the photoluminescence intensity and work function of MoS$_2$ monolayers and the threshold voltage in the MoS$_2$ field-effect transistors. Based on a two-defect-state model, the geometry-modulated behavior can be explained. This work not only offers a strategy to engineer the nature of MoS$_2$ from the synthesis perspective, but also pave a path to realize low-power MoS$_2$ CMOS integrated circuits.

FURTHER READING

Graphene technology has been widely explored to produce large sheets of conductive film to facilitate the manufacturing of flexible transparent photovoltaics. Monolayer-thick graphene has 97% transmittance in the visible regime and outstanding mechanical and electrical properties: that makes graphene suitable for transparent electrodes in order to replace the current state-of-the-art ITO electrodes, which are less flexible and are limited by the low indium supply on earth. However, scaling up the graphene manufacturing is tricky since it is typically grown on copper foils by chemical vapor deposition (CVD), and therefore, an additional transfer step is required to insert the graphene sheet into practical devices. The success of the transfer process is critical for the performances and the scalability of the graphene film.

Given the compatibility with the manufacturing processes in organic and flexible electronics, we explore roll-to-roll (R2R) to enable the deployment of large area graphene on plastic substrates. We investigate how to avoid defects and fractures in the graphene film upon transfer. We scan over several options in order to figure out how the interplay of adhesion forces between the graphene and the host substrate works out. These investigations will advance the progress of the application of graphene in future flexible electronics.

FURTHER READING:
Bonding technology plays a significant role in electronic packaging as it provides physical and electrical connections between semiconductor chips. Reliability of bonding joints affects the energy consumption and speed of an electronic system. Hence, it is important to have a reliable bonding technology. Copper (Cu) bonding technology is one of the most frequently-used bonding technologies nowadays. However, two critical issues have been limiting the reliability of lead-free Cu bonding technology: high bonding temperature (~260 °C) and aging degradation.

We have devised a graphene-based Cu bonding technology that is of low bonding temperature and high reliability. By integrating nanoscale graphene/Cu composite on the Cu substrate prior to thermocompression bonding, Sn-Cu joints can be fabricated at a bonding temperature as low as 150 °C, which is the lowest reported value to date for Cu bonding technology. Specifically, we electrochemically deposit a layer of Cu nanocone array on the Cu substrate and cover it with a graphene sheet, prior to the bonding process. When subjected to heat, microscale Sn solder deforms and replicates the Cu nanocone array morphology, and hence transforming into nanoscale Sn. Compared to microscale Sn, nanoscale Sn has much lower melting points and facile surface diffusion. This phenomenon effectively contributes to the low bonding temperature observed in our bonding technology. The presence of the graphene layer prevents the formation of Cu-Sn intermetallic compounds thus significantly slows down the aging degradation. With the advancement in graphene synthesis and transfer technology, we anticipate the graphene-based Cu bonding technology presented in this work can be integrated into the existing commercial Cu bonding technology for industrial applications in the near foreseeable future.

**FURTHER READING**

Chemical Vapor Deposition of Multiple Transition Metal Disulfides in One Synthesis Step

W. S. Leong, J. Kong
Sponsorship: MIT-SUTD Postdoctoral Fellowship, AFOSR FATE-MURI

Recently, transition metal disulfides (TMD) have received tremendous attention due to their exceptional optical and electrical properties. Many techniques have been explored to obtain monolayer TMD and chemical vapor deposition (CVD) synthesis using transition metal oxide, and chalcogenide solid precursors is the most common method used in laboratories now. However, the quantity of solid precursors used is usually surplus giving rise to chemical reactions between precursors in each of their crucibles, as a result of precursors’ diffusion at growth temperature. Hence, a CVD setup is normally dedicated for the growth of only one type of TMD to avoid cross-contamination (except for hetero-structures synthesis), and it is impossible to grow multiple monolayer TMD in one synthesis step. Here, we report a new technique to synthesize MoS\(_2\) and WS\(_2\) monolayer films in one CVD process. We first disperse a minuscule amount of metal oxide precursor on targeted substrates, which were then loaded to the furnace in slanting position, rather than horizontal, followed by a sulfur annealing to concurrently grow monolayer MoS\(_2\) and WS\(_2\) on separate substrates. The synthesized TMD films exhibit good properties as confirmed by Raman, PL, XPS, STEM analyses, and electrical measurements.

![Figure 1: a-d) Schematic illustration of the concurrent synthesis process of monolayer MoS\(_2\) and WS\(_2\), e) Image showing experimental setup used, f) Image showing the custom-made ceramic boat which was designed such that multiple Si/SiO\(_2\) wafers can be loaded at once in slanting position.](image)

FURTHER READING

Remote Epitaxy through Graphene for Two-dimensional Material Based Layer Transfer

Y. Kim, K. Lee, K. Qiao, S. Bae, H. Kum, W. Kong, J. Kim
Sponsorship: Masdar Institute, LG Electronics, DARPA, AFRL

Van der Waals epitaxy (vdWE) has gained great interest for crystalline growth as it substantially relaxes the strict lattice matching requirements in conventional heteroepitaxy and allows for facile layer release from the vdWE surface. In recent studies, vdWE was investigated on two-dimensional (2-D) materials grown or transferred on arbitrary substrates, with the primary notion that the 2-D material is the sole epitaxial seed layer in vdWE. However, the underlying substrate may still play a role in determining the orientation of the overlayers since the weak vdW potential field from 2-D materials may barely screen the stronger potential field from the substrates.

Here, we reveal that the epitaxial registry of adatoms during epitaxy can be assigned by the underlying substrate remotely through 2-D materials by modulating the interaction gap between the substrate and the epilayer. Our study shows that remote epitaxial growth can be performed through a single-atom-thick gap defined by monolayer graphene at the substrate-epilayer interface. Simulations using density functional theory (DFT) prove that remote epitaxy can occur within a ~9 Å substrate-epilayer gap. We experimentally demonstrate successful remote homoepitaxy of GaAs(001) on GaAs(001) substrates through monolayer graphene (Figure 1). Characterization by high-resolution scanning transmission electron microscopy (HRSTEM) confirms single crystalline growth of GaAs film through graphene with an interaction gap of 5 Å below the critical limit outlined by the simulation. The concept of remote homoepitaxial growth is further extended to other compound semiconductors such as InP, GaP, GaN, as well as functional oxides, SrTiO$_3$, and fluoride material systems, LiF (Figure 2). Following the growth, the single-crystalline films are rapidly released from the vdW surface of graphene to provide large-scale, single-crystalline films. This concept, here termed 2-D material based layer transfer (2-DLT), suggests a universal method to copy/paste epitaxial films of any material systems based on the underlying substrates through 2-D materials then rapidly release and transfer to substrates of interest. The potential to reuse graphene-coated substrates suggests 2-DLT will greatly advance non-Si electronics and photonics by displacing the high cost of non-Si substrates.

**FURTHER READING**

Towards Dislocation-free GaN

W. Kong, K. Qiao, J. Kim
Sponsorship: Analog Devices, Inc.

The performance of advanced GaN-based electronics and optoelectronics can rely heavily on the structural quality of the epilayer used in its fabrication. The layer’s characteristics, such as dislocation density or surface roughness, are largely inherited from the initial GaN growth. Due to the limited availability and the cost of high-quality bulk GaN substrates, heteroepitaxy of GaN on foreign substrates such as Al₂O₃, SiC, and Si is conventionally used. The lattice and thermal-expansion-coefficient mismatch of these substrates to GaN unavoidably lead to the formation of dislocations, as well as potential cracks and wafer bow.

In addition, the majority of the substrate material is usually removed from state-of-the-art devices to lower the thermal resistance of the packaged devices and improve performance. The removal of GaN devices from bulk/foreign substrates is very challenging and is an ongoing subject of research. Existing removal processes involving photoelectrochemical etching, mechanical spalling, and laser interface decomposition suffer from slow processing speed and/or significant surface roughening and cracking, limiting the process yield and practicality of substrate reusing.

Recently, we discovered that the epitaxial registry of adatoms could be determined by the underlying substrate remotely without direct contact with the substrate, but through a narrow gap defined by monolayer graphene. Therefore, homoepitaxial growth can be performed remotely through the single-atom-thickness gap, with the dislocation density of the epitaxial thin film at the same level as the high-quality substrate. In addition, because of the van der Waals interaction at the graphene interface, the epitaxial thin film can be precisely and rapidly exfoliated from the substrate, demonstrating the atomic flatness at the released surface mimicking the morphology of graphene surface. We performed the remote epitaxy of GaN on GaN/sapphire substrate with monolayer graphene as an interlayer to demonstrate high-quality, low dislocation density GaN thin films. We obtained GaN epilayer with material quality identical to the GaN/sapphire substrate in terms of surface morphology and dislocation density. We further exfoliated the GaN epitaxial thin film from the substrate achieving freestanding GaN of 300nm thick.

Ultimately, we will develop the process of GaN remote epitaxy on bulk GaN substrate with minimal defects, enabling the GaN-based electrical and optoelectronic devices approaching intrinsic performance without the limitation from material quality. On the other hand, the cost of such high-performance devices will be significantly reduced since expensive substrates will be reused.

Figure 1. a. Schematic diagram of remote epitaxy of GaN on GaN/sapphire template. b. High resolution X-ray diffraction ω/2θ scan of GaN showing (0002) peak. c. Surface morphology of remote epitaxial GaN. d. Exfoliation of thin film remote epitaxial GaN.
High efficiency and fuel flexibility make solid oxide fuel cells (SOFCs) attractive for conversion of fuels to electricity. Reduced operating temperatures, desirable for reduced costs and extended operation, however, result in significant losses in efficiency. This loss has been traced primarily to slow cathode surface reaction kinetics. In this work, we extend previous studies on the promising mixed ionic and electronic conducting perovskite-structured SrTi$_{1-x}$Fe$_x$O$_{3-x/2+\delta}$ (STF) materials system whose exchange kinetics were correlated with the minority electron charge density by replacing Ti with Sn, due to its distinct band structure and higher electron mobility.

Oxygen nonstoichiometry and the defect chemistry of the SrSn$_{1-x}$Fe$_x$O$_{3-x/2+\delta}$ (SSF) system were examined by thermogravimetry as a function of oxygen partial pressure in the temperature range of 973-1273 K. Marginally higher reducibility was observed compared to corresponding compositions in the STF system. The bulk electrical conductivity was measured in parallel to examine how changes in defect chemistry and electronic band structure, associated with the substitution of Ti by Sn, impact carrier density and ultimately electrode performance. Bulk chemical expansion was measured by dilatometry as a function of oxygen partial pressure, while surface kinetics were examined using AC impedance spectroscopy. The electrochemical properties of SSF were found not to differ significantly from the corresponding composition in STF. Though slightly shifted by the larger size of Sn, the defect equilibria and the cathode area specific resistance differed only in a limited way from that in STF. This was attributed to properties being largely dominated by Fe and not by the substitution of Ti with Sn. However, due to asymmetry in the crystal structure caused by the larger size of Sn, both thermal and chemical expansion coefficients of SSF35 were found to be around 20% and 10% lower than those of STF35, thus making SSF35 much more chemo-mechanically stable in SOFC operating conditions.

**FURTHER READING**

Controlling Concentration and Nature of Oxygen Defects in Layered Cuprate-based Materials by Electrical Bias

C. S. Kim, H. L. Tuller
Sponsor: Skolkovo Foundation

Both the nature and concentration of oxygen defects in oxide materials can have a significant impact on their physical and chemical properties, as well as key interfacial reaction kinetics such as oxygen exchange with the atmosphere. Most commonly, the desired oxygen defect concentration, or equivalently oxygen nonstoichiometry, is attained in a given material by controlling the oxygen partial pressure and temperature in which it is equilibrated or annealed. This approach, however, is limited by the range of oxygen partial pressures readily experimentally achievable and requires knowledge of the applicable defect chemical model.

In this study, we fine-tune oxygen defect concentrations in promising rare earth cuprate (RE₂CuO₄: RE = rare earth) solid oxide fuel cell (SOFC) cathode materials by application of electrical potentials across a yttria-stabilized zirconia (YSZ) supporting electrolyte. These layered perovskites can incorporate both oxygen interstitials and vacancies, thereby broadening the range of investigations. Here, we show a strong correlation between oxygen nonstoichiometry values (which are determined by in situ measurement of chemical capacitance) and oxygen surface exchange kinetics (which is inversely proportional to the area-specific-resistance). Both types of oxygen defects – interstitials and vacancies – dramatically enhance surface kinetics. These studies are expected to provide further insight into the defect and transport mechanisms that support enhanced SOFC cathode performance.

▲ Figure 1: Schematic defect diagram using Brouwer approximation for Laᵢ.₈₅Ceᵢ.₁₅CuO₄₊δ (LCCO).

▲ Figure 2: Volumetric chemical capacitance (Cchem, closed squares) and area-specific-resistance (ASR, open circles) of LCCO thin film as functions of effective oxygen partial pressure at 600 °C in log-log plots. Three colors represent three different atmospheres (1.00 atm, 0.20 atm, and 0.04 atm oxygen partial pressures).

FURTHER READING
The ability to image the nanoscale structure of materials with tunable magnetic textures is pivotal for the development of low-power and nonvolatile data storage technologies. Soft X-ray imaging has emerged in the last decade as a powerful and accurate methodology to resolve the bulk domain structure of several magnetic materials — magnetic multilayers, buried interfaces, or skyrmion lattices — as well as nanoelectronic devices under operating conditions.

Soft X-ray imaging relies on two main requirements: (i) the ability to focus a collimated X-ray beam on a spot the size of a few tens of nm and (ii) the ability to scan the focused X-ray beam with nm precision. We have commissioned a new soft X-ray nanofocusing setup installed at beamline CSX-1 of the National Synchrotron Light Source II. The schematics of this setup are shown in Figure 1. A key element is the Fresnel zone plate (inset D), which acts as a diffractive phase mask to focus X-rays to a 70-nm spot at the sample, and is fabricated using e-beam lithographic tools. The beam spot can be moved with the aid of piezo-based nanopositioners (inset C), which translate the X-ray optics while keeping the sample in a fixed position. Diffracted X-rays are collected with a CCD camera in the far field (~30 cm from the sample). The resulting magnetic scattering intensity encodes local antiferromagnetic strength and can be acquired in less than a second. By scanning the X-ray beam across the sample, we are able to probe the spatial distribution of antiferromagnetic order.

We applied this new method to the study of antiferromagnetic rare earth NdNiO$_3$. In particular, and for the first time, we unveil the inhomogeneous nature of the spin-ordered ground state (inset B). Furthermore, we identify the spatial distribution of antiferromagnetic domains and show that it follows a scale-free distribution. Our future focus is to extend our studies to the imaging of nanoscale magnetic textures in antiferromagnetic spintronic materials and devices, including in operando studies as a function of applied current.
Fabrication of Small-pitch Gratings for Smith-Purcell Radiation from Low-energy Electrons

Y. Yang, A. Massuda, C. Roques-Carmes, S. E. Kooi, Y. Yang, C. Murdia, I. Kaminer, M. Soljačić, K. K. Berggren
Sponsorship: ARO, NSF

Swift-moving electrons carry evanescent near-field, which can be coupled to far-field radiation when the electrons move closer to a periodic structure and in parallel to the periodic structure plane. This effect was named after Smith and Purcell, following their first experimental demonstration of the effect. The wavelength of Smith-Purcell radiation depends on the grating pitch and the electron energy. Here, we demonstrate Smith-Purcell radiation in the optical regime by using gratings with 50-60 nm pitch and electrons with 1.5-6 keV kinetic energy. These results have potential applications in tunable nanoscale light sources.

Our gratings were fabricated on gold-coated silicon substrates. The 200-nm-thick gold coating layer was used to suppress cathodoluminescence from silicon. The grating patterns were defined using electron beam lithography in PMMA resist, followed by 0 °C cold development in IPA:MIBK. 20 nm gold was then deposited via electron-beam evaporation and lifted-off in hot NMP. Figure 1 shows an SEM image of a 50-nm-pitch grating.

To measure Smith-Purcell radiation, the grating samples were mounted inside a modified SEM with an optical attachment to collect the radiated light and measure its spectrum. Electrons with 1.5-6 keV kinetic energy were used to induce the Smith-Purcell radiation. Figure 2 shows the measured Smith-Purcell radiation spectra from a 50-nm-pitch grating using electron beams with different kinetic energies. The peaks of the radiation spectra match well with the theoretical predictions (vertical dashed lines). We demonstrate the Smith-Purcell radiation wavelength decreases as we increase the electron kinetic energy or decrease the grating pitch.

Figure 1: Gold gratings with 50 nm pitch. The grating lines were fabricated on top of a silicon substrate coated with 200 nm gold.

Figure 2: Smith-Purcell radiation spectra from a 50-nm-pitch grating. Different line colors correspond to different kinetic energies of the electron beam. Vertical dashed lines indicate theoretical Smith-Purcell radiation wavelengths.

FURTHER READING

A Scheme for Low-dose Imaging via Conditional Sample Re-illumination

A. Agarwal, V. Goyal, K. K. Berggren
Sponsorship: Gordon and Betty Moore Foundation

Recently, several electron-beam-based low-damage imaging schemes for radiation-sensitive samples (such as proteins and biomolecules) have been investigated. It is now possible to incorporate a Mach-Zehnder interferometer (MZI) in a standard transmission electron microscope (TEM) to perform Elitzur-Vaidman Interaction-free imaging (IFI). We are theoretically investigating the performance of an MZI-based IFI with a Poisson source. We combined IFI with a conditional re-illumination scheme that reduced the probability of imaging errors at low illumination doses.

As a first step, we considered imaging of purely black-and-white pixels. As shown in figure 1, we considered two schemes: classical and IFI, with various imaging detectors. We quantified error as the probability of incorrectly inferring the transparency of a pixel ($P_{\text{err}}$), and damage as the mean number of electrons that scatter off a black pixel ($n_{\text{damage}}$), respectively. At the start of our calculations, we assumed a prior probability $q$ of a given pixel being black. Then, we found expressions to update $q$ based on the electron detection statistics, assuming a Poisson beam with mean $\lambda t$. If the value of $q$ was within a predefined minimum acceptable error threshold $\epsilon$, we made an inference on whether the pixel was black or white. If this condition was not met, we re-updated $q$ using a second round of detection statistics. This process was repeated a maximum of $N_{\text{max}}$ times.

Figure 2 shows the results of imaging utilizing conditional re-illumination, for both classical and IFI. These results were calculated with $N_{\text{max}}=1$ (circles with dotted line) and $N_{\text{max}}=50$ (crosses with dashed lines) illuminations. For both schemes, conditional re-illumination offered a reduction in $n_{\text{damage}}$ at 50 illuminations as compared to single-stage illumination. For classical imaging, $n_{\text{damage}}$ was reduced to 1, and for IFI, $n_{\text{damage}}$ saturated to 0.67, at $N_{\text{max}}=50$.

We are now working on extending these calculations to semi-transparent samples, as well as implementing this illumination scheme in a scanning TEM.

FURTHER READING


Figure 1: Classical (top) and IFI (bottom) schemes. Blue arrows indicate the possible paths that an incident electron can take. 1, 2, and 3 are imaging detectors – 1 and 2 for transmitted, and 3 for scattered electrons.

Figure 2: $P_{\text{err}}$ vs. $n_{\text{damage}}$ for classical (blue) IFI (red) with $\epsilon=0.05$ and $q=0.5$. Dotted lines with circles indicate values for single-stage illumination, and dashed lines with crosses indicate values for 50 illuminations.
A Nanofabricated, Path-separated, Grating Electron Interferometer

A. Agarwal, C.-S. Kim, R. Hobbs, D. van Dyck, K. K. Berggren
Sponsorship: Gordon and Betty Moore Foundation

Recent progress in focused-ion-beam (FIB) technology has enabled the fabrication of electron optical elements such as zone-area plates, phase plates, and beamsplitters. These nanofabricated elements can be used to perform Zernike phase-contrast imaging, holography and beam aberration correction in a conventional transmission electron microscope (TEM). We have fabricated a grating-Mach-Zehnder-electron-interferometer, using FIB milling of a single-crystalline silicon workpiece. As shown schematically in figure 1(a), the interferometer uses two thin layers of silicon as diffraction gratings; the first to split the incident electron beam, and the second to recombine two of the diffracted beams. The gap between the gratings in our interferometer was 20 µm. Fabrication of the gratings from a single crystalline silicon workpiece ensures alignment and precise positioning. We obtained a rotational alignment of ~100 µrad and a grating positioning accuracy of 100 nm. Figure 1(b) is a scanning electron micrograph of this interferometer.

We inserted this interferometer in the sample holder of a 200 kV TEM (JEOL 2010F). We used an electron beam with a diameter of 240 nm on the first grating and convergence semi-angle of 4 mrad in our experiment. As shown in figure 2(b), when imaging the second grating (figure 2(a), sample z-height z₁) at high-resolution (Ψ₀), we obtained a lattice-resolved image of silicon. As we raised our sample holder z-height to move the imaging plane below the second grating (z₁−z₂), the first-order diffracted beam from this grating (Ψ₀g) moved closer to the first-order diffracted beam from the first grating (Ψ₁g), and the two beams overlapped 20 µm below the second grating (z₆). Figure 2(c) is a high-resolution image of the overlapping beams, showing interference fringes of period 0.32 nm, which was expected from the interference of first-order silicon diffracted beams.

This interferometer could be used to perform electron holography in any TEM, as well as interaction-free imaging using the Elitzur-Vaidman scheme.

**Figure 1:** Grating interferometer. (a) Schematic of the interferometer. The two diffracted beams Ψ₀g and Ψ₁g overlap in the ‘interference plane’. (b) Scanning electron micrograph of the grating interferometer. Each grating had a mean thickness of 45nm, and the gap between the gratings was 20µm.

**Figure 2:** Interferometry in TEM. (a) Diffracted beams imaged at different planes (z₁−z₆) below the second grating. The beams Ψ₀g and Ψ₁g overlap 20µm below the second grating. (b) High-resolution TEM image of the central beam (Ψ₀) showing the silicon lattice. (c) High-resolution TEM image of the overlap spot in the interference plane, showing interference fringes.

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**FURTHER READING**

Experimental Characterization and Modeling of Templated Solid-state Dewetting of Thin Single-crystal Films

Y. A. Shin, M. A. L’Etoile, W. C. Carter, C. V. Thompson
Sponsorship: NSF

Solid-state dewetting is a physical phenomenon that disintegrates a continuous film into islands when the film is heated above a characteristic dewetting temperature but kept well below its melting temperature. It is driven by surface energy minimization and mediated via surface diffusion of atoms. Solid-state dewetting has been thought of as an issue in microelectronics, however, it has also demonstrated its potential as a simple patterning method that can be used to generate a complex and regular array of micro- and nano-sized structures in a highly reproducible way (Figure 1a, reference 1). It starts either from edges of the film or in the continuous flat region by forming a natural hole. Various instabilities that develop at retracting edges have been understood via modeling and experimenting over the past years, including “pinch-off,” “corner instability [reference 2],” and “Rayleigh-like instability [reference 3]”. The fingering instability as shown in Figure 1b, which is another instability that creates wire-like structures at retracting edges, is our current focus.

Through experiments, we have found conditions that lead to the fingering instability and have learned that spacing between fingers can be controlled via templating of film edge. We have also found that controlling the period of the fingering process affects the kinetics of the fingering, and we have developed an analytical model that predicts a relationship between the retraction rate and finger period. This model agrees well with experimental results. Our increased understanding of the various instabilities at retracting edges can be used to design templates that will lead to specific complex structures during solid-state dewetting.

However, before we can fully exploit our understanding of templated solid-state dewetting to make designed structures, we must understand natural hole formation in thin films. In polycrystalline films, grain boundary triple junctions facilitate hole formation in a well-understood way, but the formation of holes in single-crystal films (Figure 2) is not well understood. Studying this phenomenon is critical because holes can create new edges from which the film retracts. Furthermore, thinner single-crystal films develop more natural holes per unit area, and the growth of these holes can come to dominate the overall reduction of film surface area. Unsuppressed natural hole formation interrupts edge retraction modes that were intentionally patterned to create a specific structure. If controlled, however, the formation of holes could be used to pattern periodic nanostructures that span large length scales, up to several centimeters. In parallel with studying the fingering instability, we are currently working with both Ni films on MgO substrates and Ru films on sapphire substrates to identify and understand the causes of natural hole formation in single-crystal films. By understanding these mechanisms, we aim to develop templated solid-state dewetting into a powerful and cost-effective method for producing nanostructures.

**Further Reading**

Photonics and Optoelectronics

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Effects of Line Edge Roughness on Photonic Device Performance through Virtual Fabrication

S. I. El-Henawy, D. S. Boning
Sponsorship: AIM Photonics

Silicon photonics has garnered a large amount of interest in recent years due to its potential for high data transfer rates and for other, more novel applications. One attractive feature of silicon photonics is its relatively seamless integration with existing CMOS fabrication technologies. That means, however, that it is subject to similar random and systematic variations as are known to exist in CMOS manufacturing processes.

One common source of process variation is Line Edge Roughness (LER), which occurs during lithography. Since LER produces random perturbations to the component geometry, it is likely to influence the light-guiding abilities of photonic components and devices subject to LER.

We study the effect of LER on the performance of a fundamental component, the Y-branch, through virtual fabrication simulations (Figure 1). Ideally, the Y-branch transmits the input power equal to its two output ports. However, imbalanced transmission between the two output ports is observed when LER is imposed on the Y-branch (Figure 2) depending on the statistical nature (amplitude and correlation length) of the LER. The imbalance can be as low as 1% for small LER amplitudes, and reach up to 15% for large LER amplitudes (Figure 3). These results can be captured as worst-case corner models and included in variation-aware photonic compact models.

FURTHER READING
• D. Malati, A. Melloni, and F. Morichetti, “Real Photonic Waveguides: Guiding Light through Imperfections,” Advances in Optics and Photonics, vol. 6, no. 2, pp. 156-224, Jun. 2014.
Reprogrammable Electro-Chemo-Optical Devices

D. Kalaev, H. L. Tuller
Sponsorship: U.S. Department of Energy, Basic Energy Sciences Program

Photonic devices with programmable properties allow more flexibility in manipulation of light. Recently, several examples of reconfigurable photonic devices were demonstrated by controlling the local/overall index of refraction in thin films, either by thermally induced phase change in chalcogenides or by intercalation of lithium into oxides. We propose a novel approach for design of reprogrammable photonic devices based on electrochemical modification of ceria-based electro-chemo-optical devices.

Previously, it was shown that the refractive index of Pr$_x$Ce$_{1-x}$O$_{2-\delta}$ (PCO) is a function of oxygen nonstoichiometry, $\delta$ that can be controlled electrochemically via closely spaced electrodes in a lateral device configuration. For modified transverse configurations, a PCO thin film on yttrium stabilized zirconia (YSZ) substrate with Transparent Conducting Oxide (TCO) top electrode allows for voltage controlled oxygen exchange. Enhanced spatial resolution can be further achieved with the aid of lithographically patterned nano-dimensioned oxide layers.

Figure 1: Nonvolatile change in the optical transmission of Pr$_x$Ce$_{1-x}$O$_{2-\delta}$ (PCO) thin film by electrochemical oxygen pumping. a. Oxygen pumped into the PCO thin film by an applied positive bias, resulting in the low optical transmission. b. Oxygen pumped out of the PCO thin film by an applied negative bias, resulting in the high optical transmission.
On-chip Infrared Chemical Sensor Leveraging Supercontinuum Generation in GeSbSe Chalcogenide Glass Waveguide

Sponsorship: DTRA

In this report, we demonstrate the first on-chip spectroscopic chemical sensor with a monolithically integrated supercontinuum (SC) light source. Unlike traditional broadband, blackbody sources used in benchtop Infrared Radiation (IR) spectrophotometers waveguide SC sources feature high spatial coherency essential for efficient light coupling and manipulation on a photonic chip. Compared to tunable lasers, SC offers superior bandwidth coverage. The broadband nature of SC facilitates access to wavelengths that are difficult to cover using semiconductor lasers, and thereby, significantly expands the identifiable molecule repertoire of spectroscopic sensors. In our experiment, we use chalcogenide glass (ChG) as the waveguide material for both SC generation and evanescent wave sensing. ChGs are known for its broadband infrared transparency, large Kerr nonlinearity, and low two-photon absorption (TPA), ideal characteristics for our application.

400 nm thick Ge$_{22}$Sb$_{18}$Se$_{60}$ (GeSbSe) films were thermally evaporated onto 4” silicon wafers with 3 µm thermal oxide as an under cladding from GeSbSe glass powders. GeSbSe waveguides with varying length were fabricated using our previously established protocols. In the process, a 350-nm-thick ZEP resist layer was spun onto the substrate followed by exposure on an Elionix ELS-F125 tool at a beam current of 10 nA. The resist pattern was then developed by immersing in ZED-N50 developer for one minute. Reactive ion etching was performed in a PlasmaTherm etcher to transfer the resist pattern to the glass layer. The etching process used a gas mixture of CHF$_3$ and CF$_4$ at 3:1 ratio and 5 mTorr total pressure. The incident Radio Frequency (RF) power was fixed at 200 W.

Finally, the device was immersed in N-Methyl-2-pyrrolidone (NMP) overnight to remove the ZEP resist and complete device fabrication. The waveguides assume a zigzag geometry with lengths up to 21 mm. Figure 1a plots the SC spectra in GeSbSe waveguides with the different lengths and the optimal dimensions (W = 0.95 µm, H = 0.4 µm). As indicated in the figures below, the SC bandwidth extends to over half an octave, albeit with decreased total output power when the waveguide length increases to 21 mm. In the sensing experiment, the GeSbSe waveguide was immersed in carbon tetrachloride (CCl$_4$) solutions containing varying concentrations of chloroform (CHCl$_3$). The CCl$_4$ solvent is optically transparent across the near-IR, whereas the C-H bond in chloroform leads to an overtone absorption peak centering at 1695 nm, a wavelength outside the standard telecommunication bands. SC spectra near the chloroform absorption peak obtained with GeSbSe waveguides of different lengths are presented in Figure 1b. The data were normalized to the background (collected in pure CCl$_4$).

![Figure 1 (a) SC spectrum generated from our waveguide; (b) absorption peak of CHCl$_3$ on our sensor chip.](image)

**FURTHER READING**

Chemical sensors are important for many applications, from sensing explosive residues for homeland security and defense to sensing contaminants in air and water for environmental monitoring. However, the sensors currently used for these purposes are either bulky, not very sensitive, or not able to identify a chemical specifically. Integrated photonic sensors, which include a light source, photonic sensing element, and photonic detector integrated directly on-chip, that can operate in the mid-infrared (MIR) chemical fingerprint region, promise to be small, sensitive, and specific chemical sensors. They achieve this by confining light within waveguides packed into a small area and using the evanescent field that exists outside the waveguides to sense the presence of a chemical through absorption spectroscopy, identifying chemicals by their unique absorption spectra. This work focuses on designing and fabricating the first ever MIR integrated sensing element combined with a detector, operating at room temperature.

A spiral waveguide design was chosen for the sensing element due to its long interaction length, which improves sensitivity, while still maintaining a small area footprint. Fabrication was done using a double layer electron beam lithography and liftoff technique to reduce the waveguide sidewall roughness, and therefore loss, of the thermally evaporated chalcogenide glass waveguides. The thermally evaporated polycrystalline PbTe detector was deposited directly underneath the waveguide using photolithography and liftoff. This direct integration of the detector with the waveguide improves coupling of light into the detector while also reducing the size, and therefore noise, level of the detector, allowing it to function at room temperature when most MIR detectors need cooling. Figure 1 shows the spiral sensing element and waveguide integrated PbTe detector. The results from sensing methane gas using 3.3 μm light are shown in Figure 2, demonstrating that this integrated sensing element and detector can effectively sense the presence of chemicals using their MIR absorption spectra.

**FURTHER READING**

Broadband Low-loss Nonvolatile Photonic Switches Based on Optical Phase Change Materials (O-PCMs)

Q. Zhang, Y. Zhang, J. Li, R. Soref, T. Gu, J. Hu
Sponsorship: DARPA

Optical switching is an essential function in photonic integrated circuits. Recently, a new class of devices based on O-PCMs have emerged for on-chip switching. Unlike electro-optic or thermo-optic effects which are minuscule, phase transition in O-PCMs generates huge optical property modulation conducive to ultra-compact device architectures. In addition, such phase changes can be non-volatile, exemplified by the transition between amorphous (a-) and crystalline (c-) states in chalcogenide alloys. Despite these attractive features, the performances of existing PCM-based photonic switches are severely compromised by the high optical absorption in traditional O-PCMs.

Here we report the design and modeling of a new kind of photonic switches combining low-loss phase change alloys and a “nonperturbative” design to boost the switching performance. On the one hand, we use a low-loss O-PCM for this application: Ge$_2$Sb$_2$Te$_5$ (GST225). Fig 1a and 1b show the optical constants of GST225 compared with traditional PCM Ge$_2$Sb$_2$Te$_5$ (GST225), as measured by ellipsometry. At telecommunication wavelength, the material figure-of-merit, which is defined as index change over extinction coefficient, is 6 times higher. Moreover, the loss of amorphous state GSS4T1 is 0.00017 measured by waveguide cutback method, which is two orders of magnitude lower. On the other hand, the switch design is based on the huge index change of O-PCMs. The basic element is a directional coupler comprised of a bare waveguide (WG1) and a waveguide covered with a PCM strip (WG2). At (a-) state, their indices are matched, and light will be coupler from WG1 to WG2. At (c-) state, due to the large index change of O-PCM, the modal profile will be completely different, and effective index of WG2 will increase a lot so that coupling will not happen. This helps to keep the loss at a low level since light will not travel in WG2 when GSS4T1 is in its (c-) state. Fig 2 and 3 show the state-of-the-art performance of the 1 by 2 and 2 by 2 switches designed by this method.

FURTHER READING
Black phosphorus (BP) is a promising 2-D material that has unique in-plane anisotropy and a 0.3 eV direct bandgap in the mid-IR. However, waveguide integrated black phosphorus photodetectors have been limited to the near-IR on top of Si waveguides that are unable to account for BP’s crystalline orientation. In this work, we employ mid-IR transparent chalcogenide glass (ChG) both as a broadband mid-IR transparent waveguiding material to enable waveguide-integration of BP detectors and as a passivation layer to prevent BP degradation during device processing as well as in ambient atmosphere.

Our ChG-on-BP approach not only leads to the first demonstration of mid-IR waveguide-integrated BP detectors, but also allows us to fabricate devices along different crystalline axes of black phosphorus to investigate, for the first time, the impact of in-plane anisotropy on photoresponse of waveguide-integrated devices. The best device exhibits responsivity up to 40 mA/W and noise equivalent power as low as 30 pW/Hz^1/2 at 2185 nm wavelength. We also found that photodetector responsivities changed by an order of magnitude with different black phosphorus orientations. This work validates black phosphorus as an effective photodetector material in the mid-IR and demonstrates the power of the glass-on-2-D-material platform for prototyping of 2-D material photonic devices.

**FURTHER READING**

An Ultrasensitive Graphene-polymer Thermo-mechanical Bolometer

Y. Lin, X. Ji, E. N. Tas, H. Cheung, J. Lang, J. Kong, T. Palacios
Sponsorship: NSF CIQM, ARO MIT-ISN

Uncooled mid-infrared (Mid-IR) detection and imaging technologies are highly desired for night vision, security surveillance, remote sensing, industrial inspection, medical, and environmental chemical sensing. Traditional mid-IR detection technologies operating at room temperature are all associated with thermal related phenomena that transfer the optical signals into electrical signals through changes of temperature on the device. Here we propose and implement a new signal transducing scheme where the energy transfer path is optical-thermal-mechanical-electrical. By combining highly sensitive strain sensors made with percolative graphene nano-flake films synthesized by Marangoni self-assembly method, and the highly efficient polymer opto-thermo-actuators, we were able to demonstrate the proof-of-concept bolometric type mid-IR detectors (Figure 1) that could be more sensitive than state-of-the-art technologies.

Two types of photoresponse behaviors were observed in our devices: a gradual change in resistance in terms of temperature (Figure 2(a)), which may be associated with the average overlap area decrease of adjacent nano-flakes; and an abrupt “switch” like response (Figure 2(b)) that is presumably due to the decrease of the number of conduction paths of the percolative film. Microscopic characterizations and theoretical modeling were carried on to understand such behaviors. Theoretical analysis showed that our new technology could be at least one order of magnitude more sensitive than the fundamental limit of existing uncooled mid-IR technologies (Figure 2(c)).
Nanocavity Design for Reduced Spectral Diffusion of Solid-state Defects

S. Mouradian, N. Wan, M. Walsh, E. Bersin, D. Englund
Sponsorship: AFOSR

The negatively charged nitrogen-vacancy (NV) center in diamond has an electronic spin state that can be optically initialized, manipulated, and measured. Entanglement generation between two spatially separated quantum memories can be generated by coupling them to optical modes. Coupling NV centers to nanophotonic devices such as waveguides and cavities will boost the NV-NV entanglement rate by increasing the emission and collection rate of photons entangled with the spin resonators.

We can fabricate 1D photonic crystal nanobeam cavities in diamond with quality factors larger than 16,000. Unfortunately, an optimally coupled NV center in such a cavity will be only 30 nm from surfaces, and the linewidths of NV centers in such cavities is increased to 10s of GHz (1000x the natural lifetime limited linewidth) due to spectral diffusion.

To obtain NV centers with GHz linewidths in a cavity with a high-quality factor, we design and fabricate novel “Alligator’’ cavities. A bandgap is created via a sinusoidal width modulation. A high-Q mode is trapped in a defect created by reducing the amplitude of the modulation. The optimized mode (seen in Figure (a)) has a Q > 100,000 in simulation. We fabricate these cavities from single crystal bulk diamond. A scanning electron micrograph of one is seen in Figure (b). In experiment, we measure cavities with a mean Q value of ~7000 (Figure (d)). Figure (c) shows the spectrum of such a cavity. These structures should allow coupling between single NV centers with limited spectral diffusion and high-quality factor cavity modes.

▲ Figure 1 (a) Mode profile of the optimized fundamental TE mode of an Alligator cavity. (b) Scanning electron micrograph of a fabricated Alligator cavity. (c) Spectrum of a cavity resonance (Q = 10,820). (d) Distribution of quality factors over 15 measured devices.
Color centers in diamond are leading candidates for quantum information processing. Recent demonstrations of entanglement between separated spins of the nitrogen-vacancy (NV) color center constitute a major milestone in generating and distributing quantum information with solid-state quantum bits. However, the generation of entanglement in local quantum nodes containing NV centers is an inefficient process due to the largely incoherent NV optical transitions, as the zero-phonon-line (ZPL) constitutes only 4% of the NV’s spontaneous emission. This fraction can be modified if the NV center is placed in a photonic cavity, which modifies the electromagnetic environment, and thus, the NV’s emission properties via the Purcell effect. Photonic crystal (PhC) slab nanocavities offer high-quality factors (Q) and small mode volumes (V), which considerably increase the fraction of emission into the ZPL. Figure 1(A) shows the electric field profile in such a nanocavity, where the lattice constant is $a = 214$ nm and the thickness of the slab is $H = a$.

The fabrication of such structures, however, typically requires laborious reactive-ion etching (RIE) thinning of a bulk diamond down to a thickness of $H$. This need arises because high-quality single-crystal diamond thin films are not available and the chemically inert nature of diamond precludes wet undercutting techniques. In this work, we fabricate PhC nanocavities in diamond directly from bulk diamond. Electron beam lithography and reactive ion etching (RIE) first defines the PhC structures, after which alumina deposited using atomic layer deposition conformally coats and protects the diamond sidewalls. Then, anisotropic oxygen plasma undercuts the diamond slabs and, finally, hydrofluoric acid removes the hard mask and alumina to reveal suspended diamond structures (Figure 1(B)). We find high Q resonances near the NV ZPL wavelength of 637 nm, as shown in the photoluminescence spectra in Figure 1(C). The fabrication details and cavity measurements are in the last reference.

In conclusion, we report the first fabrication of photonic crystal slab nanocavities in bulk diamond. Immediate steps include the coherent coupling of a single NV center to the nanocavity, which will serve as a node in a quantum repeater and for solid-state cavity quantum electrodynamics investigations. This 2-D platform considerably expands the toolkit for classical and quantum nanophotonics in diamond.

![Figure 1](image-url)

**Figure 1:** (A) Electric field profile in an L3-defect nanocavity with a simulated $Q = 8560$. (B) Scanning electron microscope image of the diamond L3 nanocavity. (C) Photoluminescence spectrum of a single NV center, which reveals a high Q resonance at 639.4 nm.

**FURTHER READING**

Quasi-Bessel-Beam Generation using Integrated Optical Phased Arrays

J. Notaros, C. V. Poulton, M. J. Byrd, M. Raval, M. R. Watts
Sponsorship: DARPA E-PHI Program, NSF GRFP

Due to their unique diffractive properties, Bessel beams have contributed to a variety of important advances and applications, including multiplane optical trapping, reduced scattering and increased depth of field microscopy, improved laser corneal surgery, and adaptive free-space communications. Recent work has turned toward generation of Bessel beams using compact form factors, including spatial light modulators, Dammann gratings, and metasurfaces. However, these demonstrations do not provide full on-chip integration, and most are fundamentally limited to static beam formation.

In this work, integrated optical phased arrays, which manipulate and dynamically steer light, are proposed and demonstrated for the first time as a method for generating quasi-Bessel beams in a fully integrated, compact-form-factor system (Figure 1). First, the phase and amplitude distributions necessary for generating phased-array-based Bessel-Gauss beams are derived analogously to bulk-optics Bessel implementations. Next, a splitter-tree-based CMOS-compatible phased array architecture (Figure 2) is developed to passively encode arbitrary phase and amplitude feeding of the array – necessary for Bessel-Gauss-beam generation. Finally, the developed theory and system architecture are utilized to demonstrate a 0.64 mm × 0.65 mm aperture integrated phased array that generates a quasi-one-dimensional Bessel-Gauss beam with a ~14 mm Bessel length and ~30 μm power FWHM (Figure 3).

FURTHER READING

In this research (a collaboration with Dr. Daniel Smalley of Brigham Young University), we design and fabricate acousto-optic, guided-wave modulators in lithium niobate for use in holographic and other high-bandwidth displays. Guided-wave techniques make possible the fabrication of modulators that are higher in bandwidth and lower in cost than analogous bulk-wave acousto-optic devices or other spatial light modulators used for diffractive displays; these techniques enable simultaneous modulation of red, green, and blue light. In particular, we are investigating multichannel variants of these devices with an emphasis on maximizing the number of modulating channels to achieve large total bandwidths. To date, we have demonstrated multichannel full-color modulators capable of displaying holographic light fields at standard-definition television resolution and at video frame rates. Our current work explores a device architecture suitable for wearable augmented reality displays and other see-through applications, in which the light outcouples toward the viewer (Figure 1), fabricated using femtosecond laser micromachining (Figure 2).

**FURTHER READING**

A Scalable Single-photon Detector Array Based on Superconducting Nanowires

Sponsorship: AFOSR, DARPA, NSF

Detecting single photons over large numbers of spatial modes is crucial for photonic quantum information processing. This measurement usually requires an array of time-resolved single-photon detectors. The superconducting nanowire single-photon detectors (SNSPDs) are currently the leading single-photon counting technology in the infrared wavelength and have the highest performance in timing jitter, detection efficiency, and counting rate. In a conventional readout scheme, each SNSPD requires one coaxial cable in the cryostat, a low-noise RF amplifier, and a high-resolution time-to-digital converter. Implementing a system of a few SNSPD channels with the conventional readout is possible, but scaling them to tens or hundreds of channels requires formidable resources and remains an outstanding challenge.

Here, we report a scalable two-terminal SNSPD array that only requires one pair of RF cables for the readout. Figure 1 shows the architecture of the array, where a chain of detectors was connected using superconducting nanowire delay lines. The nanowire delay lines were designed to be slow-wave transmission lines with a phase velocity of only 0.016c, where c is the speed of light in vacuum. When a detector absorbs a photon and fires, it generates a pair of counter-propagating pulses towards the two terminals. By registering the pulses on the two terminals, and performing simple timing logic, one can resolve the arrival locations of up to two incident photons (see Figure 2). By analyzing the electrical pulse shapes, we also showed photon-number-resolving capability in a 4-element device. This device architecture will be useful for multi-photon coincidence detection in photonic integrated circuits.

**FURTHER READING**

Efficient, transparent electrode materials are vital for applications in smart window, LED display, and solar cell technologies. These materials must possess a wide band gap for minimal optical absorption in the visible spectrum while maintaining high electrical conductivity. Tin-doped indium oxide (ITO) has been the industry standard for transparent electrodes, but the use of the rare element indium has led to a search for better material alternatives. BaSnO$_3$ represents a promising alternative due to its high electron mobility and resistance to property degradation under oxidizing conditions, but the mechanisms by which processing conditions and defect chemistry affect the final material properties are not well understood.

This work seeks to better understand the relationships between processing, defect chemistry, and material properties of BaSnO$_3$ to better establish the consistent and controllable use of BaSnO$_3$ as a transparent electrode. To accomplish these goals, methods such as in situ resistance and impedance monitoring during annealing will be applied. In addition, a variety of novel methods such as the in situ monitoring of optical transmission (shown in Figure 1) during annealing and the in situ monitoring of resistance during physical vapor deposition will be utilized to investigate BaSnO$_3$. Direct measurements of the key constants for the thermodynamics and kinetics of oxidation in donor-doped BaSnO$_3$ will be experimentally determined for the first time. This increase in understanding will provide a predictive model for determining optical properties, carrier concentrations, and electron mobilities in BaSnO$_3$, which may become increasingly important due to its high electron mobility, high-temperature stability, and favorable crystal structure.

**FURTHER READING**

Biological, Medical Devices, and Systems

High-throughput Measurement of Single-cell Growth Rates using Serial Microfluidic Mass Sensor Arrays

Iso-dielectric Separation of Cells and Particles

Microfluidic Electronic Detection of Protein Biomarkers

Continuous Biomanufacturing Using Micro/nanofluidics

Ion Concentration Polarization Desalination using Return Flow System

A Printed Microfluidic Device for the Evaluation of Immunotherapy Efficacy

Biocompatible Dielectric-conductive Microsystems Monolithically 3-D Printed via Polymer Extrusion

Mini Continuous Stirred Tank Reactors (mini-CSTR) for Cell and Tissue Culture Applications

Chaotic Flows as Micro- and Nanofabrication Tools

On-chip Photonic Aerosol Spectrometer for Detection of Toxic Inhalable Materials

Close-packed Silicon Microelectrodes for Scalable Spatially Oversampled Neural Recording

Building Synthetic Cells for Sensing Applications

The AutoScope: An Automated Point-of-Care Urinalysis System

Cardiac Output Measurement using Ballistocardiography and Electrocardiography

Continuous and Non-invasive Arterial Pressure Waveform Monitoring using Ultrasound

Breathable Electronic Skin Sensor Array through All-in-One Device Transfer

Secure System for Implantable Drug Delivery

Enabling Saccade Latency Measurements with Consumer-grade Cameras for Monitoring of Neurodegenerative Disease Progression
High-throughput Measurement of Single-cell Growth Rates using Serial Microfluidic Mass Sensor Arrays


Sponsorship: NIH, AFOSR

Methods to rapidly assess cell growth would be useful for many applications, including drug susceptibility testing, but current technologies have limited sensitivity or throughput. Here we present an approach to precisely and rapidly measure growth rates of many individual cells simultaneously.

We flow cells in suspension through a microfluidic channel with 10–12 resonant mass sensors distributed along its length, weighing each cell repeatedly over the 4–20 min it spends in the channel (Figures 1, 2). Because multiple cells traverse the channel at the same time, we obtain growth rates for >60 cells/h with a resolution of 0.2 pg/h for mammalian cells and 0.02 pg/h for bacteria. We measure the growth of single lymphocytic cells, mouse and human T cells, primary human leukemia cells, yeast, Escherichia coli and Enterococcus faecalis. Our system reveals subpopulations of cells with divergent growth kinetics and enables assessment of cellular responses to antibiotics and antimicrobial peptides within minutes.

FURTHER READING


The development of new techniques to separate and characterize cells with high throughput has been essential to many of the advances in biology and biotechnology over the past few decades. We are developing a novel method for the simultaneous separation and characterization of cells based upon their electrical properties. This method, iso-dielectric separation (IDS), uses dielectrophoresis (DEP, the force on a polarizable object) and a medium with spatially varying conductivity to sort electrically distinct cells while measuring their effective conductivity (Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis to concentrate cells and particles to the region in a conductivity gradient where their polarization charge vanishes [Figure 1].

Sepsis is an uncontrolled activation of the immune system that causes an excessive inflammatory response. There is an unmet need to develop tools to monitor sepsis progression, which occurs quickly and provides few clues to indicate if treatment is effective. Previously, we have found the electrical profile of leukocytes changes with activation state, and we have applied IDS to characterize the electrical profile of leukocytes for monitor sepsis. After working with neutrophils, we also found that IDS can be used to distinguish different types of leukocytes having different dielectric properties. As Figure 2 suggests, once cell properties such as size, permittivity and conductivity of each part change, Clausius-Mossotti (CM) factor changes and it explains the reason why we can distinguish different types of cells in IDS. We could distinguish neutrophils and T-cells (the majority of lymphocytes) at the frequency of 5 MHz and the area under ROC curve was 0.8473. To advance the automation of the system and reduction sample preparation for clinical deployment, we could integrate the upstream separator such as inertial microfluidic sorter for removal of red blood cells (RBC) from the patient’s blood samples. It might be possible to monitor sepsis from patients in pseudo-real time.

FURTHER READING

Microfluidic Electronic Detection of Protein Biomarkers

D. Wu, J. Voldman
Sponsorship: Analog Devices, Inc.

Traditional blood tests are performed in centralized laboratories by trained technicians and need days to deliver results. The need of ~mL blood sample also makes it challenging to apply the traditional tests to preemies or even newborns. We are developing a miniaturized microfluidic electronic biosensor, which gives immediate results (within 30 minutes) and needs ~μL blood, for diagnosis of neonatal sepsis. To achieve this goal, we developed portable PCB-based multiplexed amperometry circuitry and a bead-based electronic enzyme-linked immunosorbent assay. Combining the circuitry and bead-based assay, we have demonstrated measurement of human interleukin-6, a potential neonatal sepsis biomarkers, in serum with clinically relevant limit of detection (e.g., < 40pg/ml).
Continuous biomanufacturing is a growing trend in the biopharmaceutical industry because it can reduce manufacturing cost and increase product quality. Ideas from micro/nanofluidics can be employed in all aspects of continuous biomanufacturing to enhance the overall productivity as well as the efficacy and safety of the final products.

First, we introduce a novel cell retention device based on inertial sorting for perfusion culture (Figure 1). The cell retention device maintains cells in the bioreactor and removes biologics and metabolites. Hollow fiber membrane is commonly used in the biopharmaceutical industry. However, it has challenges, such as membrane clogging/fouling, low product recovery, and inability to remove dead cells. In this context, we developed a membrane-less microfluidic cell retention device and demonstrated perfusion culture of high-concentration mammalian cells producing monoclonal antibodies for >3 weeks with high product recovery (>99%).

Second, we present a nanofluidic system for continuous-flow, multi-variate (purity, bioactivity, and protein folding) protein analysis for real-time critical quality assessments (Figure 2). This size-based nanofluidic system can complement the existing bench-type conventional analytical tools, such as size exclusion chromatography and gel electrophoresis, to meet quality assurance requirements of current and future biomanufacturing systems. We demonstrated rapid purity and bioactivity monitoring of protein drugs, such as hGH, IFN-alfa-2b, and G-CSF, using the nanofluidic system.

**Figure 1:** System schematic of perfusion culture using a microfluidic cell retention device. The Chinese Hamster Ovary (CHO) cells are maintained in a bioreactor, and monoclonal antibodies produced from these cells are collected in a harvest bottle.

**Figure 2:** Nanofluidic system for multi-variate protein analysis for real-time critical quality assessments. For example, it can monitor purity of Interferon alfa-2b biologic drugs.

**FURTHER READING**

While the conventional electrodialysis (ED) relies on bipolar ion conduction employing two ion exchange membranes, anion exchange membrane (AEM) and cation exchange membrane (CEM), our group has proposed unipolar ion conduction, so-called ion concentration polarization (ICP) desalination, employing only CEM to enhance energy efficiency. Because chloride ion, the majority salt in nature, has faster diffusivity than sodium ion, ICP desalination theoretically has a current utilization (CU) of 1.2, but the ED has only that of 1. To facilitate the ICP desalination, our group has developed series of technology from Bifurcate ICP system to Trifurcate ICP (Tri-ICP) system. Here, we have developed a return flow (RF-ICP) desalination system with a newly designed flow path for improving energy efficiency.

Figure 1 shows a schematic of RF-ICP desalination system, which has three channels separated by two nano-porous membranes. The three channels consist of a concentrate channel on the anodic side, a diluate channel on the cathodic side, and an intermediate channel in between. A feed solution flows through the inlet of intermediate channel with the highest pressure and flows through the outlet of both side channels with the lowest pressure. As the feed solution flows through the channels, a portion of the feed solution flows through the porous membrane (Por-flow) due to the pressure difference. The Por-flows facilitate two types of flow barriers, a suppressor for a chaotic electroconvection in the diluate stream and a preventer for a salt leakage from the concentrate stream. The remaining solution returns at the end of channel (RF-flow) and induces the effect of sweeping a mass on the CEM surfaces by shear stress.

We demonstrate that the developed RF-ICP system reduces a power consumption compared to the previously developed Tri-ICP system. Also, the RF-ICP system showed symmetrical product concentrations between diluate and concentration (data not shown), and the recovery rate increased to 50% compared to the Tri-ICP system, which was 25%. To improve the performance of RF-ICP system, more optimized system would be developed by various operating controls for recovery rate increase or spacer designs for energy efficiency increase.

**Figure 1:** Schematic illustration of ion transport and flow in RF-ICP desalination. Red and yellow arrows indicate the movement of cation $\lambda^+$ and anion $\beta^-$ by electric field, respectively.

**Figure 2:** Power consumption to achieve salt removal ratios with various flow velocities (1.5–3.0 mm/s).

**FURTHER READING**
Inherent challenges in device fabrication have impeded the widespread adoption of microfluidic technologies in the clinical setting. Additive manufacturing could address the constraints associated with traditional microfabrication, enabling greater microfluidic design complexity, fabrication simplification (e.g., removal of alignment and bonding process steps), manufacturing scalability, and rapid and inexpensive design iterations.

We have fabricated an entirely 3-D-printed microfluidic platform enabling the modeling of interactions between tumors and immune cells, providing a microenvironment for testing immunotherapy treatment efficacy. The monolithic platform allows for real-time analysis of interactions between a resected tumor fragment and resident or circulating lymphocytes in the presence of immunotherapy agents. Our high-resolution, non-cytotoxic, transparent device monolithically integrates a variety of microfluidic components into a single chip, greatly simplifying device operation when compared to traditionally-fabricated microfluidic systems. Human tumor fragments can be kept alive within the device. In addition, the tumor fragment within the device can be imaged with single-cell resolution using confocal fluorescence microscopy.

Further Reading

Additive manufacturing (AM), i.e., the layer-by-layer construction of devices using a computer-aided design (CAD) file, has been recently explored as a manufacturing toolbox for MEMS. The demonstration of monolithic multi-material devices in 3-D printed MEMS has the potential to implement better, more complex, and more capable Microsystems at a small fraction of the time and cost typically associated with semiconductor cleanroom microfabrication. Fused filament fabrication (FFF) is an AM technique based on extrusion of thermoplastic polymers that is arguably the simplest and cheapest commercial 3-D printing technology available. Here, we report additively manufactured monolithic Microsystems composed of conductive and dielectric layers using an FFF dual extruder 3-D printer. The base material is a biocompatible polymer, polylactic acid (PLA), which can be doped with micro/nanoparticles to become electrically conductive. Characterization of the printing technology demonstrates close resemblance between CAD files and printed objects, generation of watertight microchannels, high-vacuum compatibility, and non-cytotoxicity. A large (~23) piezoresistive gauge factor was measured for a certain graphite-doped conductive PLA, suggesting its utility to implement 3-D printed strain transducers via FFF. Multiplexed electrohydrodynamic liquid ionizers (Figure 1) with integrated extractor electrode and threaded microfluidic port were also demonstrated. The per-emitter current vs. per-emitter flowrate characteristic shows a power dependence with 0.6 coefficient (Figure 2), close to the square-root dependence predicted by de la Mora’s law for the cone-jet emission mode.

FURTHER READING

Mini Continuous Stirred Tank Reactors (mini-CSTR) for Cell and Tissue Culture Applications


Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

An ideal cell culture system will provide a well-controlled, homogeneous, and steady environment for cells and tissues. For instance, well-controlled steady states would greatly benefit organ-on-chip experiments, stem cell culture, and tissue propagation (among other relevant biomedical applications). At present, no continuously stirred mini-reactors are commercially available for lab-scale culture applications.

We are developing simple, low-cost, and user-friendly miniaturized continuously stirred tank reactors (CSTRs) for biomedical and biotechnological agitations. These well-mixed mini-CSTRs will enable cost-efficient continuous culture at small scales. We cast Polydimethylsiloxane (PDMS) casting on poly(methyl-methacrylate) molds, or directly use high resolution 3-D-printing, to fabricate these CSTRs and an Arduino platform to measure and control key parameters, such as agitation, temperature, and pressure, in small portable incubators (Figure 1). Nutrients are fed by syringe pumps, and well-controlled low-speed (benign) agitation is provided by a custom-made magnetic system. Since the reactor behaves as a well-mixed reservoir, all bulk-liquid concentrations can be measured at the outlet stream, thereby greatly reducing the need for intrusive instrumentation. We are currently validating the use of this culture platform in two model applications: (a) the extended culture of breast cancer spheroids, and (b) the culture of Chinese Hamster Ovary Cells (the warhorse for biopharmaceutical production) for continuous production of biopharmaceutical compounds (Figure 2).

**FURTHER READING**


▲ Figure 1: Mini-CSTR controlled by Arduino: Complete setup of the system including a PDMS miniCSTR (a), stepper motor support (b), stepper motor driver (c), Arduino microcontroller (d), container for spent media (e), and fresh media (f). 3-D-printed mini-CSTR (first generation, g), and (second generation, h).

▲ Figure 2: Culture of tumor spheroids by continuous perfusion in this mini-CSTR. (a) Breast cancer tumor spheroids at (a) day 1, (b) day 3, and (c) day 7 of continuous perfusion. (d) The decrease in glucose concentration within the CSTR is an indicator of metabolic activity of the population of spheroids.
Chaotic Flows as Micro- and Nanofabrication Tools


Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

Nature generates densely packed micro- and nanostructures that enable key functionalities in cells, tissues, and other materials. Current fabrication techniques are far less effective at creating microstructure, due to limitations in resolution and speed. Chaos is one of the many mechanisms that nature exploits to create complexity with simple "protocols." For example, chaotic flows have the extraordinary capacity to create microstructure at an exponential rate. We are currently developing a set of microfabrication strategies that we term chaotic printing—the use of chaotic flows for rapid generation of complex, high-resolution microstructures.

In our experiments, we use two classic mixing systems as models—Journal Bearing (JB) flow and the Kenics mixer—to demonstrate the usefulness of chaotic printing. In a miniaturized JB flow (miniJB), we induced deterministic chaotic flows in viscous liquids (i.e., methacryloyl-gelatin and poly-dimethylsiloxane), and deformed an "ink" (i.e., a drop of a miscible liquid, fluorescent beads, or cells) at an exponential rate to render a densely packed lamellar microstructure that is then preserved by curing or photocrosslinking. In a continuous version of chaotic printing, we created chaotic flows by co-extruding two streams of alginate (two inks) through a printing head that contains an on-line miniaturized Kenics mixer. The result was a continuous 3-D-printing of multi-material lamellar structures with different degrees of surface area and full spatial control of the internal microstructure (Figure 1). The combined outlet stream was then submerged in an aqueous calcium chloride solution to crosslink the emerging alginate fibers containing the microstructure.

The exponentially rapid creation of fine microstructure achievable through chaotic printing exceeds the limits of resolution and speed of the currently available 3-D printing techniques. Moreover, the architecture of the microstructure created with chaotic printing can be predicted using computational fluid dynamic (CFD) techniques. We envision diverse applications for this technology, including the development of densely packed catalytic surfaces and highly complex multi-lamellar and multi-component tissue-like structures for biomedical and electronics applications (Figure 2).

FURTHER READING

On-chip Photonic Aerosol Spectrometer for Detection of Toxic Inhalable Materials

R. Singh, D. Ma, A. Agarwal, B. Anthony

Aerosol particles are distributed in the atmosphere and can constitute serious health threats depending on their chemistry, size, and concentration. For instance, particles of different sizes are deposited in different parts of a lung airway and can lead to specific respiratory complications; and aerosols with certain functional groups can be more harmful than others. So, the comprehensive sensing of aerosol particles is critical for human health, particularly with timely monitoring of environmental pollution, industrial pollution, and defense threats. Most existing aerosol sensors are based on free-space detection methods using optical scattering, IR spectroscopy, and electrical property determination. These sensors can suffer from poor sensitivity and be expensive and bulky.

We have developed an on-chip photonic aerosol spectrometer that can perform in situ particle sizing, counting, shape, and chemical characterization. The device is based on an integrated array of waveguide and microresonator structures built on a silicon nitride-on-insulator platform using simple UV photolithography. We have demonstrated that the sensors can estimate the size of particles ranging from 100 nm to 5 microns with particle concentrations over 500 to 105 particles/cm³. An aerosol particle falling on the microresonator sensor interacts with the evanescent field of the resonators and acts as a scatterer causing energy loss. The interaction of these particles with the evanescent mode of the microresonators depends on the particle size, shape and count. Coupled with theoretical scattering models of Mie and Rayleigh, we use the measured data to extract physical properties of the airborne particles. The Q-factor of these resonators is as high as 10⁵ enabling sensing resolution to that of an individual aerosol particle. Similarly, by selecting a combination of the resonant wavelengths in microresonators to develop infra-red spectrum sensitive to the distinctive bands of organic and inorganic functional groups inherent in molecularly structures aerosol particles, the spectrometer can be used to do chemical characterization of aerosol particles. This multi resonator platform is tailor able to single or multi-species detection that can be deployed for a variety of aerosol chemistry sensing applications. The technology offers various advantages in particle sensing modalities by offering improved sensitivity, response time and reduced cost and size of the device.

▲ Figure: Schematic of the setup used in on-chip aerosol spectroscopy. It comprises three different parts: namely, aerosol delivery and transport system, on-chip photonic sensing system, and output pattern and spectrum acquisition system. (b) Fabricated photonic aerosol spectrometer.
Close-packed Silicon Microelectrodes for Scalable Spatially Oversampled Neural Recording

J. Scholvin, K. Payer, C. G. Fonstad, E. S. Boyden
Sponsorship: Simons Center for the Social Brain at MIT, Paul Allen Family Foundation, NYSCF, NIH, NSF, CBMM

A major goal of neuroscience is to understand how the activity of individual neurons yields network dynamics, and how network dynamics yield behavior (and causes disease states). Innovative neuro-technologies with orders-of-magnitude improvements over traditional methods are required to reach this goal. Nanofabrication can provide the scalable technology platform necessary to record with single-spike resolution the electrical activity from a large number of individual neurons, in parallel and across different regions of the brain. By combining innovations in fabrication, design, and system integration, we can scale the number of neural recording sites: from traditionally a small number of sparse sites, to currently over 1000 high-density sites, and in the future beyond many thousands of sites distributed through many brain regions.

We designed and implemented close-packed silicon microelectrodes (Figure 1), to enable the spatially oversampled recording of neural activity (Figure 2) in a scalable fashion, using a tight continuum of recording sites along the length of the recording shank, rather than discrete arrangements of tetrode-style pads or widely spaced sites. This arrangement, thus, enables spatial oversampling continuously running down the shank so that sorting of spikes recorded by the densely packed electrodes can be facilitated for all the sites of the probe simultaneously.

We use MEMS microfabrication techniques to create thin recording shanks and a hybrid lithography process that allows a dense array of recording sites which we connect to with submicron dimension wiring. We have performed neural recordings with our probes in the live mammalian brain, and illustrate the spatial oversampling potential of closely packed electrode sites in Figure 2.

**FURTHER READING**

Building Synthetic Cells for Sensing Applications

M. Hempel, E. McVay, J. Kong, T. Palacios
Sponsorship: AFOSR

Miniaturized sensors, less than 100 μm in diameter, equipped with communication capabilities could enable a new paradigm of sensing in areas such as health care and environmental monitoring. For example, instead of measuring a patient’s blood sugar by pricking their finger and analyzing a drop of blood externally, a microscopic sensor in the bloodstream could sense the glucose concentration internally and communicate data to the outside world non-invasively.

In this project, we work towards this vision by integrating chemical sensors and transistors on 100-µm-wide flexible polymer disks that we call synthetic cells or “SynCells” (see Figure 1). The transistor channels and sensors are made of molybdenum disulfide (MoS2), which it is an excellent material to build digital electronics and highly sensitive sensors. To use the SynCells, they are mixed into a target solution. Upon exposure to a specific substance, the chemical sensors permanently change their electrical resistance. Afterward, the SynCells are retrieved and analyzed externally.

During the last year, we improved our SynCell fabrication process and increased our transistor yield significantly. Furthermore, we successfully demonstrated chemical detection of triethylamine (see Figure 2). As next steps, we want to explore the behavior of our SynCells in microfluidic channels and investigate ways to include time-awareness in these systems.

FURTHER READING

Urinalysis is one of the most common diagnostic techniques in medicine. Over 200 million urine tests are ordered each year in the US, costing between $800 to $2,000 million in direct costs. 46% of all urinalysis tests include microscopic analysis, which involves identifying and counting each particle found in the urine. Microscopic urinalysis is a costly and complex process often done in medical laboratories. An inexpensive and automated cell-counting system would (1) increase access to microscopic urinalysis and (2) shorten the turn-around time for physicians to make diagnostic decisions by permitting the test to be done at the point-of-care.

The AutoScope is an automated, low-cost microscopic urinalysis system that can accurately detect red blood cells (RBCs), white blood cells (WBCs), and other particles in urine. We use a low-cost image acquisition system combined with two neural networks to identify these particles. By not using any optical magnification, we achieve costs three orders of magnitude less than the only commercially available semi-automated urinalysis system and a device size of 8.3 x 6.0 x 8.8 cm.

To validate the system, we calculated the accuracy, sensitivity, and specificity of the AutoScope. The specificity and sensitivity were determined by generating 209 digital urine specimens modeled after urine received in medical labs. The AutoScope had a sensitivity of 88% and 91% and a specificity of 89% and 97% for RBCs and WBCs, respectively. Next, we determined the AutoScope’s accuracy by fabricating 8 synthetic urine samples with RBCs, WBCs, and microbeads. The reference results were confirmed through a medical laboratory. The AutoScope’s counts and the reference counts were linearly correlated to each other \( r^2 = 0.980 \) across all particles. The sensitivity, specificity, and R-squared values for the AutoScope are comparable (and mostly better) than the same metrics for the iQ-200, a $100,000-$150,000 state-of-the-art semi-automated urinalysis system.

FURTHER READING

Cardiac output (CO) is one of several parameters used by cardiologists to stratify risk of patients with cardiovascular disease and has significant clinical relevance. CO is currently obtained in the ICU setting through right heart catheterization, an invasive method. This kind of procedure brings with it increased financial cost and risk to the patient. Consequently, non-invasive methods, such as ballistocardiography (BCG), have been gaining more traction and are seen as potential candidates for measuring cardiovascular parameters such as CO.

BCG utilizes detection of the body’s recoil from the ejection of blood into the arterial system. Due to its nature, BCG is prone to noise and ensemble averaging of multiple cardiac cycles is used to obtain a waveform with higher signal-to-noise ratio. An electrocardiogram (ECG) handlebar is used to generate the ECG waveform that sets the timing of the cardiac cycles for this technique. The most notable features of the BCG waveform (I, J, and K waves) are driven by the difference in blood pressure between the inlet and outlet of the ascending aorta during a cardiac cycle. Several parameters derived from these features in the waveform, such as I-J amplitude, IJK width, and the R-J interval, can be used to determine a patient’s stroke volume. Once the stroke volume is known, it can be used alongside the heart rate to calculate the cardiac output. This kind of device can be used for continuous monitoring of a patient in the home setting, removing many of the limitations seen with invasive methods.

Further Reading

Continuous and Non-invasive Arterial Pressure Waveform Monitoring using Ultrasound

J. Seo, H.-S. Lee, C. G. Sodini
Sponsorship: MEDRC – Philips, CICS

An arterial blood pressure (ABP) waveform provides valuable information for understanding cardiovascular diseases. The ABP waveform is usually obtained through an arterial line (A-line) in intensive care settings. Although considered the gold standard, the disadvantage of this method is its invasive nature. Non-invasive methods such as vascular unloading and tonometry are not suitable for prolonged monitoring. Therefore, reliable non-invasive ABP waveform estimation has long been desired by medical communities. Medical ultrasound is an attractive imaging modality because it is inexpensive, cuff-less, and suitable for portable system implementation.

The proposed ultrasonic ABP waveform monitoring is achieved by ultrasonography to observe the pulsatile change of the cross-sectional area and identify the vessel elasticity, represented by the pulse wave velocity (PWV); the propagation speed of a pressure wave along an arterial tree) with a diastolic pressure measurement. The local PWV can be estimated from the flow-area plot during a reflection-free period (e.g., the early systolic stage).

A prototype ultrasound device was designed to conduct application-specific ultrasonography in a portable form factor, shown in Figure 1. The first human subject validation shows the agreement between this method on the common carotid artery and the ABP waveform obtained at a middle finger using the vascular unloading method. Motion-tolerant ultrasonography is explored to improve the measurement stability from the first design for long term monitoring. The second human subject study in a transient stress situation demonstrates the proof-of-concept of this method for the stress testing. Currently, the human subject study to compare the A-line with this method in collaboration with Boston Medical Center is in progress.

FURTHER READING


▲ Figure 1: The prototype ultrasound system and transducer assembly. The system is capable of sufficient data rate to display blood flow and arterial pulsation simultaneously. Ultrasound gel pad is utilized to achieve acoustic coupling between the transducer surface and the skin.

▲ Figure 2: Application of the probe for motion-tolerant ultrasonography. This probe is manually held or secured by rubber bands around the subjects’ neck for the human study in a transient stress situation.
Skin electronics, which can laminate on human skin, have emerged as essential tools for human/Internet of things (IoTs) interfaces such as real-time health monitoring and instantaneous medical treatment. Amid this sweeping trend, human skin has been treated as merely a flexible, stretchable, and soft space for mounting of skin electronic devices. The skin is the outmost and the largest organ covering the external body surface and plays a vital role to maintain human life. Thus, homeostasis of the skin should be maintained even beneath the electronics. However, conventional thin-film device design, neglecting the skin, can induce problems (e.g., inflammation).

Here we propose a breathable skin electronics, not blocking physiological activity of the skin. Sweat pore-inspired micro-hole pattern in a skin patch secure ~100% breathability and an elastic modulus of the skin patch has comparable value of the skin, which can replicate mechanical deformation of the skin with strong adhesion.

Furthermore, we develop all-in-one device transfer process that high-temperature processed (~500 °C), photo-patterned inorganic device array is directly transferred onto the skin patch (Figure 1). High-quality inorganic semiconductors on skin-like patch lead to highly sensitive electromechanical devices such as strain sensors (Figure 2).
Secure System for Implantable Drug Delivery

S. Maji, U. Banerjee, R. T. Yazicigil, S. H. Fuller, A. P. Chandrakasan
Sponsorship: Analog Devices, Inc., Fellowship

Recent years have witnessed a growing increase in the use of implantable and wearable medical devices for monitoring, diagnosing, and treating our medical conditions. Advancements in electronics have opened up new avenues for deploying these devices towards applications previously overlooked, such as implanting an entire repository of medical drugs within the human body for effective time-released delivery. The advantages of a time-released implant offer over some conventional oral dosage forms are site-specific drug administration for targeted action, minimal side-effects, and sustained release of therapeutic agent. Patient compliance is more positive with the treatment regimen associated with an implantable device as it is considerably less burdensome than pills or injections. The prominent application for implantable drug delivery includes diabetes management, contraception, HIV/AIDS prevention, and chronic pain management.

In many of these applications, the control of the command to these devices lies with the patient, who can program the device as needed. For example, a woman can program her monthly schedule of contraception for her family planning and allow the device to release regular doses of contraception, alleviating daily doses. However, an alarming concern that is associated with it is the generic security concerns with regular IoT devices, and potentially, with much more catastrophic effects. Any compromise of the controller device/cell phone would render the system ineffective. The fact that there is no direct feedback from the implantable to the patient makes it even more difficult. A simple example is a malicious cell-phone continuously commanding the device to release drug without the knowledge of patient.

Our work focusses on solving this problem with a combination of energy-efficient cryptography with relevant physiological properties of the user. This makes it very difficult for any attacker, even with significant control over the controller, to break the system, while providing legitimate feedback to the user.

▲Figure 1: A generic diagram of an implantable drug delivery system involving all the parties.

▲Figure 2: Components of the proposed secure implantable drug delivery system.

FURTHER READING
Quantitative and accurate tracking of neurodegenerative disease remains an ongoing challenge. Diagnosis requires patients to undergo time-consuming neuropsychological tests that suffer from high-retest variability, making it difficult to assess the progression of the disease or a patient’s response to experimental treatments.

We tackle the lack of an objective measurement to track the progression of neurodegenerative diseases by designing algorithms that can quantify subtle changes across time in eye movement patterns that correlate with disease progression. One such feature is saccade latency – the time delay between the appearance of a visual stimulus and when the eye starts to move towards said stimulus. As a result, an unobtrusive tool that measures saccade latency (or other metrics of eye movement) consistently across time can enable the quantification of disease progression and the assessment of a patient’s response to treatment.

We propose a pipeline (Figure 1) to modify and evaluate a set of candidate eye-tracking algorithms to operate on video sequences obtained from an iPhone 6, for accurate and robust determination of saccade latency. A variant of the iTracker algorithm performed most robustly and resulted in mean saccade latencies and associated standard deviations on iPhone recordings that were essentially the same as those obtained from recordings using a high-end, high-speed camera (Figure 2). Our results suggest that accurate and robust saccade latency determination is feasible using consumer-grade cameras and might, therefore, enable unobtrusive tracking of neurodegenerative disease progression.

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In a conventional pipelined ADC, the input signal is sampled upfront as shown in Figure 1. Any jitter in the sampling clock directly affects the sampled input and degrades the signal-to-noise ratio (SNR). Therefore, for fast varying input signals, the sampling jitter severely limits the SNR. The error in sampled voltage due to clock jitter is

\[ \Delta v = (dv/dt) \cdot \Delta t \]

where \( dv/dt \) is the time-derivative of the input signal at the sampling instant and \( \Delta t \) is the jitter in the sampling clock. Since the sampling clock jitter is random, it introduces a random noise in the sampled input signal. Also, the error voltage is proportional to \( dv/dt \) and hence to the amplitude and frequency of the input signal. Thus, as the frequency of the input signal increases, the effect of sampling clock jitter becomes more pronounced. In fact, it can be shown that for a known rms sampling jitter \( \sigma_t \), the maximum SNR is limited to

\[ \text{SNR}_{\text{max}} = \frac{1}{2\pi f_{\text{in}} \sigma_t} \]

where \( f_{\text{in}} \) is the input signal frequency. Typically, it is difficult to reduce the rms jitter below 100 fs. This limits the maximum SNR to just 44 dB (which is equivalent to 7 bits) for a 10 GHz signal. Therefore, unless the effect of sampling jitter is reduced, the performance of an ADC would be greatly limited for high frequency input signals.

It has been shown that continuous-time delta-sigma modulators (CTDSM) reduce the effect of sampling jitter. But since CTDSMs rely on oversampling, they are not suitable for high frequency signals. Therefore it is imperative to develop sampling jitter-tolerant architectures for Nyquist-rate data converters.

In this project, we propose a new topology that provides increased tolerance to sampling jitter. At present, we are designing the pipelined ADC in 16-nm CMOS technology to give a proof-of-concept for tolerance to sampling jitter.

**FURTHER READING**

A Pipelined ADC with Relaxed Op-amp Performance Requirements

T. Jeong, A. P. Chandrakasan, H.-S. Lee
Sponsorship: CICS, STMicroelectronics, Korea Foundation for Advanced Studies

Among various analog to digital converter (ADC) architectures, pipelined ADCs are well suited for applications that need medium to high resolution above hundreds-of-megahertz sampling rate. To obtain good linearity, conventional pipelined ADCs must minimize multiplying digital to analog converter (MDAC) charge-transfer error by employing high-gain, fast-settling op-amps. However, such an op-amp design has become increasingly difficult due to the reduced intrinsic gain and voltage headroom in a fine-line CMOS technology. With low intrinsic gain devices, either a gain-boosting technique or a multi-stage topology is necessary to make the op-amp meet the gain requirement. Decreased power supply demands a larger capacitance to maintain the same level of SNR. As a result, the power consumption of these op-amps becomes prohibitively large.

Op-amp non-idealities have been removed or relaxed in digital domain by taking advantage of digital computation to address this issue. In this project, we propose a digital calibration scheme for op-amp-based pipelined ADCs. The ADC relaxes first stage op-amp performance requirements by using a shadow ADC and a simple digital domain calibration algorithm. To validate the functionality of the proposed calibration technique, a proof-of-concept ADC has been designed in 28nm CMOS technology and is currently being tested.

FURTHER READING


▲ Figure 1: Concept View of Proposed Calibration.
Data-dependent Successive-Approximation-Register Analog-to-Digital Converter

H. S. Khurana, A. P. Chandrakasan, H.-S. Lee
Sponsorship: CICS

This work on successive-approximation-register (SAR) analog-to-digital converters (ADCs) (Figure 1) aims at improving data-dependent savings in energy in key components of a SAR ADC by leveraging the information available from signal’s immediate past samples and the signal type. The dominant energy consuming components are the digital-to-analog converter (DAC) and the comparator.

Energy expenditure in the DAC per sample conversion depends on the DAC topology and sequence of steps taken during successive approximation. Energy in the comparator is directly proportional to the number of comparisons done per sample conversion. A design with data-dependent savings takes advantage of the correlation between successive samples in completing the conversion in fewer bit-cycles and also operates the DAC more energy-efficiently.

Previous work presented data-dependent savings by doing least-significant-bit (LSB)-first successive approximation to convert an input sample. By starting with a previous sample and using LSB-first, the algorithm converges in a fewer number of cycles than conventional most-significant-bit (MSB)-first SAR conversion when the present signal is close to the previous signal. Fewer cycles translate into energy savings in the comparator and the DAC. Another work developed successive approximation algorithms to find a sub-range from the full range in a few cycles before carrying on a binary search in this small range. In this work, we investigate a SAR ADC with a search algorithm based on the statistical characteristics of the signal for optimum energy expenditure.

FURTHER READING

Analog-to-digital converters (ADCs) often limit the performance of integrated systems for emerging applications such as next-generation communication systems, data centers, and quantum computing. The ADC performance is, in turn, limited at least partly by a track-and-hold sampling circuit (THSC). The low supply voltage of deeply scaled complementary metal-oxide-semiconductor (CMOS) transistors determines the THSC input signal range, therefore becoming a fundamental upper bound to the effective number of bits (ENOBs) of CMOS ADCs.

This research work envisions to realize THSCs in GaN-on-Si technology, which monolithically integrates GaN high-electron-mobility transistors (HEMTs) with Si-CMOS transistors, for future ultrahigh-performance ADCs. Operating GaN HEMTs at a high voltage (>30 V) allows a very large input swing (>16 V), providing signal-to-noise ratio (SNR) performance orders of magnitudes beyond the limit of CMOS THSCs. We designed and implemented two GaN HEMT THSCs. The first THSC was fabricated in a commercial GaN foundry technology on SiC substrate, providing 98-dB SNR at 200 MS/s. The second THSC design was fabricated in a GaN technology that was developed at MTL on Si substrate, which operates at 1 GS/s thanks to a higher current-gain cutoff frequency $f_T$ and external gate-bootstrapping clock (Figure 1). While these GaN HEMT THSCs achieved an unprecedentedly high SNR at a given input frequency, they suffer from dynamic nonlinearity from the GaN HEMT source-follower buffers for gate-bootstrapping sampling clock generation. Although dynamic nonlinearity correction techniques are mature with RF power amplifiers (PAs), these conventional pre-distortion techniques have high sensitivity to DC offsets, and thus, cannot be directly applied to GaN HEMT THSCs.

To overcome this challenge, we are developing a digital post-correction (DPC) technique, which will demonstrate improved linearity of GaN HEMT THSCs without using a dedicated reference ADC. By applying a DPC technique based on modified Volterra series (Figure 2), we have recently demonstrated that THSC linearity can be improved by more than 20 dB. We are presently working to enhance the linearization performance by applying advanced DPC techniques.

**FURTHER READING**

GaN Circuit-device Interaction in Fully Integrated RF Power Amplifiers

P. Choi, U. Radhakrishna, D. A. Antoniadis, E. A. Fitzgerald

Sponsorship: SMART LEES

Highly integrated GaN RF power amplifiers (PAs) have been developed for mobile devices and connected cars applications using the physics-based RF transistor compact model, MIT Virtual Source GANFET (MVSG). RF power amplifiers are required to operate in a linear region to prevent signal distortion and resultant data loss, which is mainly affected by inherent device-level nonlinear behavior. Since the second derivative of transconductance, \( g_3 \), is an intrinsic source of intermodulation distortion, many studies aimed to cancel it, especially in CMOS technology. However, the high mobility and thermal effect of GaN devices make the device nonlinearity compensation harder than in CMOS devices. Thus, we have looked into the large signal linearization considering both power gain and third-order harmonics rather than \( g_3 \) alteration techniques that cannot be properly functional in a high-power amplifier with large signal input.

In our previous design, the Class-AB + Class-C configuration was proposed for a fully integrated GaN RF amplifier, demonstrating improved linearity and efficiency. Recently, we designed another GaN RF power amplifier with the Common-Source & Common Gate (CS-CG) configuration to further improve the intermodulation distortion by optimizing the third order harmonics performance from the viewpoint of compensating for the large signal distortion. The CS-CG outperforms the Class-AB + Class-C in terms of the third order harmonics and intermodulation distortion, which means that the average time-varying composite \( g_3 \) of the CS–CG is lower than that of the Class-AB + Class-C.

To study the impact of the device and technology parameters on the circuit performance, we used both the MVSG model and the CS-CG amplifier and isolated some device parameters which affect the DC and RF performance at both device and circuit levels. Figure 1 shows the circuit implementation using 0.25μm GaN technology and its gain and third-order harmonics with varying DIBL, \( \delta \). Intermodulation distortion is further investigated with varying \( \delta \), short channel effects such as moderate punch-through, \( n_d \), and parasitics, i.e., \( C_{ds} \) and \( C_{dg} \), as depicted in Figure 2.

**Figure 1:** (a) The CS-CG RF PA, (b) DIBL, \( \delta \), changes the threshold voltage as a function of \( V_{ds} \) and thus makes the circuit behave in a different class, which also affects the composite gain and harmonics output of the CS-CG RF PA.

**Figure 2:** Two-tone intermodulation simulation with varying parameters - \( \delta \), \( n_d \), and parasitics, i.e., \( C_{ds} \) and \( C_{dg} \).

**FURTHER READING**

Cryptographically Secure Ultra-fast Bit-level Frequency Hopping for Next-generation Wireless Communications

R. T. Yazicigil, P. Nadeau, D. Richman, C. Juvekar, K. Vaidya, A. P. Chandrakasan
Sponsorship: Hong Kong Innovation and Technology Fund, Texas Instruments, NSF, TSMC

Current Internet-of-Things devices communicate via Bluetooth Low Energy (BLE). Unfortunately, BLE-connected devices are vulnerable to a wide range of attacks; this work specifically addresses selective jamming denial of service where the adversary corrupts transmitted messages targeting a single victim. Selective jamming is particularly challenging as it conceals the attacker's identity contrary to broadband-wireless jamming. To illustrate this type of attack, we demonstrate selective jamming against a commercial fitness BLE-device as shown in Figure 1. This form of attack can cause serious harm such as in the case of insulin pump medical devices.

The primary vulnerability of BLE is founded in the communication protocol which uses frequency hopping to send a message, which is decomposed into data packets, over rapidly changing sub-frequencies. The carrier frequency hops among these sub-frequencies at a relatively slow rate of 612µs per data packet (Figure 2). Conversely, an attacker needs only 1µs to identify the carrier frequency, then block the remainder of the data packet sent on that sub-frequency. To counter this attack, we developed physical-layer security through an ultra-fast bit-level frequency hopping scheme which sends every data bit on a unique carrier frequency while achieving a 1µs hop period (Figure 2).

In addition, a challenging issue is that traditional modulation schemes, such as the BLE Gaussian frequency shift keying (GFSK) modulation with fixed carrier offset of ± 250kHz for Bit 1 and Bit 0, permit the attacker to selectively overwrite individual bits in a packet once the carrier frequency is localized. The attacker gains control over the packet that will be received by the victim. We protect against this attack by implementing a cryptographically secure data-driven dynamic channel selection scheme that enables 80-way pseudorandom FSK modulation and provides data encryption in the physical layer.

In this work, we demonstrated the first integrated bit-level frequency-hopping transmitter that hops at 1µs period and uses data-driven random dynamic channel selection to enable secure wireless communications with data encryption in the physical layer.

FURTHER READING

A Dense 240-GHz 4×8 Heterodyne Receiving Array on 65-nm CMOS Featuring Decentralized Generation of Coherent Local Oscillation Signal

Z. Hu, C. Wang, R. Han
Sponsorship: TSMC, MIT-SMART, NSF

There is a growing interest in pushing the frequency of beam-steering systems towards terahertz range, in which case narrow-beam response can be realized at chip scale. However, this calls for disruptive changes to traditional terahertz receiver architectures, e.g., square-law direct detector arrays (low sensitivity and no phase information preserved) and small heterodyne mixer arrays (bulky and not scalable). In the latter case, corporate feed for generating and distributing the local oscillation signals (LO)—typically a necessary component—can be very lossy at large scale. Here, we report a highly scalable 240-GHz 4×8 heterodyne array achieved by replacing the LO corporate feed with a network that couples LOs generated locally at each unit. A major challenge for this architecture is that each unit should fit into a tight $\lambda/2 \times \lambda/2$ area to suppress side lobes in beamforming, making the integration of the mixer, local oscillator, and antenna into a unit extremely difficult. This challenge is well-addressed in our design. We have built highly-compact units, which ultimately enables the integration of two interleaved 4×4 phase-locked sub-arrays in 1.2-mm².

The schematic of the circuit of one unit is shown in Figure 1(a). Its core component is a self-oscillating harmonic mixer (SOHM), which can simultaneously (1) generate high-power LO signal and (2) down-mix the radio frequency (RF) signal. The SOHM is connected to both an intra-unit slot antenna (TL₁ and TL₂) for RF receiving and a co-planar waveguide (CPW)/slotline mesh (TL₃) for strong LO coupling with neighboring SOHMs. Owing to the coupling, LOs generated in each unit can be all locked to an external reference signal so that the array is coherent. Die photo showing the placement of the array and the PLL is given in Figure 1(b). Measured spectrum of 4.6-MHz (below the noise corner frequency) baseband signal is shown in Figure 2, from which we obtain a sensitivity (required incident RF power to achieve SNR=1 at baseband) over 1-kHz detection bandwidth of 38.8pW – more than 6× improvement over state-of-the-art large-scale homodyne arrays.

FURTHER READING

Low-cost 3-D imaging recently becomes increasingly attractive because of its enormous potential in security applications. In particular, waves in the low terahertz (THz) range provide powerful capabilities for 3-D imaging due to the large available bandwidth and improved angular resolution (compared with radio frequency and mm-wave signals), and good transmission (<0.01 dB/m) through extreme weather conditions (compared with infrared and visible light).

We propose a comb radar architecture to increase the bandwidth to more than 0.1 THz without using ultra-wideband components. Shown in Figure 1, it utilizes equally-spaced signal tones with frequency modulation; the generated IF signals are then combined in the digital domain. The proposed comb radar architecture has many advantages compared with conventional Frequency-Modulated Continuous-Wave (FMCW) radar in silicon: peak performance is maintained across a large bandwidth, finer Doppler frequency resolution, larger intermediate frequency (thus smaller flicker noise) and higher linearity. Similar to our previous frequency-comb-based THz spectrometer, in this radar, all components including antennas can be integrated on a single chip, our solution has merits of low cost, small volume, and lightweight.

Figure 2 shows the architecture of the proposed comb radar. It consists of multiple channels with a suitable bandwidth in each channel, leading to an aggregated bandwidth that is larger than 0.1 THz. Note that the number of channels is not limited by the architecture, so the aggregated bandwidth is only limited by the bandwidth of a single channel. The FMCW signal is fed into the first channel directly and up-converted through single sideband mixers to the subsequence channels step by step. The transmitter and the receiver share one on-chip antenna to save the area and power. The mixer first receiver utilizes the transmit power as local oscillator signal and down-converts the received echo signal to IF for further image processing. In addition, since backside radiation has asymmetric radiation pattern and multiple reflections in the attached silicon lens, front-side radiation is desired. To this end, we adopt a substrate-integrated-waveguide antenna utilizing its multiple high-order resonance modes in orthogonal directions. Compared with patch antenna, the new on-chip antenna design has much wider bandwidth (>10% fractional bandwidth).

FURTHER READING
Nitrogen-vacancy (NV) centers in diamond have attracted attention for spin-based quantum sensing in ambient conditions. They have demonstrated outstanding nanoscale sensing and imaging capabilities for magnetic fields. However, these sensing systems require many discrete devices to operate. This limits their scalability. In this work, we demonstrate a chip-scale CMOS and NV integrated platform for magnetic field sensing. The CMOS chip performs the required spin manipulation and read-out functions for NV sensing protocols.

Magnetic field sensing is accomplished by determining the spin states of the NV. The frequency of the spin states is determined by through optically detected magnetic resonance (ODMR). The magnetic field is proportional to the frequency splitting of the spin states (2.8 MHz/Gauss). Our system has an on-chip microwave (MW) signal generator, operating from 2.6 GHz to 3 GHz. In addition, an on-chip coil with parasitic loops radiates the AC magnetic field with an amplitude up to 10 Gauss with 95% uniformity over 50 µm x 50 µm. This MW radiation efficiently manipulates the NV spin ensembles. This is followed by on-chip optical readout of the spin state. A CMOS-compatible metal-dielectric structure filters out the optical pump (532 nm) with an isolation of 10 dB. An on-chip patterned P+/N-Well photodiode, beneath the MW coil and the filter, detects the NV red fluorescence. This photodiode is patterned to reduce the unwanted coupling to the MW coil. The measured photodiode responsivity is 230mA/W. The proposed system opens the door for a highly integrated quantum system with applications in the life sciences, tracking, and advanced metrology.

FURTHER READING

An Energy-efficient Reconfigurable DTLS Cryptographic Engine for End-to-End Security in IoT Applications

U. Banerjee, C. Juvekar, A. Wright, Arvind, A. P. Chandrakasan
Sponsorship: Texas Instruments, Qualcomm Innovation Fellowship

End-to-end security protocols, like Datagram Transport Layer Security (DTLS), enable the establishment of mutually authenticated confidential channels between edge nodes and the cloud, even in the presence of untrusted and potentially malicious network infrastructure. While this makes DTLS an ideal solution for IoT, the associated computational cost makes software-only implementations prohibitively expensive for resource-constrained embedded devices. We address this challenge through the design of energy-efficient hardware to accelerate the DTLS protocol along with associated cryptographic computations.

Figure 1 shows a block diagram of our system, which consists of a 3-stage RISC-V processor, a memory-mapped DTLS engine supporting the AES-128 GCM, SHA-256, and prime curve elliptic curve cryptography (ECC) primitives. We demonstrate hardware-accelerated DTLS which is 438x more energy-efficient and 518x faster than software implementations. The use of dedicated hardware for DTLS also reduces code size by 78KB and data memory usage by 20KB, thus increasing processor resources available to the application stack.

The test chip, shown in Figure 2, was fabricated in a 65nm LP CMOS process, and it supports voltage scaling from 1.2V down to 0.8V. The RISC-V processor achieves 0.96DMIPS/MHz, consuming 40.36μW/MHz at 0.8V. The DTLS engine consumes 44.08μJ per DTLS handshake, and 0.89nJ per byte of application data, both at 0.8V. Therefore, through the design of reconfigurable energy-efficient cryptographic accelerators and a dedicated protocol controller, this work makes DTLS a practical solution for implementing end-to-end security on resource-constrained IoT devices.

FURTHER READING

Ultra-Low-Power, High-sensitivity Secure Wake-up Transceiver for the Internet of Things

M. R. Abdelhamid, A. Paidimarri, A. P. Chandrakasan
Sponsorship: Delta Electronics

The Internet of Things (IoT) connects together an exponentially growing number of devices with an estimate of more than 70 billion devices in less than ten years from now. Such devices revolutionize the personal heart monitoring, home automation, as well as the industrial monitoring systems. Unfortunately, the wireless IoT nodes consume a huge portion of their energy on communicating with other devices. On the other hand, a longer battery lifetime or even a batteryless energy-harvesting operation requires a sub-microwatt consumption without significant performance degradation. In this work, we propose protocol optimizations as well as circuit-level techniques in the design of a -80dBm sensitivity ultra-low power wake-up receiver for on-demand communication with IoT nodes.

Wireless protocols such as Bluetooth low-energy (BLE) are optimized for short-length packets with small preambles and reduced header sizes. However, the power consumption of a low duty-cycled node in the default connected-mode is limited by the periodic beacons dictated by the protocol. Commercial BLE chips are then limited to tens of microwatts even though their standby power is in the nanowatt range. This wake-up receiver exploits the lower limit of the standby power to achieve significant power reduction through a wake-up scheme wrapped around the BLE advertising protocol. The receiver, shown in Figure 1, employs such duty-cycled wake-up scheme to mitigate the power/sensitivity trade-off achieving sub-microwatt average power at the required BLE sensitivity. When the receiver decodes its wake-up pattern inside the BLE advertising packet, depicted in Figure 2, it generates a wake-up signal then reconfigures its correlator with a new pattern. Figure 3 illustrates the power/latency trade-off where a user with a commercial app can use a cellphone to wake any sleeping IoT node up using the BLE standard according to the application at hand.

FURTHER READING

Contactless Current Sensing for Industrial IoT

P. Garcha, B. Haroun, S. Ramaswamy, V. Schaffer, D. Buss, J. Lang, A. P. Chandrakasan
Sponsorship: Texas Instruments

The ability to sense current is crucial to many industrial applications including power line monitoring, motor controllers, battery fuel gauges, etc. We are developing smart connectors with current sensing abilities for use in the industrial internet of things (IoT). These connectors can be used for 1) power quality management: to measure real power, reactive power, and distortion, and 2) machine health monitoring applications for continuous monitoring, control, prevention, and diagnosis. At the system level, the smart connectors need to 1) measure AC, DC, and multiphase currents, 2) reject stray magnetic fields, and 3) detect impending connector failure. On the sensor level, they need to provide high measurement bandwidth (BW) and low power operation.

Current can be sensed directly by using a shunt resistor, but it leads to large power dissipation for measuring high current levels (10-100 A). Indirect/contactless sensing, which senses the magnetic field strength, is a better option as it offers galvanic isolation and the ability to operate safely in high voltage applications. Examples of contactless current sensors include Hall, magneto-resistive (MR), and fluxgate (FG) sensors. FG sensors with integrated magnetics offer higher sensitivity than Hall sensors (nT vs. μT) and higher linearity and lower offset hysteresis than MR sensors, making them a good choice for industrial current sensing.

The proposed system consists of a central processor and multiple low-power, high-BW FG sensors to make synchronous measurements (Figure 1). The measured data from all sensors is stored on the central processor, which runs preliminary analytics on the data before sending it to the cloud. Figure 2 shows the workings of a basic fluxgate sensor design. The proposed sensor makes use of various power saving techniques to reduce the energy per measurement, as well as digitally assisted analog circuits to push for high BW and BW scalability with duty cycling, from >100 kHz BW for machine health monitoring to <1 kHz for power quality management.

FURTHER READING

Drones are getting increasingly popular nowadays. Nanodrones specifically are easily portable and can fit in your pocket. Equipped with multiple sensors, the drone functionality is getting more powerful and smart (e.g., track objects, build 3-D maps, etc.). These capabilities can be enabled by powerful computing platforms (CPUs and GPUs), which consume a lot of energy. The size and battery limitations of Nanodrones make it prohibitive to deploy.

This work presents Navion, an energy-efficient accelerator for visual-inertial odometry (VIO) that enables autonomous navigation of miniaturized robots, and augmented reality on portable devices. The chip fuses inertial measurements and mono/stereo images to estimate the camera’s trajectory and a sparse 3-D map. VIO implementation requires large irregularly structured memories and heterogeneous computation flow. The entire VIO system is fully integrated on-chip to eliminate costly off-chip processing and storage. This work uses compression and exploits structured and unstructured sparsity to reduce on-chip memory size by 4.1x. Navion is fabricated in 65nm CMOS. It can process 752x480 stereo images at 171 fps and inertial measurements at 52 kHz, consuming an average 24mW. It is configurable for maximizing accuracy, throughput, and energy-efficiency across different environments. This is the first fully integrated VIO in an ASIC.

**FURTHER READING**

Unmanned Autonomous Vehicles (UAV) have received wide attention. Their capability to autonomously navigate around the environment enables many applications including search-and-rescue, surveillance, wildlife protection, and environment mapping. The key technique to empower such capabilities is the frontier-exploration algorithm, which periodically makes decisions on where the vehicle should explore next in an unknown environment based on previously acquired knowledge. However, such algorithms are computationally expensive. In a practical system, the computation is usually offloaded to a powerful computer, causing a significant delay in the response time. This also makes the system strongly dependent on the presence of a stable wireless connection. These factors prohibit the application of the frontier-exploration algorithm to resource-constrained miniature UAVs with limited battery and computation power.

In this work, we present an algorithm to reduce the computation cost of the state-of-the-art mutual information based frontier-exploration algorithm. The key idea behind the algorithm is to use the same computations between different parts of the mutual information computation and reduce redundant computations. Additionally, our approach seeks a more compact representation of the environment, which minimizes the number of operations required to run the algorithm.

In practice, our algorithm enables the complicated frontier-exploration algorithm to be deployed to a battery-powered miniature UAVs with limited computation power. The algorithm makes it possible for the UAV to explore a closed unknown environment with no stable wireless connections. Thanks to the capability of local computation, the latency of running the algorithm is reduced, enabling the UAVs to explore faster and quickly react to the changes in the environment. The saved computation power can be allocated to the actuators of the UAV, enabling the UAVs to stay in the air longer and therefore explore a larger area given fixed power budget.

FURTHER READING

Efficient Processing for Deep Neural Networks

Y.-H. Chen, T.-J. Yang, Y. N. Wu, J. Emer, V. Sze
Sponsorship: DARPA YFA, MIT CICS, Intel, Nvidia

Artificial Intelligence powered by deep neural networks (DNNs) has shown great potential to be applied to a wide range of industry sectors. Due to DNNs’ high computational complexity, energy efficiency has ever-increasing importance in the design of future DNN processing systems. However, there is currently no standard to follow for DNN processing; the fast-moving pace in new DNN algorithm and application development also requires the hardware to stay highly flexible for different configurations. These factors open up a large design space of potential solutions with optimized efficiency; and a systematic approach becomes crucial.

To solve this problem, we address the co-optimization among the three most important pillars in the design of DNN processing systems: architecture, algorithm, and implementation. First, we present Eyeriss, a fabricated chip that implements a novel data flow architecture targeting energy-efficient data movement in the processing of DNNs (Figure 1). Second, we develop Energy-Aware Pruning (EAP), a new strategy of removing weights in the network to reduce computation so that it becomes more hardware-friendly and yields higher energy efficiency (Figure 2). Finally, we present a tool to realize fast exploration of the architecture design space under different implementation and algorithmic constraints.

FURTHER READING

Energy-efficient Deep Neural Network for Depth Prediction

D. Wofk, F. Ma, T.-J. Yang, S. Karaman, V. Sze
Sponsorship: Analog Devices, Inc.

Depth sensing and estimation is a key aspect of positional and navigational systems in autonomous vehicles and robots. The ability to accurately reconstruct a dense depth map of a surrounding environment from RGB imagery is necessary for successful obstacle detection and motion planning. Since deep convolutional neural networks (DNNs) have proven to be successful at achieving high accuracy rates in image classification and regression, recent work in the deep learning space has focused on designing neural networks for depth prediction applications. However, the high accuracy of DNN processing comes at the cost of high computational complexity and energy consumption, and most current DNN designs are unsuitable for low-power applications in miniaturized robots. In this project, we aim to address this gap by applying recently developed methodologies for estimating and improving the energy-efficiency of DNNs to an existing depth-prediction DNN. We envision an outcome in which the depth-prediction DNN is modified to be better suited for a specialized hardware implementation that could be integrated with a low-power visual-inertial odometry system to result in a combined navigational system for miniaturized robots.

Further Reading

Depth Estimation of Non-Rigid Objects for Time-of-Flight Imaging

J. Noraky, V. Sze
Sponsorship: Analog Devices, Inc.

Depth sensing is used in a variety of applications that range from augmented reality to robotics. Time-of-flight (TOF) cameras, which measure depth by emitting and measuring the roundtrip time of light, are appealing because they obtain dense depth measurements with minimal latency. However, as these sensors become prevalent, one disadvantage is that many TOF cameras in close proximity will interfere with one another, and techniques to mitigate this can lower the frame rate at which depth can be acquired. Previously, we proposed an algorithm that uses concurrently collected optical images to estimate the depth of rigid objects. Here, we consider the case of objects undergoing non-rigid deformations. We model these objects as locally rigid and use previous depth measurements along with the pixel-wise motion across the collected optical images to estimate the underlying 3-D scene motion, from which depth can then be obtained. In contrast to conventional techniques, our approach exploits previous depth measurements directly to estimate the pose, or the rotation and translation, of each point by finding the solution to a sparse linear system. We evaluate our technique on a RGB-D dataset where we estimate depth with a mean relative error of 0.58%, which outperforms other adapted techniques.

**FURTHER READING**
**Small-footprint Automatic Speech Recognition Circuit**

D.-C. Chueh, A. P. Chandrakasan  
Sponsorship: Foxconn Technology Group

With the advanced technology of speech and natural language processing, spoken language has become a feasible way for human-machine interaction. Due to the high complexity of articulated speech signal, automatic speech recognition (ASR) generally requires intensive computation and memory size to achieve good performance. However, due to its widespread applications on robots, wearables, and mobile devices, it’s desirable to design circuit to implement ASR locally in a resource-limited environment, particularly in which power consumption is a critical concern.

In this work, we first scrutinize software speech recognition procedure; evaluate the memory and computational resource needed when transferring to hardware, and take advantage of circuit design to minimize size and power usage. We design small-footprint ASR system (Figure 1) with cutting-edge neural network that can best perform acoustic modeling with memory restrictions, along with weight truncation and quantization. Dedicated arithmetic unit design, parallelization, and resource dispatching further reduce latency. We implement weighted finite-state transducer (WFST) to incorporate the phonetic probability with language model to select the best word transcription. Model compression, caching, and lattice truncation are adopted to adapt the ASR to circuit and optimize the design.

Our ASR design leveraging powerfulness and robustness of neural network in hybrid ASR model outperforms conventional model in recognition accuracy, whereas conducting ASR tasks on-chip sees great reduction in power compared to CPU. We show a 24X reduction in neural network weight size compared to previous hardware design. Our work demonstrates the feasibility to operate an ASR in a small-footprint environment in applications with small vocabulary size and optimized model.

![Figure 1: ASR chip design.](image)

**FURTHER READING**
Convolutional Neural Networks (CNN) have emerged to provide the best results in a wide variety of machine learning (ML) applications, ranging from image classification to speech recognition. However, they require huge amounts of computation and storage. When implemented in the conventional von-Neumann computing architecture, there is a lot of data movement per computation between the memory and the processing elements. This leads to a huge power consumption and long computation time, making CNNs unsuitable for many energy-constrained applications, e.g., smartphones, wearable devices, etc. To address these challenges, we propose embedding computation capability inside the memory (Figure 1). By doing that, we can significantly reduce data transfer to/from the memory and also access multiple memory addresses in parallel, to increase processing speed. The basic convolution operation in a CNN layer can be simplified to a dot-product between the layer inputs ($X$) and the filter weights ($w$), to generate the outputs ($Y$) for that layer. In this work, CNNs are trained to use binary filter weights ($w = +/-1$), which are stored as a digital ‘0’ or ‘1’ in bit-cells of the memory array. The digital inputs ($X$) are converted to analog voltages and sent to the array, where the dot-products are performed in the analog domain. Finally, the analog dot-product voltages are converted back into the digital domain outputs ($Y$) for further processing.

To demonstrate functionality for a real CNN architecture, the Modified National Institute of Standards and Technology (MNIST) handwritten digit recognition dataset is used with the LeNet-5 CNN (Figure 2). We demonstrated a classification accuracy of 98.35%, which is within 1% of what can be achieved with an ideal digital implementation. We achieved more than 16x improvement in the energy-efficiency in processing the dot-products vs. full-digital implementations. Thus our approach has the potential to enable low-power ubiquitous ML applications for smart devices in the Internet-of-Everything.

FURTHER READING

Reconfigurable Neural Network Accelerator using 3-D Stacked Memory Supporting Compressed Weights

W. Jung, A. Ji, A. P. Chandrakasan
Sponsorship: Taiwan Semiconductor Manufacturing Company (TSMC)

The recent success of machine learning, with the help of emerging techniques, such as convolutional neural networks, have been rapidly changing the way many traditional signal processing problems are being solved, including vision processing, speech recognition, and other prediction and optimization problems. However, neural networks require a large number of weight parameters and processing power that are difficult to accommodate efficiently using a normal CPU architecture. This necessitates dedicated on-chip solutions.

A major challenge in recent on-chip neural network processors is reducing the energy consumed by memory accesses, as the cost for data operations becomes relatively cheaper than the cost for data movement in recently advanced processes. One approach is to simply reduce the amount of data movement by using compression schemes (i.e., reducing the bit-width of weights and activations). Han, et al. develop a deep compression technique to non-uniformly quantize floating point weights to 4-bit values, without any loss of accuracy. This was further extended to quantizing to only 2-bit ternary weights. Another approach is to increase the memory capacity, for example with 3-D stacked memory, to reduce the required number of costly external DRAM accesses.

Our proposed design takes full advantage of these compression schemes by directly integrating the decompression within the processing element. In addition, the design can be reconfigured to perform more general fixed-point computations with variable bit-widths. Combining this with a closely integrated memory chip through 3-D stacking makes it possible to run large networks with less data movement to and from the external DRAM, resulting in improved energy efficiency compared to other implementations.

FURTHER READING

In the post-ImageNet era, computer vision and machine learning researchers are solving more complicated Artificial Intelligence (AI) problems using larger data sets driving the demand for more computation. However, we are in the post-Moore’s Law world where the amount of computation per unit cost and power is no longer increasing at its historic rate. This mismatch between supply and demand for computation highlights the need for co-designing efficient machine learning algorithms and domain-specific hardware architectures. By performing optimizations across the full stack from application through hardware, we improved the efficiency of deep learning through smaller model size, higher prediction accuracy, faster prediction speed, and lower power consumption.

Our approach starts by changing the algorithm, using “Deep Compression” that significantly reduces the number of parameters and computation requirements of deep learning models by pruning, trained quantization, and variable length coding. “Deep Compression” can reduce the model size by 18× to 49× without hurting the prediction accuracy. We also discovered that pruning and the sparsity constraint not only applies to model compression but also applies to regularization, and we proposed dense-sparse-dense training (DSD), which can improve the prediction accuracy for a wide range of machine learning tasks. To efficiently implement “Deep Compression” in hardware, we developed EIE, the “Efficient Inference Engine,” a domain-specific hardware accelerator that performs inference directly on the compressed model which significantly saves memory bandwidth. Taking advantage of the compressed model, and being able to deal with the irregular computation pattern efficiently, EIE improves the speed by 13× and energy efficiency by 3,400× over GPU.

Further Reading

# Electronic, Magnetic, Superconducting, and Neuromorphic Devices

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In future logic technology for the Internet of Things and mobile applications, reducing transistor power consumption is of paramount importance. Transistor technologies based on III-V materials are widely considered as a leading solution to lower power dissipation by enabling dramatic reductions in the transistor supply voltage. Vertical nanowire (VNW) transistor technology holds promise as the ultimately scalable device architecture.

In this work, we present the smallest vertical nanowire transistors of any kind in any semiconductor system. These devices are sub-10 nm diameter InGaAs VNW metal–oxide–semiconductor field-effect transistors (MOSFETs). They are fabricated by a top-down approach, using reactive ion etching, alcohol-based digital etch, and Ni alloyed contacts. A record ON current of 350 μA/μm at OFF current of 100 nA/μm and supply voltage of 0.5 V is obtained in a 7 nm diameter device. The same device exhibits a peak transconductance of 1.7 mS/μm and minimal subthreshold swing of 90 mV/dec at a drain voltage of 0.5 V. This yields the highest quality factor (defined as the ratio between transconductance and subthreshold swing) of 19 reported in vertical nanowire transistors. Excellent scaling behavior is observed with peak transconductance and ON current increasing as the diameter is shrunk down to 7 nm. The performance of our devices exceeds that of the best Si/Ge transistor by a factor of two at half the supply voltage.

FURTHER READING

10-nm Fin-Width InGaSb p-Channel FinFETs

W. Lu, J. A. del Alamo
Sponsorship: SRC, DTRA, KIST, Lam Research Corporation

Recently, III-V multi-gate MOSFETs have attracted great interest to replace silicon in future CMOS technology. This is due to III-V semiconductor’s outstanding carrier transport properties. Although impressive n-type transistors have been demonstrated on materials such as InAs and InGaAs, research in III-V p-channel devices is lagging. The antimonide system, such as InGaSb, has the highest hole mobility among all III-V compound semiconductors, and its hole mobility can be further improved by applying compressive strain. Therefore, InGaSb is regarded as one of the most promising semiconductors to replace p-channel Si MOSFETs.

FinFET is a nonplanar transistor in which the conducting channel sticks out of the wafer top in a similar way as the fin of a shark above the ocean surface. In a FinFET, the gate wraps around the fin helping to reduce leakage current when the device is OFF and mitigating short-channel effects. FinFET is the state of the art transistor architecture in current Si CMOS technology, and demonstration of III-V FinFETs is imperative.

In this work, we greatly advance the state-of-the-art of antimonide-based electronics by demonstrating deeply-scaled InGaSb p-channel FinFETs through a fully CMOS-compatible fabrication process. To achieve this, we have developed a novel antimonide-compatible digital etch technology, which has a consistent etch rate of 2 nm/cycle on InGaSb. It is the first demonstration of digital etch on InGaSb-based transistors of any kind. The new technologies enabled the first fabricated InGaSb FinFETs featuring fin widths down to 10 nm and gate lengths of 20 nm. Single fin transistors with fin width of 10 nm and channel height of 23 nm (aspect ratio of 2.3) have achieved a record transconductance of 160 μS/μm at $V_{DS} = 0.5$ V. When normalized to device footprint, we achieve a record transconductance of 704 μS/μm. Digital etch has been shown to effectively improve the turn-off characteristics of the devices.

This work not only highlights the potential of InGaSb p-channel multigate MOSFETs, but also pushes the state-of-the-art of antimonide fabrication technology significantly for general applications in which the antimonide-based compounds can shine.

**FURTHER READING**

InGaAs is a promising candidate as channel material for CMOS technologies beyond the 7 nm node. In this dimensional range, only high aspect-ratio (AR) 3-D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs FinFET prototypes have been demonstrated recently. However, as the fin width is scaled down to 10 nm, severe ON-current degradation is observed. The origin of this performance degradation is largely related to the quality of the high-K/semiconductor interface at the fin sidewalls. One of the key process technologies to improve the interface quality is digital etch (DE). DE is a self-limiting etching process that consists of dry oxidation of the semiconductor surface and wet etch of the oxide. This process allows for the accurately scaling down of the fin width and smoothing the sidewalls. Digital etch is also the last process step before the gate oxide is deposited over the fins. Therefore, plays a crucial role in surface preparation and holds the key for further improvements to device transport and electrostatics.

In this work, we compare the electrical performance of two identical sets of InGaAs FinFETs processed side-by-side that differ only in the type of digital etch that is applied. In one case, the oxide removal step was accomplished using H\textsubscript{2}SO\textsubscript{4}, in the other, HCl was used. The starting material consists of 50 nm thick (H\textsubscript{2}SO\textsubscript{4}) moderately-doped InGaAs channel layer on top of InAlAs buffer (both lattices matched to InP), as shown in Figure 1(a). Fins are first patterned using E-beam lithography and RIE etched. After this, four cycles of digital etch are applied. Then, the gate dielectric composed of 3 nm HfO\textsubscript{2} is deposited by Atomic Layer Deposition. and Mo is sputtered as gate metal and patterned by RIE. In this process, the HSQ that defines the fin etch is kept in place. This makes our FinFETs double-gate transistors with carrier modulation only on the fin sidewalls. The device is finished by via opening and ohmic contact and pad deposition. Transmission Electron Microscopy (Figure 1(b)) is used to verify that the fin shape and dimensions are similar in both samples. Well-behaved characteristics and good sidewall control are obtained in both types of devices. There are a few notable differences. In the OFF state, the HCl sample shows lower gate leakage but larger subthreshold swing compared to the H\textsubscript{2}SO\textsubscript{4} sample (Figure 2(a)). This suggests that HCl treatment results in a higher interface state density (D\textsubscript{it}) toward the valence band. In the ON state, however, the intrinsic transconductance, g\textsubscript{m,i}, exhibits a peculiar trend. For wide fins, the HCl sample shows higher performance but in very narrow fins (W<20 nm), H\textsubscript{2}SO\textsubscript{4} performs better (Figure 2(b)). This implies that HCl yields a higher mobility but lower carrier concentration at comparable overdrive. For aggressively scaled fins, the carrier concentration in the fin becomes comparable to D\textsubscript{it} and, as a result, the intrinsic g\textsubscript{m} of H\textsubscript{2}SO\textsubscript{4} sample (with a lower D\textsubscript{it} toward the conduction band) prevails.
InGaAs is a promising n-channel material candidate for future CMOS technology due to its superior electron transport properties and low voltage operation. Due to the lack of good native oxide, it has been challenging to achieve a high-quality gate stack, which includes the gate oxide as well as the oxide/semiconductor interface. Many have observed hysteresis and threshold voltage instability in InGaAs MOSFETs that are attributed to interface and oxide defects. In this work, we study the frequency dispersion of InGaAs MOSFETs, an important electrical parameter that is also affected by gate stack defects.

The InGaAs MOSFETs used in this study are fabricated in a contact-first, gate-last self-aligned manner. Figure 1 shows the device schematic. The intrinsic channel consists of 8 nm-thick In$_{0.7}$Ga$_{0.3}$As. The gate insulator is a 2.5 nm-thick HfO$_2$, deposited by Atomic Layer Deposition (ALD) at 250$^\circ$C. The gate metal Mo is 35 nm thick, deposited by evaporation.

These devices show state-of-the-art performance. We have carried out frequency-dependent electrical characterization from DC to 10 GHz. For the frequency range between 100 kHz and 10 MHz, we employ a lock-in setup and measure the AC drain current induced by AC gate voltage. For frequency range from 100 MHz to 10 GHz, the device S-parameters are measured using a vector network analyzer. From these measurements, we extract the intrinsic transconductance, $g_{m,i}$. Figure 2 (a) shows the frequency dispersion of the intrinsic transconductance ($g_{m,i}$) from DC to 10 GHz. As AC frequency increases, deep-level trap states can no longer respond, and device performance improves. $g_{m,i}$ increases from 775 mS/mm to 2200 mS/mm from DC to 10 GHz. The dispersion throughout the entire frequency range also indicates defect states with different time constants. It is remarkable how much unrealized intrinsic performance is left at DC. Figure 2 (b) shows peak $g_{m,i}$ at 10 GHz as a function of gate voltage. Here it is clear that the higher the gate voltage, the larger the gap between DC and 10 GHz $g_{m,i}$. At the highest $g_{m,i}$, the ratio is about a factor of 3.

In conclusion, we have found large frequency dispersion of intrinsic transconductance in InGaAs MOSFETs, leading to a compromised device performance at DC. Thus, it is important to mitigate the oxide and interface defects in order to unveil the intrinsic outstanding transport properties of InGaAs.

**FURTHER READING**

Vertical Gallium Nitride Power Transistors

Y. Zhang, M. Sun, T. Palacios
Sponsorship: ARPA-E SWITCHES

Lateral and vertical gallium nitride (GaN)-based devices are excellent candidates for next-generation power electronics. They are expected to significantly reduce the losses in power conversion circuits and enhance the power density. Vertical GaN devices can achieve higher breakdown voltage (BV) and handle higher current/power than lateral GaN devices and are therefore promising for high-voltage and high-power applications.

The development of vertical GaN power transistors has been hindered by the need to perform epitaxial regrowth or dope the layer p-type. The epitaxial regrowth greatly increases the complexity and cost of device fabrication. p-type GaN has low ratio for the acceptor activation, memory effects, and much lower carrier mobility compared to that in n-GaN.

We demonstrate a novel normally-off vertical GaN power transistor with submicron fin-shaped channels. This vertical fin transistor only needs n-GaN layers, with no requirement for epitaxial regrowth or p-GaN layers (Figure 1). A specific on-resistance of 0.2 mΩ-cm² and a BV over 1200 V have been demonstrated, with a threshold voltage of 1 V rendering normally-off operation (Figure 2). These results set a new record performance for 1200-V class power transistors and demonstrate the great potential of vertical GaN fin power transistors for high-power applications.

FURTHER READING

Vertical gallium nitride (GaN) devices are excellent candidates for next-generation power electronics. However, their commercialization has been hindered so far by the high cost and small diameter of GaN substrates. GaN vertical devices on low-cost silicon (Si) substrates are therefore highly desired, as they could allow for at least 50-to-100-fold lower wafer and epitaxy costs as well as the possibility of processing on 8-inch Si substrates. However, the insulating buffer layers typically found on GaN-on-Si wafers make it challenging to realize vertical current conduction.

Since 2014, we have developed three generations of vertical GaN-on-Si power diodes. The first generation utilized a quasi-vertical structure, where the anode and cathode are placed on a mesa step on the same wafer side (Figure 1(a)). We then demonstrated fully-vertical diodes by flip-chip-bonding the GaN-on-Si wafer to another Si wafer followed by the removal of insulating buffer layers. Recently, a novel technology was developed for making fully-vertical diodes (Figure 1(b)). Si substrate and buffer layers were selectively removed, and the bottom cathode was formed in the backside trenches. A specific differential on-resistance of 0.35 mΩ·cm² and a breakdown voltage of 720 V were both demonstrated (Figure 2), setting a new record performance in all vertical GaN power diodes on foreign substrates.

**FURTHER READING**

Stemming from their high breakdown voltages, large power densities, and high efficiency, GaN devices have quickly grown in popularity over the last two decades. With uses in millimeter wave applications like radar, satellite communication, and electronic warfare, the ever-increasing demand for high power devices that operate over large bandwidths requires that new transistor technology is created. Since vertical device dimensions and doping can be carefully controlled during wafer growth, a vertical design is ideal for RF devices which need short gate lengths. Moreover, by utilizing the vertical dimension, we can achieve excellent power density at millimeter-wave frequencies with minimal die area, and since most transport occurs through the bulk of the material, we also expect thermal management and reliability improvements when compared to the traditional GaN high electron mobility transistor (HEMTs). In this project, we adopt the design of recently developed vertical GaN transistors, which were initially optimized for high power applications, and modify them for improved RF performance.

Another important benefit of a vertical fin design is the ability for threshold voltage engineering. In RF devices, an important metric to non-linearity is $g_m''$ (the second derivative of device transconductance), which is ideally flat. One method for correcting this is through threshold voltage engineering where devices of varying VT are connected in parallel. Since shifting VT also shifts the peaks of $g_m''$, with careful design, the peaks of one transistor’s $g_m''$ can effectively cancel those of another when superimposed. The resultant device will then have a flatter transconductance response with improved RF performance. Through the fin-based design of the transistors in this project, the transconductance can be adjusted by simply altering the width of each fin, thus allowing for optimized large signal response for RF applications.

At MTL, we are fabricating the first vertical GaN fin RF transistors. For this, we are using electron beam lithography paired with a combination of dry and wet etching to achieve 100-300 nm tall fins with very smooth and vertical sidewalls. A molybdenum gate allows for a well-controlled etch-back process which coats only the sidewalls in metal. Further dry/wet etching can then be used to access the highly doped drain layer, which was defined during wafer growth. With the gate, source, and drain all on the top surface, this design will be compatible with GaN on Si technology, capable of significantly reducing material costs.

**FURTHER READING:**

Gallium nitride (GaN)-based transistors are very promising candidates for high power applications due to their high electron mobility and high electric breakdown field. Compared to conventional Si or GaAs based devices, wide bandgap GaN also has fundamental advantages for high-temperature applications thanks to their very low thermal carrier generation below 1000°C. However, in spite of the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN HEMTs could cause early degradation and failure under high-temperature operation (over 300°C). These include ohmic degradation, gate leakage, buffer leakage and poor passivation. In addition, to enable digital circuits, it is critical to have enhancement-mode HEMTs, while two-dimensional electron gas induced by AlGaN/GaN heterostructure makes HEMTs be natural depletion-mode devices.

In this work, we are developing a new GaN technology for high-temperature applications (>300°C). For this, we are first increasing the temperature stability of the ohmic contacts in GaN HEMTs, by combining a refractory metal such as tungsten (W) with Si-ion implantation, which locally dopes the material n-type and reduces the contact resistance. The schematic cross section is shown in Figure 1. An \( R_c \) of 0.8 \( \Omega \) mm, I\text{max} of 700 mA/mm were obtained with the W ohmic contacts in a transistor with a gate length of 4 \( \mu \)m. The W ohmic contacts were stable at least up to 300°C in air for at least 30 min, as seen in Figure 2, while conventional alloyed Ti/Al/Ni/Au ohmic contacts showed a strong temperature dependence and their contact resistance increased from 0.47 \( \Omega \) mm (RT) to 2.15 \( \Omega \) mm (300°C).

Gate injection transistors (GIT) have also been studied for enhancement-mode HEMTs. The structure used in this work had a 110nm extra p-GaN layer on 15nm Al\(_{0.2}\)Ga\(_{0.8}\)N barrier layer to fully deplete 2DEG under gate area. As shown in Ids-Vgs in Figure 3, a positive \( V_T \) around 3V was achieved, and their high-temperature stability is currently under investigation.
Novel GaN Transistor Design for High Linearity Applications
Q. Xie, U. Radhakrishna, T. Palacios
Sponsorship: DARPA DREaM, ONR PECASE

Enhancing the linearity of Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) is essential for future RF applications that require extremely low intermodulation distortion and gain compression. In this project, we have studied the origins of non-linearities in GaN-based amplifiers and propose device-level solutions to improve linearity. First, the drop in transconductance ($g_{m}$) at high current levels observed in GaN transistors can be mitigated with either self-aligned or finFET-like structures. This is due to the higher current-driving capability of the source access region on these devices. The second cause of device non-linearity has been linked to the large second derivative of the transconductance with respect to gate-source voltage ($V_{gs}$) ($g_{m}^{''}$). This can be overcome by using a new generation of engineered finFET transistors where the width of each fin is optimized for minimizing $g_{m}^{''}$.[3] In addition, the non-linear behavior of the device capacitances with operating voltage also plays a very important role in device non-linearities. In this case, too, nanostructures can be used to improve device performance. Finally, memory effects due to surface and buffer trap also contribute to non-linearities in amplifiers, and they can also be overcome through the use of nanostructures.

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**Figure 1:** Examples of 3-D device models used in TCAD simulations. (a) Full model; (b-d) FinFET with drain access region featuring the planar, straight fin, and tapered fin designs, respectively. “S”, “G”, and “D” represents the source, gate and drain electrodes, respectively. For clarity, the gate and passivation are hidden in (b-d).

**Figure 2:** Characteristics of FinFETs of varying fin widths. (a) Transfer curves; (b) $C_{gd}$ vs. $V_{G}$. The model simulated is illustrated in Fig. 1(a–b).

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**FURTHER READING**

Sub-micron p-Channel GaN Tri-gate MISFET
N. Chowdhury, T. Palacios

Remarkable attributes of GaN has led to the development of transistor technology for both power electronics and RF applications. Even though much attention is given to n-channel GaN transistor technology, p-channel GaN transistors still lack attention. Development of p-channel GaN transistors is a must to harness the full potential that GaN technology has to offer in achieving high-efficiency power conversion.

In this work, we have demonstrated for the first time sub-micron p-channel tri-gate MISFET with fin width of 200 nm. Figure 1(a) shows the schematic of fabricated device structure along with device dimensions. Figure 1(b) and 1(c) show the SEM image of the final device and the fins respectively. Because of the relatively thin AlGaN layer, the measurement results show significant electron contribution to the total drain current. However, if we deduct the current due to 2-DEG at the interface of AlGaN/GaN, we can extract the hole current. Figure 2 shows the IDS-VDS characteristics of the hole current. To prove that the current in Figure 2 predominantly is not because of the holes in the top p-GaN layer rather than the 2-DHG present at the GaN/AlGaN interface, we performed a low-temperature measurement. Because of relatively higher activation energy of Mg (~240 meV) in GaN, the p GaN layer is expected to be frozen out at around 77K leaving only the 2-DHG channel for the hole current. Figure 3 shows the hole current at 80K.

![Figure 1](image1.png)

**Figure 1:** (a) Schematic of 3-D device and device dimensions (b) SEM of final device (c) Fins after TMAH treatment.

![Figure 2](image2.png)

**Figure 2:** IDS-VDS characteristics due to hole current at room temperature.

![Figure 3](image3.png)

**Figure 3:** IDS-VDS characteristics due to hole current at 80K.
Reliability of GaN High Electron Mobility Transistors

B. Wang, W. A. Sasangka, G. J. Syaranamual, Y. Gao, R. I. Made, C. L. Gan, C. V. Thompson
Sponsorship: SMART

High electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures have been studied in literature for a variety of high-frequency and high-power applications. To minimize lattice mismatch and suppress defects generation, HEMTs, under study, are mostly fabricated on sapphire or SiC substrates. Currently, there is strong interest to fabricate GaN HEMTs on silicon substrates due to its low cost and compatibility with complementary metal–oxide–semiconductor (CMOS) integration technology. However, market adoption of this technology is still limited by the HEMT device reliability.

We have investigated the effects of Si$_x$N$_{1-x}$ passivation density on the reliability of AlGaN/GaN-on-Si HEMTs. Upon stressing, devices degrade in two stages: fast-mode degradation, followed by slow-mode degradation (Figure 1). Both degradations can be explained by different stages of pit formation at the gate edge. Fast-mode degradation is caused by pre-existing oxygen at Si$_x$N$_{1-x}$/AlGaN interface. It is not significantly affected by the Si$_x$N$_{1-x}$ density. On the other hand, slow-mode degradation is associated with Si$_x$N$_{1-x}$ degradation caused by electric-field-induced oxidation. By using high-density Si$_x$N$_{1-x}$, the slow-mode degradation can be minimized.

Devices for research purposes are usually designed and fabricated in a way that certain failure can be magnified to study the failure mechanism better. However, commercial devices focus more on reliability and performance maximization. In ongoing research, we are also interested in characterizing the reliability of commercial GaN HEMTs produced by CREE Inc. A statistical reliability model will be developed, and comparison with devices produced by SMART-LEES will be made. Figure 2 shows the initial characterization of GaN HEMTs produced by CREE, Inc. Reliability testing of these devices is underway.

FURTHER READING

Gallium Nitride (GaN) transistors are increasing in popularity for high voltage power electronics applications. The most promising device structure is the metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT). MIS-HEMTs are of interest because of their high breakdown voltage, low gate leakage current, and high channel conductivity. However, before commercial deployment, more work is required to improve the reliability and to reduce the instability of GaN MIS-HEMTs (Figure 1). Our work is focused on the characterization, ON-state time-dependent dielectric breakdown (TDDB), OFF-state TDDB, and Weibull statistical analysis of a novel GaN transistor. Our goal is to study and understand the physics behind gate dielectric breakdown in this device in order to assess device robustness to prolonged operation. We have completed many studies on these devices to determine breakdown location along the channel, chip to chip variation, temperature dependence, voltage dependence, threshold voltage shift, and projected lifetime.

During sustained ON-state bias at a high voltage, these devices exhibit trapping effects, stress-induced leakage current (SILC), progressive breakdown and eventually, hard dielectric breakdown (Figure 2). This is comparable to past MIS-HEMT studies in our group. As expected, hard breakdown time decreases as both temperature and drain voltage (VDS) are increased.

OFF-state TDDB proved difficult because of parasitics, test implementation, and a high variability of over three orders of magnitude in hard breakdown time. An alternative methodology was used, increasing VDS in a linear ramp until hard breakdown occurred. This allows us to characterize the instantaneous breakdown voltage of the devices. Analyzing these results using a Weibull distribution shows a two-slope distribution. This can mean that two breakdown mechanisms are present or that there are multiple layers in the gate stack with different rates of defect generation.

Our present research focuses on determining a methodology to accurately evaluate device lifetime during the application of a large drain bias while the device is in the OFF state.

**FURTHER READING**


▲ Figure 1: Cross section of a typical MIS-HEMT (left) and a depiction of defect generation and breakdown path formation in the gate dielectric under high field stress using the percolation model (right).

▲ Figure 2: A typical gate current progression during an ON-state TDDB experiment displaying trapping effects, SILC, and no progressive breakdown before hard breakdown.
Gate Dielectric Reliability under Mechanical Stress in High-voltage GaN Field-effect Transistors

E. S. Lee, J. A. del Alamo
Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining attention as a solution to meet the growing demand for energy and sustainability. GaN field-effect transistors (FET) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry large current. However, at the present time, the GaN metal-insulator-semiconductor high-electron-mobility-transistor (MIS-HEMT), the device of choice for electric power management, is limited from commercialization due to many challenges, including gate dielectric reliability. Under continued gate bias, the dielectric ultimately experiences a catastrophic breakdown that renders the transistor useless, a phenomenon called time-dependent dielectric breakdown (TDDB).

One key issue is the impact of mechanical strain on TDDB. In particular, when studying OFF-state stress conditions where the drain-source bias is very positive and gate-source bias is negative, the presence of unknown traps at both the interfaces and the bulk of the heterolayers can detrimentally impact dielectric reliability. Mechanical strain introduced during fabrication steps may be causing further reliability problems by amplifying the presence of traps.

To understand the impact of mechanical strain on TDDB, we apply external strain by physically bending the devices. We compare the TDDB distributions which follow the Weibull statistical distribution at different external strain.

Figure 1 shows TDDB under ON-state stress conditions. Under this situation, the gate is held at a positive bias while the drain and the source are grounded. Since the channel is not depleted, the electric field across the dielectric is distributed throughout the entire gate length and therefore traps make minimal impact on TDDB. Indeed, the breakdown statistics show that for two different mechanical strain, there is little change.

One other hand, figure 2 shows that TDDB under OFF-state stress condition changes with external strain. Under this stress condition, the majority of the electric field through the dielectric is focused at the gate/drain edge. As more of the electric field is focused in a small area, traps can play a significant role in TDDB.

Understanding the role of mechanical stress in amplifying trap effects will help the efforts to understand the physics behind TDDB.

Further Reading

High-performance Graphene-on-GaN Hot Electron Transistor

A. Zubair, A. Nourbakhsh, M. Qi, H. Wang, M. Hempel, J. Kong, D. Jena, M. Dresselhaus, T. Palacios
Sponsorship: ARO, NSF CIQM, AFOSR

Hot electron transistors (HETs) are promising devices for high-frequency operation and probing the fundamental physics of hot electron transport. In a HET, carrier transport is out of plane (Figure 1) due to the injection of hot electrons from an emitter to a collector which is modulated by a base electrode. HETs have been used to probe scattering events, band nonparabolicity, size-quantization effects, and intervalley transfer in different material systems. Monolayer graphene, being the thinnest available conductive membrane in nature, provides us with the opportunity to study the HET transport properties at the ultimate scaling limit.

Previously, we have demonstrated graphene-base HET with GaN/AlN emitter and a graphene/WSe$_2$ van der Waals heterostructure collector base-collector stack that can overcome the performance limitation of the graphene-base HETs with oxide barriers. In this work, we studied the effect of material parameters on the transport properties of the heterojunction diodes (i.e., Emitter-Base and Base-Collector) of HETs, and their impact on the HET performance. Temperature dependent transport measurements identify quantum mechanical tunneling as the major carrier transport mechanism in HETs. We demonstrate a new generation of graphene-base HET with record current density above kA/cm$^2$ (Figure 2) by scaling the tunneling barrier thickness and device geometry optimization. Preliminary simulations show that with further optimization graphene-on-GaN HET can outperform the bulk HETs towards ultra-high frequency operation.

Further Reading


Figure 1: Schematic cross section and biasing configuration for graphene-on-GaN HET presented in this work (left). Energy band diagram along the transport direction (out of plane) at $V_{CB}$ = 0V (solid lines) and $V_{CB}$ > 0V (dotted lines) (right).

Figure 2: Benchmarking of experimentally demonstrated HETs with sub-10 nm base thickness with different base materials (blue, purple and black symbols represent graphene, MoS$_2$ and GaN base, respectively). Theoretical device performance for optimized device structure (ideal HET) has been added as reference.
Circuit-performance Evaluation of Negative Capacitance FETs using MIT Virtual Source Negative Capacitance FET (MVSNC) Model

U. Radhakrishna, A. I. Khan, S. Salahuddin, D. A. Antoniadis
Sponsorship: SMART-LEES, NSF-NEEDS

Negative Capacitance Field Effect Transistors (NCFETs) have emerged as promising candidates for CMOS technology scaling due to their potential for sub-60-mV/decade operation by utilizing negative capacitance effects in ferroelectric materials. A ferroelectric oxide (FE-oxide) capacitor in series with the normal gate-stack capacitor of a conventional MOSFET forms the NCFET as shown in Figure 1. A physics-based compact model, MVSNC, is proposed to capture the device–behavior under static and dynamic operating conditions using the MVS-framework for the underlying MOSFET and the Landau-Khalatnikov (L-K) equation to model the FE-oxide as shown in sub-circuit of Figure 1.

The baseline MOSFET is characterized against Intel-45nm data and while PZT oxide of \( t_{FE} = 5 \) nm is chosen for NCFETs. The model is implemented in Verilog-A, and transient simulations are performed using a commercial simulator (ADS®). The simulated device-level IV- and CV-characteristics of NCFET and baseline FET are shown in Figure 1. With same off-currents, NCFETs exhibit steep subthreshold-swing (SS) due to stabilization of negative capacitance (NC)-state in FE-oxide and \( V_{G,int} \) amplification compared to VG. Higher on-current (at same \( V_D \)) with reduced or negative DIBL at certain \( V_D \) regimes can also be seen. The CV-characteristics show capacitance-amplification in sub-threshold regime.

Leakage in FE-oxide that can potentially remove the SS-steepness advantage in NCFETs is studied along with work-function engineering (WFE) that is proposed to mitigate the impact of FE-leakage. By shifting the FE-oxide’s Q-V curves along voltage-axis, WFE allows NC-state to be reached at low-V\(_{DD}\). The energy-delay \( (E-t_d) \) figure-of-merit of the NCFETs can be compared against baseline CMOS using loaded ring-oscillator (RO)-simulations. 21-stage ROs loaded with a constant capacitance \( C_L \) whose value is equal to total on-capacitance \( (C_{GG} \) at \( V_D = 0 \) and \( V_G = \) 1V) of the constituent baseline FETs of inverter are shown in Figure 2. Here, \( V_{DD} \) is swept to get the energy-delay plot. The figure shows reduced \( E-t_d \) in NCFETs even under leakage because of lower switching loss in \( C_L (0.5C_L V_D^2 f) \). The benefit of lower \( E-t_d \) with NCFETs is significant at scaled \( V_{DD} \) nodes and can be preserved even under DE-leakage scenarios by adopting WFE.

FURTHER READING
As continued scaling of silicon field-effect transistors (FETs) grows increasingly challenging, alternative paths for improving digital system energy efficiency are actively being pursued. These paths include replacing the transistor channel with emerging nanomaterials (such as carbon nanotubes: CNTs), as well as utilizing negative capacitance effects in ferroelectric materials in FET gate stacks, e.g., to improve sub-threshold slope beyond the 60 mV/decade limit (at temperature $= 300 \, {\text{K}}$) for conventional FETs (which in itself is difficult to achieve due to short-channel effects). However, which path provides the largest energy efficiency benefits, and whether these multiple paths can be combined to achieve additional energy efficiency benefits, is still unclear.

Here, we experimentally demonstrate the first negative capacitance carbon nanotube FETs (CNFETs: Figure 1), combining the benefits of both carbon nanotube channels (which offer superior electrostatic control vs. silicon-based FETs, simultaneously with superior carrier transport) and negative capacitance effects. We experimentally demonstrate negative capacitance CNFETs (NC-CNFTs) that achieve sub-60 mV/decade sub-threshold slope. Across 50 NC-CNFTs, our experimental results show an average sub-threshold slope of 55 mV/decade at room temperature, compared to 70 mV/decade for baseline CNFTs, i.e., without negative capacitance (Figure 2). The average on-state drive current ($I_{\text{ON}}$) of these NC-CNFTs improves by 2.1× vs. baseline CNFTs, for the same off-state leakage current ($I_{\text{OFF}}$). This work demonstrates a promising path forward for future generations of energy-efficient electronic systems.

**Figure 1.** (a) Schematic of baseline CNFET. (b) Carbon nanotube (CNT). (c) Scanning electron microscope (SEM) of CNFET channel region (top view). (d) Schematic of NC-CNFT.

**Figure 2.** (a) Experimentally measured drain current vs. gate-to-source voltage ($I_D$ vs. $V_{GS}$) characteristics from 50 baseline CNFETs and 50 NC-CNFTs (measured with drain-to-source voltage: $V_{DS} = 50 \, \text{mV}$). (b) Corresponding distribution of sub-threshold slope (SS, calculated over a 60 mV $V_{GS}$ range) for CNFETs in (a).

**FURTHER READING**

MoS\(_2\) FETs with Doped HfO\(_2\) Ferroelectric/Dielectric Gate Stack

A. Zubair, A. Nourbakhsh, M. Theng, E. McVay, T. Palacios

Sponsorship: ARO, AFOSR

Atomically thin layered two-dimensional transition metal dichalcogenides such as molybdenum disulfide (MoS\(_2\)) have been proposed to enable aggressive miniaturization of FETs. We previously reported ultra-short channel MoS\(_2\) FETs with channel length down to 15 nm and 7.5 nm using graphene and directed self-assembly pattern technique, respectively. However, the power scaling in such devices suffers from the same issues as in CMOS technology. Obtaining a subthreshold swing (SS) below the thermionic limit of 60 mV/dec by exploiting the negative-capacitance (NC) effect in ferroelectric (FE) materials is a novel effective technique to allow for the reduction of the supply voltage and power consumption in field-effect transistors (FETs). Conventional ferroelectric materials, i.e., lead zirconate titanate, bismuth ferrite, and polymer ferroelectric dielectrics such as P(VDF)-TRFE are not technologically compatible with standard CMOS fabrication processes. On the other hand, fluorite-type doped HfO\(_2\) ferroelectric thin-films deposited by ALD offers the CMOS compatibility and scalability required for advanced electronic applications.

In this work, we demonstrate NC-MoS\(_2\) FETs by incorporating a ferroelectric doped HfO\(_2\) (Al:HfO\(_2\) or Si: HfO\(_2\)) in the FET gate stack. Standard HfO\(_2\) has monoclinic crystal structure which can be transformed into orthorhombic phase by temperature, pressure, or doping. The electrical properties of the doped HfO\(_2\) thin-films can be tuned from dielectric to ferroelectric and even antiferroelectric by changing dopant type (Zr, Al, Si, Gd, Y, etc.), dopant fraction and/or capping layer. The ferroelectric nature of typical doped HfO\(_2\) thin film can be confirmed by the polarization measurement (Figure 1). Here, Si:Hf composition is kept fixed by controlling the 3DMAS/TEMAH pulses during the ALD. We observe steep SS in FETs when used these FE in the gate stack with carefully matched FE/DE bilayer. The NC-MoS\(_2\) FET built on a typical FE/DE bilayer showed a significant enhancement of the SS to 57 mV/dec at room temperature, compared with SS\(_{\text{min}} = 67\) mV/dec for the MoS\(_2\) FET with only HfO\(_2\) as a gate dielectric.

**FURTHER READING**


▲ Figure 1: Polarization vs. electric field of Si doped HfO\(_2\) thin film showing strong ferroelectric property compared to regular HfO\(_2\) thin film. Monoclinic doped HfO\(_2\) transforms into orthorhombic phase after rapid thermal annealing.

▲ Figure 2: Sub-threshold swing improvement in a MoS\(_2\) FET with FE/DE bilayer gate stack compared to FET with DE gate stack. Negative differential capacitance effect in the ferroelectric Al:HfO\(_2\) leads to SS lower than 60 mV/decade.
Graphene-based Ion-sensitive Field-effect Transistor Sensors for Detection of Ionized Calcium

C. Mackin, M. Xue, T. Palacios
Sponsorship: MIT-ARL ISN, NSF CIQM

Ion-sensitive field-effect transistors (ISFET) are used for measuring ion concentration in solution. Typical ISFET is silicon-based and suffers stability problems. Graphene is an atomically thin material with excellent electrical, mechanical, optical, and chemical properties. It can be used to replace silicon for biological and chemical sensing with the potential of being light weighted, flexible, and transparent.

This work develops a sensing platform (Figure 1A) with 152 individual ISFETs and an automatic data acquisition system. The array is functionalized with an ion-selective membrane and acts as a calcium sensor with excellent selectivity, sensitivity and response time. In particular, only calcium ion can be transported from the solution phase into the membrane via a charge neutral ionophore. At equilibrium, a stable Nernstian interface potential is achieved. With higher calcium concentration, the interface potential increases causing an effective shift in the sensor I-V characteristic. Hence, the sensor can detect and quantify changes in ionized calcium concentration through the shift in sensors I-V characteristic.

The shift in I-V characteristic is quantified by the location of minimum conduction point in graphene’s V-shaped curve, Dirac point. The theoretical rate of change in potential versus calcium concentration at room temperature is approximately 30mV/decade for bivalent ions such as calcium. Our data shows an average slope of 30.1 mV/decade with a standard deviation of 1.9 mV/decade, which agrees very well with the theory, therefore, indicates excellent sensitivity. By matching data from transient response with data from I-V characteristic, we can calculate the concentration of calcium with a single calibration reference. As depicted in Figure 1C, sensors are capable of quantifying ionized calcium concentrations spanning over five orders of magnitude. This proof-of-concept work represents a milestone in the development of graphene-based sensors for solution-phase chemical detection of analytes such as ionized calcium.

FURTHER READING

High Breakdown Voltage in Solution-processed High-voltage Organic Thin Film Transistors

A. Shih, E. V. Schell, A. I. Akinwande
Sponsorship: DARPA

Organic thin film transistors (OTFT) are excellent candidates for large area electronics on arbitrary and flexible substrates, enabling novel flexible displays as well as wearable electronics such as artificial skin. However, enabling truly-ubiquitous electronics through OTFTs demands not only high performance and high degree of flexibility, but also a wide range of operating voltages. Applications such as electrophoretic displays, digital X-ray imaging, photovoltaic systems-on-glass, and TFT-MEMS integration for large actuation are but a few that can enable high driving voltages on an OTFT technology platform.

We are currently developing a solution-processed 6,13-Bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) high-voltage, organic, thin film transistor (HVOTFT) with self-assembled monolayer (SAM) treatments that is capable of driving voltages beyond -450 V while operating with threshold voltages below -10 V. The ability to modulate such high-voltages with a relatively low gate voltage is highly appealing for future MEMS integration. The HVOTFT is defined by a dual channel architecture comprised of a gated and offset region, enabling FET and high-voltage capabilities, respectively. Furthermore, a high-k cubic pyrochlore dielectric Bi$_{1.5}$Zn$_1$Nb$_{1.5}$O$_7$ (BZN) is employed to achieve low gate leakage currents and low threshold voltages.

A combination of organosilane self-assembled monolayers and a self-shearing drop cast method is used to grow thin (< 100 nm) crystal bands of TIPS-pentacene on the HVOTFT structures. Controlling the thickness of the organic semiconductor layer is critical in achieving high breakdown voltages of ~450 V as well as high $I_{ON}/I_{OFF}$ current ratios of 104 A/A. Recent efforts in developing a self-aligned solution-process using surface energy engineering to enhance control of the crystal growth as well as to have transistor-to-transistor isolation have proven promising.

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**FURTHER READING**

Organic thin film transistors (TFTs) have been of great interest lately because of their potential applications in flexible systems, enabling devices such as electronic skins or implantable medical devices. With the ability to bend these new systems comes the question of how bending affects device performance. Consequently, thicker oxide layers are desirable because they are less likely to be stretched thin when flexed, preventing tunneling processes and high leakage currents. High-k dielectrics, such as the cubic pyrochlore Bi$_{1.5}$Zn$_{1}$Nb$_{1.5}$O$_{7}$ (BZN), have the potential to improve the reliability of this technology because they allow for a thicker film without decreasing capacitive coupling.

In this work, we investigated how the operating characteristics, like capacitance, change when devices are flexed. When the BZN is bent, strain is introduced into the crystal structure which can affect the dielectric constant. To explore this, we fabricated MIM capacitors and measured capacitance at different degrees of curvature to extract the dielectric constant. The capacitors, shown in Figure 1, were fabricated with a reactive sputtered BZN. Frequently, BZN is annealed at temperatures of 500-700°C; however, many flexible substrates, such as the Kapton polyimide films used here, are not compatible with such high-temperatures. Without annealing, the BZN was amorphous with a dielectric constant of around 30 as compared to values up to 200 found in crystalline BZN.

We found that when the devices were bent to the radii of curvature shown in Figure 2, the capacitance dropped to 85-95% of the original capacitance when flat. As there was no apparent change in thickness or area of the devices, we attributed this to a change in dielectric constant caused by strain in the crystal structure altering the alignment of electric dipoles in the material. When the devices were again laid flat, the capacitance returned to 95-99% of the original value. The information found in the MIM capacitor could be used to infer how device bending would affect behavior of a BZN-based OTFT for flexible applications.

**FURTHER READING**

Recent studies on the topological insulators (TI) have attracted great attention due to the rich spin-orbit physics and promising applications in spintronic devices. In particular, the strongly spin-moment coupled electronic states have been extensively pursued to realize efficient spin-orbit torque (SOT) switching. However, so far current-induced magnetic switching with TI has been observed only at cryogenic temperatures. Whether the topologically protected electronic states in TI could benefit from spintronic applications at room temperature remains a controversial issue.

In this work, we report SOT switching in a TI/ferromagnet heterostructure with perpendicular magnetic anisotropy (PMA) at room temperature. Ferrimagnetic cobalt-terbium (CoTb) alloy with robust bulk PMA is directly grown on a classical TI material, Bi$_2$Se$_3$. The low switching current density provides definitive proof of the high SOT efficiency from TI and suggests the topological spin-momentum locking in TI even if it is neighbored by a strong ferromagnet. Furthermore, the effective spin Hall angle of TI is determined to be several times larger than commonly used heavy metals. Our results demonstrate the robustness of TI as an SOT switching material and provide an avenue towards applicable TI-based spintronic devices.

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**Further Reading**

Current-induced Domain Wall Motion in Compensated Ferrimagnets

S. A. Siddiqui, J. Han, J. T. Finley, C. A. Ross, L. Liu
Sponsorship: NSF, SRC

Antiferromagnetic materials show promises compared to ferromagnetic materials for spintronic devices due to their immunity to external magnetic fields and their ultra-fast dynamics. However, difficulties in controlling and determining their magnetic state are limiting their technological applications. At the compensation point, the two antiparallel sub-lattices in a ferrimagnet have the same magnetic moment, and the material is an antiferromagnet. Compensated ferrimagnets are expected to exhibit fast magnetic dynamics like an antiferromagnet, and yet their magnetic state can be manipulated and detected like a ferromagnet, and therefore, have been pursued as a candidate system for ultrafast spintronic applications. Previously, it was demonstrated that current-induced spin-orbit torque could provide an efficient switching mechanism for a compensated ferrimagnet. However, limited by the quasi-static measurement technique, the nature of the switching dynamics in these experiments is yet to be revealed. In this work, we provide the first experimental proof of current-induced fast domain wall (DW) motion in a compensated ferrimagnet.

Using a magneto-optic Kerr effect microscope, we determine the spin-orbit torque-induced DW motion in Pt/Co$_{1-x}$Tb$_x$ microwires with perpendicular magnetic anisotropy. The DW velocity is determined as a function of applied current amplitude. A large enhancement of the DW velocity is observed in angular momentum compensated Pt/Co$_{0.74}$Tb$_{0.26}$ microwires compared to single layer or multi-layer ferromagnetic wires (Figure 1). Using analytical model, we also find that near angular momentum compensation point, the domain walls do not show any velocity saturation unlike ferromagnets or uncompensated ferrimagnets since both the effective gyromagnetic ratio and effective damping diverge at this composition (Figure 2). Moreover, by studying the dependence of the domain wall velocity with the longitudinal in-plane field, we identify the structures of ferrimagnetic domain walls across the compensation points. The high current-induced domain wall mobility and the robust domain wall chirality in compensated ferrimagnets open new opportunities for spintronic logic and memory devices.

FURTHER READING

High-k dielectrics play a key role in modern microelectronic circuitry, given their ability to provide reduced leakage currents while providing adequate capacitance in ever smaller nano-dimensional metal-oxide semiconductor field-effect transistor (MOSFET) devices. Recently, the Beach group at MIT demonstrated the ability to modulate the magnetic properties of transition metal thin films by electrical bias across thin films of Gd$_2$O$_3$. The reversible switching was demonstrated to be assisted by the electro-migration of oxygen ions to and away from the transition metal/Gd$_2$O$_3$ interface. This novel process, now called “magneto-ionic control” creates new opportunities for nonvolatile information storage.

Like magneto-ionic device, there is another important emerging device called “memristor” which applies field driven ionic transport-controlled property toggling. Though this device has been researched widely for a decade and defect chemistry of dielectrics is critical to the device operation, understanding of defect chemistry of dielectrics used for memristors are still limited. Here, we have examined electrical and transport properties of Gd$_2$O$_3$ via impedance spectra as a function of temperature and oxygen partial pressure considering Gd$_2$O$_3$ as a model oxide for ionic migration-controlled devices. In this research, we found that Gd$_2$O$_3$ can be electronic or mixed ionic-electronic conductor at high-temperature via controlling doping and phase. This research will be continued to the lower temperature regime to understand the correlation between the behavior of such devices and defect chemistry of dielectrics.

In addition, we have begun an investigation of the mechanism of magneto-ionic devices in a viewpoint of considering magneto-ionic device as an electrochemical cell. Previous research indicated that this device behaves in a manner similar to high-temperature electrochemical devices. We are preparing model devices that reflect features of both magneto-ionic and electrochemical devices and are examining their properties in situ.

FURTHER READING

Probing 2-D Magnetism in van der Waals Crystalline Insulators via Electron Tunneling


In this work, we introduce tunneling through layered insulators as a versatile probe of nanoscale magnetism. We fabricate van der Waals heterostructures of two graphite sheets separated by a magnetic CrI$_3$ tunnel barrier (Figure 1). For magnetic tunnel junctions, the barrier height is lowered for electrons aligned with the magnetic layer, resulting in a direct dependence of the conductance across the junction on the magnetic ordering in the CrI$_3$ barrier.

Layers of CrI$_3$ align their spins perpendicular to the crystal, either up or down. By sweeping an applied magnetic field, we detect discrete steps in the junction conductance (Figure 2) corresponding to individual layers in the CrI$_3$ barrier flipping out-of-plane magnetization. For example, when the magnetic field is swept up past 1 T in the bilayer device, the spins in the two layers of CrI$_3$ both align with the field, resulting in a 95% magnetoresistance.

Moreover, we can control the spin polarization of the output current with applied magnetic field, generating currents with up to 99% polarization. Thus, in addition to studying 2-D magnetic crystals using electrical readout of the magnetization, this result could also be applied to develop novel magnetic memory devices incorporating spin-orbit torques and other spintronic techniques.

FURTHER READING


▲ Figure 1: False-color optical micrograph of a representative tetralayer CrI$_3$ tunnel junction device. Inset: schematic of electrons tunneling through the CrI$_3$ barrier between the two graphite contacts.

▲ Figure 2: Zero-bias junction conductance vs. applied magnetic field swept up (black) and down (purple) for bilayer (a) and tetralayer (b) CrI$_3$ tunnel junction devices.
Microwave Modulation of Relaxation Oscillations in Superconducting Nanowires

E. Toomey, Q.-Y. Zhao, A. N. McCaughan, K. K. Berggren
Sponsorship: Intel, IARPA, NSF GRFP

Superconductors are ideal platforms for studying nonlinear behavior due to their nonlinear switching dynamics and phase relationships. Josephson junctions (JJJs), the most common superconducting devices, have a nonlinear current-phase relationship that allows them to phase lock to weak external periodic drives. This phenomenon, known as the AC Josephson effect, produces distinct DC steps in the time-averaged current-voltage characteristics at voltage intervals of $V_n = n hf/2e$, where $n$ is an integer, $h$ is Planck’s constant, $f$ is the frequency of the external radiation, and $e$ is the electronic charge. Such a relationship has enabled technology such as the Josephson voltage standard and analog-to-digital converters.

Unlike JJJ, superconducting nanowires are governed by a thermal nonlinearity that controls the switching into and out of the resistive state. In this work, we have studied fast oscillations in superconducting nanowires based on the electrothermal feedback between the nanowire hotspot and an external shunt resistor with a series inductance. In addition to studying how circuit parameters influence the frequency of the oscillations, we show that the oscillations can mix with an external microwave drive and eventually phase lock (Figure 1). This process produces a nanowire analog to the AC Josephson effect, with steps occurring at intervals of $V_n = nf I_c L$, here $n$ is an integer, $f$ is the frequency of the drive, $I_c$ is the critical current of the nanowire, and $L$ is the series inductance (Figure 2). In addition to offering a potential avenue for measuring inductance through the appearance of phase-locked steps, the ability of these oscillations to mix with an external drive is promising for applications such as parametric amplification and frequency multiplexing.

**FURTHER READING**

The development of a practical supercomputer relies on having a scalable memory cell, energy efficient control circuitry, and the ability to read and write a state without sacrificing density. Typical superconducting memories relying on Josephson junctions (JJs) have demonstrated extremely low power dissipation ($10^{-19}$ J) and rapid access times (< 10 ps), but suffer from large device dimensions and complex readout circuitry, making scalability a considerable challenge.

As an alternative to JJ-based superconducting memories, we have made a memory based solely on lithographic niobium nitride nanowires. The state of the memory is dictated by persistent current stored in a superconducting loop, while the write and read operations are facilitated by nanowire cryotron devices patterned alongside the memory loop in a single lithographic process. In addition to ease of fabrication, superconducting nanowires offer the advantage of relying on kinetic rather than geometric inductance, allowing the memory cell to be scaled down for high device density without sacrificing performance. Additionally, since persistent current is stored without Ohmic loss, the memory cell has minimal power dissipation in the static state.

We have demonstrated a 3 µm x 7 µm proof-of-concept device with an energy dissipation of ~ 10 fJ and a bit error rate < 10^-7. Current work focuses on developing a multilayer fabrication process to expand the single memory element into an array and to reduce device dimensions for further density optimization.

**FURTHER READING**

Although several types of architectures combining memories and transistors have been used to demonstrate artificial synaptic arrays, they usually present limited scalability and high-power consumption. Analog-switching devices may overcome these limitations, yet the typical switching process they rely on, formation of filaments in an amorphous medium, is not easily controlled and hence hampers the spatial and temporal reproducibility of the performance.

Here we demonstrate single-crystalline SiGe epiRAM with minimal spatial/temporal variations with long retention/great endurance, and high analog current on/off ratio with tunable linearity in conductance update, thus justifying epiRAM’s suitability for transistor-free neuromorphic computing arrays. This is achieved through one-dimensional confinement of conductive Ag filaments into dislocations in SiGe and enhanced ion transport in the confined paths via defect selective etch to open up the dislocation pipes. In SiGe epiRAM, the threading dislocation density can be maximized by increasing Ge contents in SiGe or controlling degree of relaxation23, and we discovered that 60 nm-thick Si$_{0.9}$Ge$_{0.1}$ epiRAM contains enough dislocations to switch at tens of nanometer scale devices. Our simulation-based on all those characteristics of epiRAM shows 95.1% accurate supervised learning with the MNIST handwritten recognition dataset. Thus, this is an important step towards developing large-scale and fully-functioning neuromorphic-hardware.

![Figure 1: a) Cycle-to-cycle variation (1%), b) Device-to-device variation (4%), c) TEM image showing confined Ag filament, d) $>10^9$ endurance, e) Linear conductance update, f) 1.8 years retention at room T, g) Intrinsic Schottky barrier to block sneak path, h) > 95% MNIST Data classification, i) 2.8% variation and 100% yield in array form.](image)

**FURTHER READING:**
The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based memristor, a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, offers to replace classic transistors in the future. It has the potential to achieve an order of magnitude lower operation power compared to existing RAM technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed ionic electronic conductors; thereby providing guidelines for material selection and for achieving improved device performance and robustness.
Lithium Neuromorphic Computing and Memories

J. C. Gonzalez-Rosillo, K. M. Mullin, Y. Zhu, Z. Hood, J. L. M. Rupp
Sponsorship: CMSE

Ionically-controlled memristors could allow for the realization of highly functional, low-energy circuit elements operating on multiple resistance states and to encode information beyond binary. The application of a sufficiently high electric field induces a non-volatile resistance change linked to locally induced redox processes in the oxide. State-of-the-art devices operate mainly on O₂⁻, Ag⁺ or Cu₂⁺ ions hopping over vacancies. Surprisingly, despite their fast diffusivity and stability towards high voltages, lithium solid-state oxide conductors have almost been neglected as switching materials. Our work investigates lithium ionic carrier and defect kinetics in oxides to design material architectures and interfaces for novel Li-operated memristors as alternative memory material.

Extensive efforts were devoted to understand the growth of the chosen Li-oxides conductor thin films by Pulsed Laser Deposition (PLD) and to microfabricate model thin film architecture devices. In-house overlithiated pellets of the selected oxides were synthesized and used as PLD targets. Dense, crack-free thin film oxides have been successfully grown on Pt/Si_N_x/Si substrates, including multilayer heterostructures of two selected Li-oxide materials. Remarkably, Pt/Li-oxide/Pt structures (Figure 1a and b) show a significant bipolar resistive switching effect with a resistance ratio $R_{off}/R_{on} \sim 10^4-10^5$ at beneficial low operation voltages to reduce the footprint at operation (~3V for a non-device lab optimized architecture) (Figure 1a).

In addition, sweep rate, thickness, and area dependence studies suggest that the bulk oxide plays a major role in the diffusion of the ionic species for achieving a large and tunable resistance ratio. This phenomenon makes the new investigated Li-oxides novel candidate material as new neuromorphic computing element. In situ Raman Spectroscopy and TEM experiments will shed light on the microstructure and its defects and will allow a better understanding of the underlying physical mechanism of the switching behavior. Also, new routes are explored to modify the lithiation degree of the thin films and would add an extra parameter to tune and alter switching kinetics and resistance retention.

![Figure 1: (a) Sketch of the proposed architecture and (b) a micrograph of a microfabricated device. Electrode size is 500 µm.](image)

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**WSe₂ Thin Film Solar Cells**

E. McVay, A. Zubair, M. Hempel, T. Palacios

**Sponsorship:** NASA, AFOSR FATE MURI

Our group is interested in exploring the ultimate limits of microsystem scaling and functionality. The amount of energy available to the system is one of the key constraints, and solar cells based on transition metal dichalcogenides (TMDs) could be a key component of future highly-integrated microsystems.

Single atomic layer TMDs have been explored extensively for ultrathin optoelectronic applications due to their direct bandgap and strong light-matter interactions. However, optoelectronic applications of multi-layer TMD thin-films have not been as extensively studied despite their strong absorption characteristics and wide absorption frequency. Nevertheless, published work has shown that a p-n junction made with chemically doped multilayer MoS₂ can achieve an efficiency of 2.8%, and a vertical Schottky junction WSe₂ solar cell can achieve efficiencies as high as 6.7%. Most intriguingly, it has been shown that with careful design, a 15nm WSe₂ solar cell can absorb 90% of 633nm incident light, demonstrating that TMDs can push the limit of thin film photovoltaics.

In this work, we study the electronic transport and photovoltaic characteristics of multilayer (~100 nm) WSe₂ devices that can later be integrated as the energy harvester in a micro-scale sensing system. We have demonstrated a Schottky junction WSe₂ solar cell using dissimilar metal contacts. The proof-of-concept dual-metal device showed an open-circuit voltage of ~ 0.2 V, short circuit current density ~ 4 mA/cm² and power conversion efficiency ~ 2% under white light illumination with input power of 300 W/m². This study is extended to explore methods to better optimize the WSe₂ based solar cell using experimental and modeling techniques. We are currently developing hole and electron transport layers to improve the device efficiency.

**FURTHER READING:**

Critical Design Parameters for Omnidirectional 2-D Filled Photonic Crystal Selective Emitter for Thermophotovoltaics

R. Sakakibara, V. Stelmakh, W. R. Chan, M. Ghebrebrhan, J. D. Joannopoulos, M. Soljačić, I. Čelanović

Sponsorship: ARO, U.S. Department of Energy

Thermophotovoltaic (TPV) systems are promising as small-scale, portable generators to power sensors, small robotic platforms, and portable computational and communication equipment. In TPV systems, an emitter at high-temperature emits radiation that is then converted to electricity by a low bandgap photovoltaic cell. One approach to improve the efficiency is to use hafnia-filled two-dimensional (2-D) tantalum (Ta) photonic crystals (PhCs). These emitters enable efficient spectral tailoring of thermal radiation for a wide range of incidence angles. However, fabricating these PhCs is difficult. We use focused ion beam (FIB) imaging and simulations to investigate the effects of fabrication imperfections on the emittance of a fabricated hafnia-filled PhC and to identify design parameters critical to the overall PhC performance. We demonstrate that, more so than uniform cavity filling, the PhC performance relies on the precise cavity period and radius values and thickness of the top hafnia layer.

![Figure 1: Schematic of a filled photonic crystal (PhC). The geometric parameters are cavity period $a$, cavity radius $r$, cavity depth $d$, and hafnia thickness $t$. The substrate is tantalum.](image1)

![Figure 2: Focused ion beam (FIB) image of the fabricated filled PhC cross section clearly shows incomplete cavity filling and a thick layer of hafnia above the cavity.](image2)

FURTHER READING


Low-power Management IC for Vibrational Energy Harvesting Applications

Sponsorship: Analog Devices, Inc.

Vibration-based machine health monitoring provides an efficient real-time method for tracking the health of industrial motors, thereby achieving predictive maintenance and avoiding machine downtime. Vibration sensors are attached to the vibrating motors, and periodically transmit data indicative of machine health. To power such monitors, we demonstrate a vibration-based energy harvesting system whose schematic is shown in Figure 1. It extracts power from 50Hz industrial motors and comprises a co-designed MEMS-based transducer and associated low-power management circuit.

The MEMS-based energy harvester shown in Figure 1 can generate about 1 mW output power under matched load at resonance. However, its high quality-factor results in significant reduction in output power and voltage at off-resonance conditions. The system is made resilient to manufacturing variations which cause a mismatch between the harvester’s natural resonance and the motor frequency by using the interface power electronics. A Meissner oscillator circuit shown in Figure 2 is used to achieve battery-less cold-start from low harvester-voltages at off-resonance. A regular operation circuit is designed to operate once the cold-start circuit generates above-1V output voltage ($V_{\text{out}}$). This circuit employs an H-bridge to interface the harvester whose FETs are switched based on current-feedback. The load-storage element is toggled between the two ports of the harvester to synthesize the desired load-current at any frequency. The circuit thus accomplishes conjugate-impedance matching for efficient power extraction from the harvester. Further, it can tune the harvester’s source reactance to electrically shift its resonance to achieve increased bandwidth of operation.

The IC implemented in the Taiwan Semiconductor Manufacturing Company (TSMC) 180nm process (shown in Figure 1) is co-designed with the harvester achieves cold-start from 150mV-peak AC-voltage from the harvester at 5% off-resonance (10x state-of-the-art). The H-bridge circuit is able to deliver 800 μW to the load at 71% efficiency at resonance as shown in Figure 2. It is also able to perform frequency tuning to account for manufacturing tolerances (A first low-power IC demonstration for this application).

FURTHER READING

Electromagnetic MEMS Harvester for Vibrational Energy Harvesting Applications
Sponsorship: Analog Devices, Inc.

Powering machine health monitoring sensors with the motions from the machinery allows install-and-forget implementation of the machine health monitoring network. Electromagnetic MEMS based-transducer provides an efficient interface between industrial machines and the rest of the vibration-based energy harvesting system. Implementing the mechanical harvester’s spring system on silicon, allows the mechanical system and the circuit to be manufactured through the same process, cutting down on both assembly time and complexity.

The transducer design uses a modified version of the classic 4 bar linkage spring design. The long beams are tapered such that the end connecting to the guide rod is wider than the connecting region to the shuttle, which houses the magnet (see Figure 1). This alleviates the stress experienced at the joints of the beam, which is the typical weak point of the structure. With the tapered beam, the current design achieves a full stroke of 1.6mm and is more robust with regard to handling during the assembly process. The design also offers good modal separation, with the modal frequency of the first undesirable mode several hundred Hz above the desired, horizontal translational mode.

The coils are manually wound using 42 AWG enamel coated copper wires with two coils placed at 150mm above and below the magnet’s plane of motion. The coils and the spring system are each fixed in a plastic package. When attached to the source of vibration, the harvester’s magnet vibrates in between the coils, inducing an EMF in the coils in accordance with Lenz’s Law. The coils are connected in series, and the induced voltages add to produce an output voltage, which is interfaced with custom designed circuitry for energy harvesting. The assembled mechanical harvester can deliver 1mW of output power at resonance with a matched load.

FURTHER READING
MEMS energy harvesting has been keenly pursued to provide perpetual power for many wireless applications including distributed sensor networks and upcoming IoT systems. However, scavenging a sufficient amount of power for wireless communication from environmentally available vibrations, typically at low frequency (<70 Hz) and low acceleration (0.5g), has neither been successful nor reported at the MEMS scale. Here we present a bi-stable buckled beam MEMS energy harvester which could meet those requirements in terms of low operating frequency, wide bandwidth, and power, all packaged in the size of a coin. This new design does not rely on conventional linear or non-linear resonance of the MEMS structure, but instead operates with large snapping motions of buckled beams at very low frequencies. A fully functional piezoelectric device has been designed, monolithically fabricated, and tested to induce bi-stable buckling of ~200 µm. The first batch device generated peak power of 85 nW with 50% half-power bandwidth under 70 Hz at 0.5g.

Our bi-stable nonlinear oscillator-based MEMS energy harvester has a clamped-clamped beam structure with a stack of thin-films having 28 pairs of beams 0.4 mm wide in a silicon frame of 15 mm × 12 mm. Each beam has approximately 500 interdigitated Au fingers over 0.2 µm thick PZT. A proof mass is located in the middle, connecting the beams to synchronize their out-of-plane motion and minimize undesirable torsion.

Thin-film layers of various stresses have an effective total compression and balanced stress with respect to the neutral axis to achieve bi-stable buckling. The residual stress and the thickness of the thin films are monitored for each deposition step, and progressive feedback control of subsequent deposition is employed to minimize deviation from the design target. The final released device (Figure 1) shows desired bi-stable buckling of about 200 µm (Figure 2) which is within 5% of the designed value. The dynamic testing with a laser vibrometer validates the design concept that the buckled beam device could have large-amplitude oscillations with low-frequency and low-amplitude inputs (<70 Hz and 0.5g).

**FURTHER READING**


▲ Figure 1: Photo of the released device.

▲ Figure 2. Surface profile scan: Surface profile of four beams showing the buckling on both sides (bi-stable) at around 200 µm.
RuO$_2$ as Cathode Material of Thin Film Lithium-ion Batteries (LIB)


Sponsorship: SMART, MIT Lincoln Laboratory

Technologies for the Internet of Things (IoT) are being developed for a vast number of networking applications. Thin film batteries are important for IoT systems as they are better integrated within an integrated circuit (IC) and can store energy that is harvested by green generators (e.g., solar cells) and provide it to sensors. RuO$_2$ had been found to have a larger specific capacity compared to other cathode materials of lithium ion batteries (LIB), and thus, is a good candidate as a cathode material of thin film LIB. We are currently studying the reaction mechanism of RuO$_2$ and lithium in parallel with the fabrication of full battery devices.

To analyze the mechanism of lithium storage in thin film RuO$_2$, we performed cyclic voltammetry (CV) tests with varying lower limits, as shown in Figure 1. Surprisingly, the lithiation process consists of 3 peaks while the delithiation process consists of 4 peaks. Moreover, the 3$^{rd}$ delithiation peak does not appear in sequential order relative to the other delithiation peaks. To reveal the correspondence between the peaks and specific reactions, ex situ cross-sectional TEM, electron diffraction, Raman spectroscopy, and XPS are currently being used.

In addition to characterizing the lithiation of RuO$_2$, we have also built full battery devices that include a lithiated Si anode, a lithium phosphorous oxynitride (LiPON) electrolyte, and RuO$_2$ cathode. Figure 2 shows the cycle performance of the microbattery at a rate of C/10. It could deliver a highly reversible capacity of approximately 150 µAh cm$^{-2}$ µm$^{-1}$ after 100 cycles, which is still 2.5 times higher than commercial CYMBET microbatteries. Ongoing work is focused on improving the cyclability of the RuO$_2$ and silicon anodes through stress engineering, as well as improving the volumetric capacity through process improvements. These initial results suggest a promising route towards IC integratable batteries for on-chip power delivery.

![Figure 1: CV scans with varying lower limit of RuO$_2$ thin film. Counter electrode was Li metal, and electrolyte was 1M LiPF$_6$ in 1:1(v:v) EC/DMC.](image1)

![Figure 2: Cycle data of thin film RuO$_2$/LiPON/Li-Si full batteries.](image2)

FURTHER READING

Among all the known anode materials for Li-ion batteries, Si is a promising candidate for applications in CMOS-compatible microbatteries. It has extraordinarily high capacities (8375 Ah/cm$^3$, 3579 Ah/kg), which is a result of the unique alloying mechanism during lithiation that involves bond breakage and a series of formation of new short-range structures. The reversible lithiation of Si anodes (Figure 1, highlighted) has not been extensively studied, and there have also been debates over whether it is a diffusion process or a phase-transition process. Here we adopt the potentiostatic technique to study the reversible phase transitions that occur in the second and subsequent lithiation cycles.

It was found that there is always a peak in the current vs. time curve under desirable potentiostatic test conditions in the reversible lithiation regime (Figure 2). The existence of the peak suggests there is phase transition in the reversible lithiation, rather than pure diffusion where current should decrease monotonically with time. The time at which the peak occurs ($t_{\text{peak}}$) increases with the applied potential, which indicates slower kinetics for the phase transition. Kinetic parameters could be extrapolated from the current vs. time curves upon modeling and fitting.

**FURTHER READING**

Li-O$_2$ batteries offer the possibility of storing twice the gravimetric energy density of Li-ion batteries. Li-O$_2$ batteries operate by reacting oxygen with lithium ions in a non-aqueous solvent to form Li$_2$O$_2$ on a conductive cathode material. However, Li$_2$O$_2$ has poor electronic conductivity and passivates the electrode area. Achieving high capacity requires careful attention to Li-O$_2$ discharge mechanisms in order to optimize cathode void space filling by Li$_2$O$_2$.

Li-O$_2$ discharge occurs by two competing mechanistic pathways which are responsible for two possible morphologies of Li$_2$O$_2$ discharge product. The surface pathway involves two consecutive electron transfers to form a ~10 nm thin film of Li$_2$O$_2$. The solvent pathway involves the solvation of the reaction intermediate Li$^+$-O$_2^-$, which then reacts in solution to form ~100 nm in diameter toroids of Li$_2$O$_2$. Since toroids allow for greater volumes of Li$_2$O$_2$ to form with less electrode area coverage, toroids are preferable to maximize capacity. However, the exact dependence of each pathway on different discharge conditions and solvent properties to promote toroid formation is not fully understood.

Rotating ring-disk electrode (RRDE) experiments were performed to understand these pathway trends. A rotating rod creates convection currents that sweep reactants to the central disk electrode (Figure 1). Li$_2$O$_2$ film and soluble Li$^+$-O$_2^-$ are formed at the disk. Soluble Li$^+$-O$_2^-$ is swept to the ring electrode and oxidized, providing a measure of the relative size of the solvent pathway. By comparing ring and disk currents, the separate contribution of each discharge pathway can be determined.

We then developed a model based on nucleation and growth of the Li$_2$O$_2$ film to explain potentiostatic discharge curves collected from RRDE experiments under different discharge conditions, such as varying solvent water content (Figure 2). The model demonstrates that high Li$^+$-O$_2^-$ solvent solubility inhibits the surface pathway and that this effect is primarily responsible for toroid promotion.

**FURTHER READING**

Multi-cell Thermogalvanic Systems for Harvesting Energy from Cyclic Temperature Changes

L. Xu, P. A. Linford, B. Huang, C. V. Thompson, Y. Shao-Horn
Sponsorship: HKUST-MIT Research Alliance Consortium

Technologies for the Internet of Things (IoT) are being developed. An IoT network consists of large quantities of networked sensors that are often in remote or difficult to access locations, which drives the need for self-powered systems. Here, we come up with two types of multi-cell thermogalvanic systems that generate electrical power through temperature cycles.

The dual-temperature, dual-stack, self-powered electrochemical system is depicted in Figure 1. This dual-temperature system uses two identical electrochemical stacks, which can be a single battery or multiple batteries connected in series; however, each electrochemical stack is held at a different temperature. On the other hand, a single-temperature system works similarly, with the electrochemical stacks having similar operating potentials but oppositely signed temperature coefficients. Its operation is illustrated in Figure 2. Both systems can harvest energy from temperature cycles.

We have tested both dual-temperature systems and single-temperature systems with different cathode/anode materials, load resistances, and frequencies of temperature cycles. The largest energy conversion efficiency was obtained from the dual-temperature experiment with two homemade LiCoO₂/Li coin cells in which the cathodes with composition Li₀.₈₅CoO₂ were cycled between 20 °C and 50 °C. The loads were two 100Ω resistors. The current is shown in Figure 3, and the efficiency was calculated to be 0.22%. This value is comparable to the efficiency obtained using charging-free thermally regenerative electrochemical cycles (TRECs), thermocapacitive cycles and ionic thermoelectric supercapacitors, but with more flexibility of material selection. In the meantime, we have also tested two single-temperature systems with four LiV₂O₅/Li-Al and three LiCoO₂/Li cells, and one LiMnO₂/Li-Al and one LiV₂O₅/Li-Al cell, respectively. Although the efficiency and power were still limited, they confirmed the feasibility of this concept. These systems can be further optimized by using materials with higher temperature coefficients and decreasing internal resistance at the same time.

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The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Eight faculty members participate in the CICS: Director Hae-Seung Lee, Duane S. Boning, Anantha Chandrakasan, Ruonan Han, David Perreault, Max Shulaker, Charles Sodini, and Vivienne Sze.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed, THz, and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, deep learning systems, emerging technologies, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.
The MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) brings together MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional materials.

Graphene and other two-dimensional (2-D) materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of; at the same time that they have very rich electronic and chemical properties. For more than 40 years, MIT has led the work on the science and engineering of 2-D materials. More recently, since 2011, the MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2-D materials, devices, and systems to provide discriminating or break-through capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials to optoelectronics, RF communications, and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools, and analysis for the creation of a vision for the future of new systems enabled by 2-D materials.

Some of the multiple benefits of the Center’s membership include complimentary attendance to meetings, industry focus days, and live webcasting of seminars related to the main research directions of the Center. The members of the Center also gain access to a resume book that connects students with potential employers, as well as access to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today’s challenges for these materials, devices, and systems.
The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT GaN) is an interdepartmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications, and it coordinates work on the growth, technology, novel devices, circuits, and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing, and power management, as well as advanced optoelectronics. Most of the work is done on GaN materials and devices that are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride (GaN) Energy Initiative organizes numerous activities to advance the understanding of GaN materials, technology, and devices. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and pre-prints through its website.
The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will, in turn, transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personalized medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personalized medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication, and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient’s needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry’s societal transformation, Medical Electronic Devices.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacturing devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners’ diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure, and cerebral blood flow velocity. MEDRC has 4 sponsoring companies, 8 faculty members, 12 active projects, and approximately 15 students. A visiting scientist from a project’s sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT’s Institute for Medical Engineering and Science (IMES) that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.
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Principal Research Scientist  
Materials Research Laboratory  
Leader, Lab for Education and Application Prototypes, (LEAP),  
AIM Photonics Academy

**Faculty Profiles**

**Anuradha M. Agarwal**  
Principal Research Scientist  
Materials Research Laboratory  
Leader, Lab for Education and Application Prototypes, (LEAP),  
AIM Photonics Academy

**GRADUATE STUDENTS**

Dan Hao Ma, DMSE  
Eveline Postelnicu, DMSE  
Robin Singh, MechE (co-supervised with B. Anthony)  
Peter Su, DMSE  
Mingxiu Sun, MechE (co-supervised with B. Anthony)

**SELECTED PUBLICATIONS**


Methods of nanofabrication, especially applied to superconductive quantum circuits, photodetectors, high-speed superconductive electronics, and energy systems.

Rm. 38-219 | 617-324-0272 | berggren@mit.edu

RESEARCH SCIENTIST
Donald Keathley, RLE

POSTDOCTORAL ASSOCIATES
Reza Baghadi, RLE
Ilya Charaev, RLE

GRADUATE STUDENTS
Navid Abedzadeh, EECS
Akshay Agarwal, EECS
Brenden Butters, EECS
Andrew Dane, EECS, NASA TR Fellow
Hyung Wan Do, EECS
Murat Onen, EECS
Emily Toomey, EECS, NSF Fellow
Marco Turchetti, EECS
Yang Yujia, EECS
Di Zhu, EECS, A*STAR Fellow

UNDERGRADUATE STUDENTS
Ignacio Estay Forno, EECS
Hector Iglesias, Physics
Yukimi Morimoto, EECS

VISITORS
Luca Camellini, École Polytechnique Fédérale de Lausanne
Chia-Jung Chung, PSI Quantum
Eugenio Maggiolini, Politecnico di Torino
Menghie Zheng, Hunan University

SUPPORT STAFF
Marco Colangelo, Research Support Assistant
James Daley, Research Specialist
Dorothy Fleischer, Administrative Assistant
Owen Medeiros, Research Support Assistant
Mark Mondol, Assistant Director Nanostructures Lab
Rinske Wijtmans Robinson, Administrative Assistant

SELECTED PUBLICATIONS

Duane S. Boning
Clarence J. LeBel Professor of Electrical Engineering
Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Design for manufacturability of processes, devices, and circuits. Understanding variation in semiconductor, photonics and MEMS manufacturing, emphasizing statistical, machine learning, and physical modeling of spatial and operating variation in circuits, devices, and CMP, electroplating, spin coating, etch, and embossing processes.

Rm. 39-415a | 617-253-0931 | boning@mtl.mit.edu

GRADUATE STUDENTS
Basma Aiouche, MechE
Hongge Chen, EECS
Shile Ding, MechE/Sloan
Philip Ebben, MechE/Sloan
Sally El-Henawy, EECS
Christopher Lang, EECS
Timothy Marquart, MechE/Sloan
Germain Martinez, EECS
Daniel Moon, EECS
Muhammad Humas Shabbir, MechE
Gokce Solakoglu, MechE
Zhengxing Zhang, EECS

SUPPORT STAFF
Jami Mitchell, Administrative Assistant
Leslie Quinn, Administrative Assistant

SELECTED PUBLICATIONS


V. Michael Bove, Jr.
Principal Research Scientist
Media Arts and Sciences/Media Lab

Sensing, communication, user interface, and display (particularly 3-D and holographic) for consumer electronics. Materials and fabrication methods for diffractive light modulators.
Rm. E15-490 | 617-253-0334 | vmb@media.mit.edu

GRADUATE STUDENTS
Pedro Colon Hernandez, MAS
Bianca Datta, MAS
Sundeep Jolly, MAS
Everett Lawson, MAS
Philippa Mothersill, MAS
Daniel Novy, MAS
Vik Parthiban, MAS
Laura Perovich, MAS
Edwina Portocarrero, MAS
Caroline Rozendo Xavier dos Santos, MAS
Ali Shtarbanov, MAS

VISITOR
Shoichiro Sekiguchi, NHK TV

SUPPORT STAFF
Kristin Hall, Member Relations Manager

SELECTED PUBLICATIONS


Edward S. Boyden
Y. Eva Tan Professor in Neurotechnology at MIT
MIT Media Lab and McGovern Institute
Department of Biological Engineering
Department of Brain and Cognitive Sciences

Developing tools that enable the mapping of the molecules and wiring of the brain, the recording and control of its neural dynamics, and the repair of its dysfunction. Systematically analyzing and repairing normal and pathological brain computations.

Rm. E15-485 / 46-2171C | 617-324-3085 | esb@media.mit.edu

RESEARCH SCIENTISTS AND STAFF
Desiree Dudley, Media Lab
Manos Karagiannis, Media Lab
Demian Park, Media Lab
Jorg Scholvin, Media Lab
Doug Weston, Media Lab
Aimei Yang, Media Lab
Jian-Ping Zhao, Media Lab

POSTDOCTORAL ASSOCIATES
Shahar Alon, MAS
Giovanni Talei Franzesi, MAS
Ruixuan (Rui) Gao, MAS
Erica (Eunjung) Jung, MAS
Monique Kauke, MAS
Kiryl Piatkevich, MAS
Deblina Sarkar, MAS
Or Shemesh, MAS
Ru Wang, MAS
Chi Zhang, MAS

GRADUATE STUDENTS
Nick Barry, MAS
Orhan Celiker, EECS
Alexi Georges Choueiri, BCS
Danielle Cosio, BCS
Peilun Dai, BCS
Amauche Emenari, BCS
Daniel Estadiant, BCS
Daniel Goodwin, MAS
Ishan Gupta, BE
Eghbal Hosseini, BCS
Shannon Johnson, MAS
Louis (Jeong Seuk) Kang, Harvard
Changyang Linghu, EECS
Yixi Liu, EECS
Daniel Oran, MAS
Nikita Pak, ME
Andrew Payne, MAS
Paul Reginato, BE
Sam Rodrigues, Physics
David Rolnick, Mathematics
Cipriano Romero, EECS
Anubhav Sinha, HST
Mike Skuhersky, MAS
Ho-Jun Suk, HST
Corban Swain, BE
Cristina Torres Caban, BE
Asmamaw (Oz) Wassie, BE

Young Gyu Yoon, EECS
Jay (Chih-Chieh) Yu, EECS

SUPPORT STAFF
Holly Birns, Administrative Assistant
Lisa Lieberson, Senior Administrative Assistant

SELECTED PUBLICATIONS


* co-first authors
** co-corresponding authors
Matteo Bucci
Assistant Professor
Department of Nuclear Science and Engineering
Center for Advanced Nuclear Energy Systems (CANES)

RESEARCH SCIENTIST
Bren Phillips, NSE

POSTDOCTORAL ASSOCIATE
Mahamudur Rahman, NSE, MechE

GRADUATE STUDENTS
Florian Chavagnat, NSE
Anupam Jena, NSE
Artyom Kossolapov, NSE
Madhumitha Ravichandran, NSE
Jee Hyun Seong, NSE
Chi Wang, NSE
Limiao Zhang, NSE

UNDERGRADUATE STUDENTS
Olorunsola (Jerry) Akinsulire, NSE
Megan McCandless, MechE

VISITORS
Jiang Ge, XJTU
Jan Petrik, TUP
Bing Tan, XJTU

SELECTED PUBLICATIONS


Boiling heat transfer, surface engineering, nuclear reactor safety and efficiency.
Rm. 24-212 | 617-715-2336 | mbbucci @ mit . edu
Vladimir Bulović
Director, MIT.nano
Fariborz Maseeh Professor of Emerging Technology
Department of Electrical Engineering & Computer Science

Physical properties of organic and organic/inorganic composite structures, and
development of nanostructured electronic and optoelectronic devices. Applications
of nanostructured materials in large-scale technologies.
Rm. 13-3138 | 617-253-7012 | bulovic @ mit . edu

RESEARCH SCIENTISTS
Robert Nick, RLE
Anna Osherov, RLE
Annie Wang, RLE

POSTDOCTORAL ASSOCIATES
Giovanni Azzellino, RLE
Dane DeQuillettes, RLE
Maximilian Hoerantner, RLE
Joel Jean, RLE
Anurag Panda, RLE

GRADUATE STUDENTS
Roberto Brenes, EECS
Yumeng Cao, EECS
Wendy Chang, EECS
Matthew Chua, EECS, A*STAR Fellow
Mingye Gao, EECS
Jinchí Han, EECS
Madeliene Laitz, EECS, NSF Fellow
Melissa Li, EECS
Thomas Mahony, EECS
Apoorva Murarka, EECS
Farnaz Niroui, EECS, NSERC Scholarship
Mayuran Saravanapavanantham, EECS
Melany Sponseller, EECS
Richard Swartout, EECS
Ella Wassweiler, EECS, NSF Fellow
Mengfei Wu, EECS
Sihan Xie, DMSE
Haz Zhu, Physics
Ryan Zimmerman, MechE

UNDERGRADUATE STUDENTS
Adira Balzac, MechE
Elaine Ng, Physics
Jeffrey Yuan, EECS

VISITORS
Damien Reardon, DSM
Nageh Allam, American University of Cairo

SELECTED PUBLICATIONS


**Jacopo Buongiorno**  
TEPCO Professor, Associate Department Head  
Department of Nuclear Science and Engineering  
Director Center for Advanced Nuclear Energy Systems (CANES), an MITEI Low-Carbon Energy Center

- **Boiling heat transfer; nuclear reactor design and safety; offshore floating nuclear power plant; nanofluids for nuclear applications.**
- **Rm. 24-206 | 617-253-7316 | jacopo@mit.edu**

**GRADUATE STUDENTS**

- Patrick Champlin, NSE
- Lucas Rush, NSE
- Guanyu Su, NSE
- Patrick White, NSE

**UNDERGRADUATE STUDENT**

- Ze (Jenny) Dong, NSE, Sloan Fellow

**SUPPORT STAFF**

- Carolyn Carrington, Administrative Assistant

**SELECTED PUBLICATIONS**


Anantha Chandrakasan
Dean of Engineering
Van nevar Bush Professor of Electrical Engineering
& Computer Science
Department of Electrical Engineering & Computer Science

Anantha Chandrakasan
Dean of Engineering
Van nevar Bush Professor of Electrical Engineering
& Computer Science
Department of Electrical Engineering & Computer Science

POSTDOCTORAL ASSOCIATES
Wanyeong Jung
Ujwal Radhakrishna
Rabia Tugce Yazicigil

GRADUATE STUDENTS
Mohamed Radwan Abdelhamid, EECS
Utsav Banerjee, EECS
Avishek Biswas, EECS
Di-Chia Chuie, EECS (co-supervised with J. Glass)
Aya Galal, EECS
Preetinder Garcha, EECS
Taehoon Jeong, EECS (co-supervised with H.-S. Lee)
Zexi (Alex) Ji, EECS
Chiraag Juvekar, EECS
Harneet Khurana, EECS (co-supervised with H.-S. Lee)
Skanda Koppula, EECS
Saurav Maji, EECS
Rishabh Mittal, EECS (co-supervised with H.-S. Lee)
Nathan Monroe, EECS (co-supervised with J. H. Lang)
Sirma Orguc, EECS
Madeleine Waller, EECS
Miaorong Wang, EECS

VISITORS
Dennis Buss, Texas Instruments
Samuel Henry Fuller, Analog Devices, Inc.

UNDERGRADUATES STUDENTS
Sara Flanagan, EECS
Natalie Mions, EECS
Mengyuan (Mina) Sun, EECS

SUPPORT STAFF
Yuvie Cjapi, Administrative Assistant
Margaret Flaherty, Administrative Assistant

PUBLICATIONS


Riccardo Comin
Assistant Professor
Department of Physics

Rm. 13-2153 | 617-253-7834 | rcomin @ mit . edu

POSTDOCTORAL ASSOCIATES
Jonathan Pelliciari, SNSF Fellow
Zhihai Zhu, Physics

GRADUATE STUDENTS
Min Gu Kang, Physics, Samsung Fellow
Abraham Levitan, Physics
Jiarui Li, Physics
Qian Song, DMSE

UNDERGRADUATE STUDENTS
Benjamin Harpt, Physics
Talya Klinger, Physics

SUPPORT STAFF
Monica Wolf, Administrative Assistant

SELECTED PUBLICATIONS


Jesús A. del Alamo
MTL Director
Donner Professor
Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

RESEARCH SCIENTIST
Alon Vardi, MTL

POSTDOCTORAL ASSOCIATES
Young Tack Lee, MTL
Xin Zhao, MTL

GRADUATE STUDENTS
Xiaowei Cai, EECS
Alex Lednev, EECS
Ethan Lee, EECS
Wenjie Lu, EECS

UNDERGRADUATE STUDENT
Lisa Kong, DMSE

VISITOR
Jerzy Kanicki, University of Michigan
Moshe Tordjman, Technion

SUPPORT STAFF
Elizabeth Kubicki, Administrative Assistant
Mary O’Neil, Administrative Assistant

SELECTED PUBLICATIONS


Nicholas X. Fang
Professor
Department of Mechanical Engineering

Nanophotonic, Acoustic metamaterials and devices, Optical 3-D printing,
Nanofabrication instrument
Rm. 3-435B | 617-253-2247 | nicfang @ mit . edu

POSTDOCTORAL ASSOCIATES
Seok Kim, MechE
Shahrzad Ghaffari Mosanenzadeh, MechE

GRADUATE STUDENTS
Hui Feng Du, MechE
Xin Hao Li, MechE
Chu Ma, MechE
Zheng Jie Tan, DMSE

VISITORS
Youngtae Cho, Changwon National University
Will Liu, Hong Kong University
Yu Zhang, Xia Men University
Zhi Jia Zhang, Xian Jiaotong University

SUPPORT STAFF
Chevalley Duhart, Administrative Assistant

SELECTED PUBLICATIONS


Karen K. Gleason  
Associate Provost  
Alexander and I. Michael Kasser Professor  
Department of Chemical Engineering  

**POSTDOCTORAL ASSOCIATES**  
Meysam Heydari Gharahcheshmeh, ChemE  
Maxwell Robinson, ChemE  
Minghui Wang, ChemE  
Jungjie Zhao, ChemE  

**GRADUATE STUDENTS**  
Priya Moni, MatE  
Xiaoxue Wang, ChemE  

**UNDERGRADUATE STUDENT**  
Mofoluwaso Jebutu, ChemE  

**VISITORS**  
Saibal Mitra, University of Missouri, Columbia  
Wiebke Reichstein, Kiel University, Germany  

**SUPPORT STAFF**  
Alina Haverty, Administrative Assistant  

**SELECTED PUBLICATIONS**  


Jongyoon Han
Professor
Department of Electrical Engineering & Computer Science
Department of Biological Engineering

Nanofluidic / Microfluidic technologies for advanced biomolecule analysis and sample preparation; cell and molecular sorting, novel nanofluidic phenomena, biomolecule separation and pre-concentration, seawater desalination and water purification, neurotechnology.

Rm. 36-841 | 617-253-2290 | jyhan@mit.edu

POSTDOCTORAL ASSOCIATES
David Collins, SUTD / RLE
Hyungkook Jeon, RLE
Kerwin Keck, SMART Center
Yin Lu, SMART Center
Bee Luan Kho, SMART Center
Chenhui Peng, RLE
Hyunryul Ryu, RLE
Dhiraj Sinha, SUTD / RLE
Smitha Thamarath Surendran, SMART Center
Junghyo Yoon, RLE
Ying Zhou, SMART Center / SUTD

GRADUATE STUDENTS
Alex Barksdale, EECS
Kyungyong Choi, EECS
Matthew Flavin, EECS
Taehong Kwon, EECS
Wei Ouyang, EECS
Ching Ann Tee, SMART Center, NUS
Aoli Xiong, SMART Center, NTU
Chia-Chen ‘Debbie’ Yu, EECS

VISITORS
Aniruddh Sarkar, Ragon Institute
Lidan Wu, Broad Institute

SUPPORT STAFF
Cindy Higgins, Administrative Assistant

SELECTED PUBLICATIONS


*equal contributors
Ruonan Han
Associate Professor
Department of Electrical Engineering & Computer Science

POSTDOCTORAL ASSOCIATE
Xiang Yi, MTL

GRADUATE STUDENTS
Jack Holloway, EECS
Zhi Hu, EECS
Mohamed I. Ibrahim, EECS
Mohamed I. Khan, EECS
Mina Kim, EECS
James Mawdsley, EECS
Cheng Wang, EECS
Guo Zhang, EECS

UNDERGRADUATE STUDENTS
Ronald A. Davis, EECS
Nestor Franco, EECS
Weerachai (Junior) Neeranartvong, EECS

VISITORS
Lingshan Kong, Nanyang Technological University
Rui Ma, Mitsubishi Electric Research Labs
Zihan Wang, Fudan University

SUPPORT STAFF
Joanna Maclver, Administrative Assistant

SELECTED PUBLICATIONS


Song Han
Assistant Professor
Department of Electrical Engineering & Computer Science

Machine learning, artificial intelligence, model compression, Hardware accelerator, domain-specific architecture, FPGA, VLSI System.

Rm. 38-344 | 707-797-7288 | songhan@mit.edu

GRADUATE STUDENTS
Yujun Lin, EECS
Zhijian Liu, EECS
Hanrui Wang, EECS

VISITORS
Han Cai, Shanghai Jiaotong University
Jiacheng Yang, Shanghai Jiaotong University
Sherif Fawzy, University of Toronto
Kevin Nicholas Kiningham, Stanford University
Ji Lin, Tsinghua University

SELECTED PUBLICATIONS


S. Han, "Compressing and Regularizing Deep Neural Networks, Improving Prediction Accuracy using Deep Compression and DSD Training," O’Reilly invited article, Nov. 2016.


F. Iandola, S. Han, M. Moskewicz, K. Ashraf, W. J. Dally, and K. Keutzer, "SqueezeNet: AlexNet-level Accuracy with 50x Fewer Parameters and < 0.5MB Model Size," arXiv, 2016.

Juejun (JJ) Hu
Merton C. Flemings Associate Professor
Department of Materials Science & Engineering

Integrated photonics, optical thin films, glass and amorphous materials, silicon photonics, light management in photovoltaics, magneto-optical isolation, integration on unconventional substrates (polymers, optical crystals, 2-D materials, etc.), infrared imaging, spectroscopy, metasurface.

Rm. 13-4054 | 302-766-3083 | hujuejun @ mit.edu

RESEARCH SCIENTIST
Tian Gu, DMSE

POSTDOCTORAL ASSOCIATES
Lan Li, DMSE
Hongtao Lin, DMSE
Carlos A. Rios Ocampo, DMSE
Mikhail Shalaginov, DMSE
Shaoliang Yu, DMSE
Haijie Zuo, DMSE

GRADUATE STUDENTS
Skylar Deckoff-Jones, DMSE
Qingyang Du, DMSE
Sarah Geiger, DMSE
Derek Kita, DMSE
Jerome Michon, DMSE
Gufan Yin, DMSE
Yifei Zhang, DMSE

UNDERGRADUATE STUDENTS
Fayed Ali, MechE
Cedric Delmy, MechE

VISITOR
Bin Huang, Hunan University

SUPPORT STAFF
Cory James, Administrative Assistant

SELECTED PUBLICATIONS


Sang-Gook Kim
Professor
Department of Mechanical Engineering

GRADUATE STUDENTS
Haluk Akay, MechE
Xinhao Li, MechE
Ruize Xu, MechE

VISITOR
Zi-Xun Jia, Visiting Student

SUPPORT STAFF
Tony Pulsone, Administrative Assistant

SELECTED PUBLICATIONS


Jeehwan Kim
Class ’47 Career Development Associate Professor
Department of Mechanical Engineering
Department of Materials Science & Engineering

Two-dimensional material based layer transfer, brain-inspired neuromorphic computing, single-crystalline graphene electronics, advanced photovoltaics.
Rm. 38-276 | 617-324-1948 | jeehwan@mit.edu

POSTDOCTORAL ASSOCIATES
Sanghoon Bae, MechE
Shinhyun Choi, MechE
Wei Kong, MechE
Hyunseong Kum, MechE
Peng Lin, MechE
Hanwool Yeon, MechE

GRADUATE STUDENTS
Chanyeol Choi, EECS
Yunjo Kim, MechE
Kuangye Lu, MechE
Subeen Pang, MechE
Kuan Qiao, MechE
Seungchan Ryu, MechE
Scott Tan, MechE

VISITORS
Byunghun Lee, Yonsei University
Doyoon Lee, Hongik University

SUPPORT STAFF
Emilie Heilig, Administrative Assistant

SELECTED PUBLICATIONS


Jing Kong
Professor
Department of Electrical Engineering & Computer Science

POSTDOCTORAL ASSOCIATES
Giovanni Azzellino, RLE
Yunfan Guo, RLE
Qingqing Ji, RLE
Xiang Ji, RLE
WeiSun Leong, RLE
Nannan Mao, RLE
JiHoon Park, RLE
Mahdi Tavakoli, RLE
Xu Zhang, MTL
Jiayuan Zhao, RLE
Lin Zhou, RLE

GRADUATE STUDENTS
Marek Hempel, EECS
Angyu Lu, EECS
Luiz Gustavo Pimenta Martins, Physics
Pin-Chun Shen, EECS
Cong Su, NSE
Haozhe Wang, EECS

VISITORS
Bingnan Han, Beihang University
Jin Niu, Beijing University of Chemical Technology
Xiaoyan Zhu, China University of Geosciences

SUPPORT STAFF
Arlene Wint, Administrative Assistant

SELECTED PUBLICATIONS


Jeffrey H. Lang  
Vitesse Professor  
Department of Electrical Engineering & Computer Science

Analysis, design, and control of electro-mechanical systems with application to traditional rotating machinery and variable-speed drives, micro/nano-scale (MEMS/NEMS) sensors and actuators, flexible structures, and the dual use of actuators as force and motion sensors.

Rm. 10-176 | 617-253-4687 | lang @ mit . edu

POSTDOCTORAL ASSOCIATE  
Ujwal Radhakrishna, RLE

GRADUATE STUDENTS  
Alan Casallas, EECS  
Daibo Chen, EECS  
Mingye Gu, EECS  
Jinchu Han, EECS  
Rakesh Kumar, EECS  
Nathan Monroe, EECS  
Apoorva Murarka, EECS  
Alex Oliva, EECS  
Mark Yang, EECS

UNDERGRADUATE STUDENTS  
Daniel Sheen, EECS

VISITOR  
Dennis Buss, Texas Instruments

SUPPORT STAFF  
Donna Gale, Administrative Assistant  
Arlene Wint, Administrative Assistant

SELECTED PUBLICATIONS  


Hae-Seung Lee
ATSC Professor of Electrical Engineering & Computer Science
Director of Center for Integrated Circuits and Systems
Department of Electrical Engineering & Computer Science

Analog and Mixed-signal Integrated Circuits, with a Particular Emphasis in Data Conversion Circuits in Scaled CMOS.
Rm. 39-521 | 253-5174 | hslee@mtl.mit.edu

POSTDOCTORAL ASSOCIATE
Sungwon Chung, EECS

GRADUATE STUDENTS
Taehoon Jeong, EECS
Harneet Singh Khurana, EECS
Changwook Min, HST
Rishabh Mittal, EECS
Joohyun Seo, EECS
Xi Yang, EECS

SUPPORT STAFF
Elizabeth Kubicki, Administrative Assistant

PUBLICATIONS


Luqiao Liu  
Robert Shillman (1974) Career Development Assistant Professor  
Department of Electrical Engineering & Computer Science

Spintronics; spin-based logic and memory device; nanoscale magnetic material for information storage and microwave application; fabrication technique of magnetic nanodevices; spin-related phenomena in semiconductor, topological insulator, superconductors, and low dimensional material; magnetic dynamics

Rm. 39-553a | 617-253-0019 | luqiao@mit.edu

POSTDOCTORAL ASSOCIATES  
Yabin Fan  
Hailong Wang  
Yanfei Wu

GRADUATE STUDENTS  
Joseph Finley, EECS  
Jiahao Han, EECS  
Justin Hou, EECS  
Taqiyyah Safi, EECS  
Pengxiang Zhang, EECS

SUPPORT STAFF  
Steven O’Hearn, Administrative Assistant

SELECTED PUBLICATIONS  


Jurgen Michel  
Senior Research Scientist  
Materials Research Laboratory

**RESEARCH SCIENTIST**  
Bing Wang, SMART

**POSTDOCTORAL ASSOCIATE**  
Ruitao Wen, MRL

**GRADUATE STUDENTS**  
Yiding Lin, SMA3  
Danhao Ma, DMSE  
Xueying Zhao, DMSE

**SUPPORT STAFF**  
Cory James, Administrative Assistant

**SELECTED PUBLICATIONS**


Tomas Palacios  
Professor  
Department of Electrical Engineering & Computer Science

Design, fabrication, and characterization of novel electronic devices in wide bandgap semiconductors & 2-D materials, polarization & bandgap engineering, transistors for sub-mm wave power & digital applications, new ideas for power conversion & generation, interaction of biological systems with semiconductor materials & devices, large area & ubiquitous electronics based on 2-D materials.

Rm. 39-567a | 617-324-2395 | tpalacios @ mit . edu

POSTDOCTORAL ASSOCIATES
Jie Hu, MTL  
Amirhasan Nourbakhsh, MTL  
Noelia Vico Trivino, MTL  
Xu Zhang, MTL  
Yuhao Zhang, MTL

GRADUATE STUDENTS
Nadim Chowdhury, EECS  
Marek Hempel, EECS  
Sameer Joglekar, DMSE  
Yuxuan Lin, EECS  
Charles Mackin, EECS  
Elaine McVay, EECS  
Ayrton Munoz, EECS  
Joshua Perozek, EECS  
Daniel Piedra, EECS  
Qingyun Xie, EECS  
Mantian Xue, EECS  
Mengyang Yuan, EECS  
Ahmad Zubair, EECS

UNDERGRADUATE STUDENTS
Jacob Pritzker, EECS  
Mark Theng, EECS  
Ertem Nusret Tas, EECS

SUPPORT STAFF
Joseph Baylon, Administrative Assistant

SELECTED PUBLICATIONS


Jennifer L. M. Rupp
Thomas Lord Assistant Professor of Materials Science & Engineering
Department of Materials Science & Engineering
Assistant Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Rm. 8-242 | 617-253-4477 | jrupp@mit.edu

POSTDOCTORAL ASSOCIATES
Alexander Bork, NSE
Alfonso Carrillo, DMSE
Juan Carlos Gonzalez-Rosillo, DMSE
Zachary Hood, DMSE, NSF Fellowship
Kunjoong Kim, DMSE

GRADUATE STUDENTS
Thomas Defferriere, DMSE
Reto Pfenninger, DMSE, ETH Zurich, CH
Eva Sediva, DMSE, ETH Zurich, CH
Philipp Simons, DMSE
Yuntao Zhu, DMSE

UNDERGRADUATE STUDENTS
Neil Aggarwal, DMSE
Christopher M. Eschler, DMSE
Claire Halloran, DMSE
Erick Hernandez, DMSE
Kaitlyn M. Mullin, DMSE
Noa Schwartz, DMSE

VISITORS
Marco Gysel, ETH Zurich, CH
Jonathan Spring, ETH Zurich, CH

SUPPORT STAFF
Priyanka Chaudhuri, Administrative Assistant

SELECTED PUBLICATIONS


Charles G. Sodini
LeBel Professor
Department of Electrical Engineering & Computer Science

Electronics and integrated circuit design and technology. Specifically, his research involves technology intensive integrated circuit and systems design, with application toward medical electronic devices for personal monitoring of clinically relevant physiological signals.
Rm. 39-527b | 617-253-4938 | sodini@mtl.mit.edu

COLLABORATORS
Sam Fuller, Analog Devices, Inc.
Tom O’Dwyer, Analog Devices, Inc.

GRADUATE STUDENTS
Kyle Beeks, EECS
Maggie Delano EECS
Sidney R. Primus, EECS
Joohyun Seo, EECS

SUPPORT STAFF
Joanna MacIver, Administrative Assistant

SELECTED PUBLICATIONS


Vivienne Sze
Associate Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Joint design of signal processing algorithms, architectures, VLSI and systems for energy-efficient implementations. Applications include computer vision, machine learning, autonomous navigation, image processing and video coding.

Rm. 38-260 | 617-324-7352 | sze @ mit . edu

GRADUATE STUDENTS
Yu-Hsin Chen, EECS (co-advised with Joel Emer)
Hsin-Yu Lai, EECS (co-advised with Thomas Heldt)
James Noraky, EECS
Gladynel Saavedra Pena, EECS (co-advised with Thomas Heldt)
Amr Suleiman, EECS, ODGE Fellowship
Mehul Tikekar, EECS (co-advised with Anantha Chandrakasan)
Yannan Nellie Wu, EECS, EECS Department Fellowship (co-advised with Joel Emer)
Tien-Ju Yang, EECS
Zhengdong Zhang, EECS

UNDERGRADUATE STUDENTS
Valerie Sarge, EECS
Diana Wofk, EECS

SUPPORT STAFF
Janice L. Balzer, Administrative Assistant

SELECTED PUBLICATIONS


Carl V. Thompson  
Stavros Salapatas Professor of Materials Science and Engineering  
Department of Materials Science & Engineering  
Processing and property optimization of thin films and nanostructures for applications in electronic, microelectromechanical, and electrochemical devices and systems. Interconnect and device reliability.  
Rm. 13-5069 | 617-253-7652 | cthomp@mit.edu

RESEARCH SCIENTIST  
Wardhana Sasangka, SMART

POSTDOCTORAL ASSOCIATES  
Michael Chon, MRL  
Pushpendra Kumar, SMART  
Baoming Wang, MRL  
Xinghui Wang, SMART

GRADUATE STUDENTS  
Thomas Batcho, DMSE  
Maxwell L’Etoile, DMSE  
Jinghui, Miao, DMSE  
Yoon Ah Shin, DMSE  
Lin Xu, DMSE  
Gao Yu, SMA3 Fellow, NTU

VISITORS  
Seong-Ho Baek, Daegu Gyeongbuk Institute of Science & Technology  
Andrea Giunto, École Polytechnique Fédérale de Lausanne  
Daniele Perego, Paul Scherer Institute, SMART  
Berke Piskin, Middle East Technical Institute  
Annie Weathers, Lincoln Laboratory

SUPPORT STAFF  
Sarah Ciriello, Administrative Assistant

SELECTED PUBLICATIONS  


Harry L. Tuller
Professor
Department of Materials Science & Engineering

Energy related materials, solid oxide fuel cells, transparent conductive oxides, resonant and chemoresistive sensors, thin film transistors, memory devices.

Rm. 13-3126 | 617-253-6890 | tuller@mit.edu

POSTDOCTORAL ASSOCIATES
Dima Kalaev, MRL
Clement Nicollet, MRL

GRADUATE STUDENTS
Michael Campion, DMSE
Thomas Defferriere, DMSE
Changsub Kim, DMSE
Sunho Kim, DMSE

VISITORS
Alexis Grimaud, CNRS Paris
George Harrington, Kyushu University
Dino Klotz, Kyushu University
Nicola Perry, Kyushu University
Jonathan Polfus, SINTEF, Oslo

SUPPORT STAFF
Elisabeth Anderson, Administrative Assistant

SELECTED PUBLICATIONS


Luis Fernando Velásquez-García  
Principal Research Scientist  
Microsystems Technology Laboratories

Micro- and nano-enabled multiplexed scaled-down systems that exploit high electric field phenomena; powerMEMS, additively manufactured MEMS/NEMS. Actuators, cold cathodes, nanosatellite propulsion, ionizers, microplasmas, portable mass spectrometry, pumps, sensors, X-ray sources.

Rm. 39-415B | 617-253-0730 | lfvelasq @ mit . edu

POSTDOCTORAL ASSOCIATES
Chenye Yang, MTL

GRADUATE STUDENTS
Ashley L. Beckwith, MechE  
Yosef S. Kornbluth, EECS  
Zhumei Sun, MechE

VISITORS
Brenda García Farrera, Tecnológico de Monterrey  
Erika García Lopez, Tecnológico de Monterrey  
Imperio Anel Perales Martínez, Tecnológico de Monterrey  
Emmanuell Segura Cárdenas, Tecnológico de Monterrey  
Alan Osiris Sustaita Narváez, Tecnológico de Monterrey  
Anthony Taylor, Edwards

SUPPORT STAFF
Valerie DiNardo, Administrative Assistant

SELECTED PUBLICATIONS


Joel Voldman
Professor
Associate Department Head
Department of Electrical Engineering & Computer Science

Microtechnology for basic cell biology, applied cell biology, Immunology, and human health.

Rm. 36-824 | 617-253-2094  | voldman @ mit . edu

---

POSTDOCTORAL ASSOCIATES
Dohyun Lee, RLE
Sarvesh Varma, RLE

GRADUATE STUDENTS
Nicha Apichitsopa, EECS
Alex Jaffe, EECS
Jaemyon Lee, EECS
Dan Wu, MechE

GRADUATE STUDENTS


SELECTED PUBLICATIONS


Materials comprising carbon nanotubes (CNT), such as hierarchical nanoeengineered advanced composites for aerospace applications are promising new materials thanks to their mechanical and multifunctional properties.

Rm. 33-408 | 617-252-1539 | wardle@mit.edu

POSTDOCTORAL ASSOCIATES
Luiz Acauan, AeroAstro
Estelle Cohen, AeroAstro
Kehang Cui, AeroAstro
Itai Stein, AeroAstro
Yue Zhou, AeroAstro

GRADUATE STUDENTS
Fred Daso, AeroAstro
Nathan Fritz, MechE
Ashley Kaiser, DMSE
Reed Kopp, AeroAstro
Jeonyoon Lee, MechE
Richard Li, AeroAstro
Xinchen Ni, MechE

UNDERGRADUATE STUDENTS
Alan Alahmad, AeroAstro
Samuel Belden, DMSE
Travis Hank, AeroAstro
Casimir Lesperance, MechE
Clementine Mitchell, AeroAstro
Sofi Peterson, MechE
Amy Vanderhout, AeroAstro

VISITORS
Heena Mutha, MechE
Diemut Strebe, CAST Visiting Artist
Carlos Teixeira, Porto, Portugal

SUPPORT STAFF
Britton ‘Bryt’ Bradley, Administrative Assistant
John Kane, Research Specialist

SELECTED PUBLICATIONS


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- James Mawdsley (R. Han)
  Low-Noise Frequency Synthesizer for a Sub-mm-Wave Carbonyl Sulphide Molecule Clock

- Diana Wolk (V. Sze)
  Energy-Efficient Deep Neural Network for Depth Prediction

- Dale Lidston (B. L. Wardle)
  Synthesis, Characterization, and Mode I Fracture Toughness of Aligned Carbon Nanotube Polymer Matrix Nanocomposites

- Andrew Maclinnes (V. M. Bove, Jr.)
  Minimization of Aberrations for the Mark IV Holographic Architecture using Optical Software Modeling
  lang@mit.edu

- Boying Meng (J. Voldman)
  Reconfigurable Neural Probe for Chronic Recording

- Sidney Primas (C. G. Sodini)
  The AutoScope: An Automated, Low-Cost Urinalysis System for the Point-of-Care

- Mihika Prabhu (D. R. Englund)
  Towards Optimal Capacity-achieving Transceivers with Photonic Integrated Circuits

- Ali Shtarbanov (V. M. Bove, Jr.)
  AirTap: A Multimodal Interactive Interface Platform with Free-space Cutaneous Haptic Feedback via Toroidal Air-vortices

- Tathaga Srimani (A. P. Chandrakasan)
  Energy Efficient Computing: From Nanotubes To Negative Capacitance

- Zhumei Sun (L. F. Velásquez-García)
  Exploration of Metal 3-D Printing Technologies for the Microfabrication of Freeform, Finely Featured, Mesoscaled Structures

- Richard Swartwout (V. Bulović)
  Smoothing Silver Nanowires for Optoelectronic Applications

- Emily Toomey (K. K. Berggren)
  Microwave Response of Nonlinear Oscillations in Resistively Shunted Superconducting Nanowires

- Miaorong Wang (A. P. Chandrakasan)
  Algorithms and Low-Power Hardware for Keyword Spotting Applications

- Tien-Ju Yang (V. Sze)
  Neural Network Simplification Using A Progressive Barrier Based Approach*

S.M.

- Navid Abedzadeh (K. K. Berggren)
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- Haluk Akay (S.-G. Kim)
  Low-Frequency Vibrational Energy Harvesting at the Micro and Meso Scale

- Ashley Beckwith (L.F. Velásquez-García)
  Additive Manufacturing of Microfluidics for Evaluation of Immunotherapy Efficacy

- Eric Bersin (D. R. Englund)
  Super-resolution Localization and Readout of Individual Solid-state Qubits

- Pedro Colon-Hernandez (V. M. Bove, Jr.)
  Hover: A Wearable Object Identification System for Audio Augmented Reality Interactions

- Erik Eisenach (D. R. Englund and D. A. Braje)
  Tunable and Broadband Loop Gap Resonator For Coherent Control Of Nitrogen Vacancy Centers In Diamond

- Nathan Fritz (B. L. Wardle)
  Micro Computed Tomography for Interlaminar Analysis, Void Quantification, and Feature Localization in Carbon Fiber Composites

- Cornwell Hayden (B. L. Wardle)
  Tensile and Interfacial Properties of Radially Aligned CNT Grown Carbon Fibers

- Taehoon Jeong (A. P. Chandrakasan and H.-S. Lee)
  A Pipelined Analog-to-Digital Converter with Low-gain, Low-bandwidth Op-Amps

- Yosef Kornbluth (L. F. Velásquez-García)
  Focused Atmospheric-pressure Microsputterer for Additive Manufacturing of Microelectronics Interconnects

- Germain Martinez (D. S. Boning)
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- **Daniel Moon** (D. S. BONING)
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- **Valerie Sarge** (V. SZE)
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- **Nigel Chou** (S. M. MANALIS)
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- **Maggie Delano** (C. G. SODINI)
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  Theory and Modeling of Field Electron Emission from Low-dimensional Electron Systems
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  Design-space and Scalable Technology for GaN Based Power Transistors
- **Edwina Portocarrero Navarro** (V. M. BOVE, JR.)
  Networked Playscapes: Redefining the Playground
- **Priyanka Raina** (A. P. CHANDRAKASAN)
  Energy-efficient Circuits and Systems for Computational Imaging and Vision on Mobile Devices
- **Andy Shih** (A. I. AKINWANDE)
  Flexible and Solution-Processed Organic Thin Film Transistors for High Voltage Applications
- **Ren-Jye Shiue** (D. R. ENGLUND)
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- **Katia Shtrykova** (E. P. IPPEN)
  Fully Integrated CMOS-compatible Mode-locked Lasers
- **Amr Suleiman** (V. SZE)
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- **Mehul Tikekar** (A. P. CHANDRAKASAN AND V. SZE)
  Energy-efficient Video Decoding using Data Statistics
- **Matthew Trusheim** (D. R. ENGLUND)
  Nanoscale Engineering of Spin-based Quantum Devices in Diamond
- **Tony Wu** (M. A. BALDO)
  Development in Utilizing Singlet Fission and Triplet-Triplet Annihilation to improve Solar Cell Efficiency
- **Ruize Xu** (S.-G. KIM)
  Low-frequency, Low-amplitude MEMS Vibration Energy Harvesting
Glossary

TECHNICAL ACRONYMS

ADC  Analog-to-Digital Converters
CMOS  Complementary Metal–Oxide–Semiconductor
CNT  Carbon Nanotubes
ECP  Electro-chemical Plating
FET  Field-effect Transistor
HSQ  Hydrogen Silsesquioxane
InFO  Integrated Fan Out
MOSFET  Metal–Oxide–Semiconductor Field-effect Transistor
nTRON  Nanocryotron
RDL  Re-distribution Layers
RIE  Reactive ion etching
SNSPDs  Superconducting nanowire single photon detectors
SS  Subthreshold swing
TMAH  Tetramethylammonium Hydroxide
TREC  Thermally regenerative electrochemical cycle

MIT ACRONYMS & SHORTHAND

BE  Department of Biological Engineering
Biology  Department of Biology
ChemE  Department of Chemical Engineering
CICS  Center for Integrated Circuits and Systems
CMSE  Center for Materials Science and Engineering
IRG  Interdisciplinary Research Group
DMSE  Department of Materials Science & Engineering
EECS  Department of Electrical Engineering & Computer Science
ISN  Institute for Soldier Nanotechnologies
KI  David H. Koch Institute for Integrative Cancer Research
LL  Lincoln Laboratory
MAS  Program in Media Arts & Sciences
MechE  Department of Mechanical Engineering
MEDRC  Medical Electronic Device Realization Center
MIT-CG  MIT/MTL Center for Graphene Devices and 2D Systems
MITEI  MIT Energy Initiative
MIT-GaN  MIT/MTL Gallium Nitride (GaN) Energy Initiative
Glossary

MISTI  MIT International Science and Technology Initiatives
MIT-SUTD  MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech  MIT Skoltech Initiative
MTL  Microsystems Technology Laboratories
NSE  Department of Nuclear Science & Engineering
Physics  Department of Physics
Sloan  Sloan School of Management
SMA  Singapore-MIT Alliance
↑ SMART  Singapore-MIT Alliance for Research and Technology Center
↑ SMART-LEES  SMART Low Energy Electronic Systems Center
SUTD-MIT  MIT-Singapore University of Technology and Design Collaboration Office
UROP  Undergraduate Research Opportunities Program

U.S. GOVERNMENT ACRONYMS

AFOSR  U.S. Air Force Office of Scientific Research
↑ FATE-MURI  Foldable and Adaptive Two-dimensional Electronics Multidisciplinary Research Program of the University Research Initiative
AFRL  U.S. Air Force Research Laboratory
ARL  U.S. Army Research Laboratory
↑ ARL-CDQI  U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO  Army Research Office
ARPA-E  Advanced Research Projects Agency - Energy (DOE)
DARPA  Defense Advanced Research Projects Agency
↑ DREaM  Dynamic Range-enhanced Electronics and Materials
DoD  Department of Defense
DoE  Department of Energy
↑ EFRC  U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA  U.S. DoD Defense Threat Reduction Agency
IARPA  Intelligence Advanced Research Projects Activity
↑ RAVEN  Rapid Analysis of Various Emerging Nanoelectronics
NASA  National Aeronautics and Space Administration
↑ GSRP  NASA Graduate Student Researchers Project
NDSEG  National Defense Science and Engineering Graduate Fellowship
NIH  National Institutes of Health
↑ NCI  National Cancer Institute
NNSA  National Nuclear Security Administration
NRO  National Reconnaissance Office
NSF  National Science Foundation
\textsuperscript{t}CBMM  NSF Center for Brains, Minds, and Machines
\textsuperscript{t}CIQM  Center for Integrated Quantum Materials
\textsuperscript{t}CSNE  NSF Center for Sensorimotor Neural Engineering
\textsuperscript{t}E3S  NSF Center for Energy Efficient Electronics Science
\textsuperscript{t}GRFP  Graduate Research Fellowship Program
\textsuperscript{t}IGERT  NSF The Integrative Graduate Education and Research Traineeship
\textsuperscript{t}NEEDS  NSF Nano-engineered Electronic Device Simulation Node
\textsuperscript{t}SEES  NSF Science, Engineering, and Education for Sustainability
\textsuperscript{t}STC  NSF Science-Technology Center
ONR  Office of Naval Research
\textsuperscript{t}PECASE  Presidential Early Career Awards for Scientists and Engineers

OTHER ACRONYMS

CNRS Paris  Centre National de la Recherche Scientifique
CONACyT  Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE  Institute of Electrical and Electronics Engineers
IHP Germany  Innovations for High Performance Microelectronics Germany
KIST  Korea Institute of Science and Technology
KFAS  Kuwait Foundation for the Advancement of Sciences
MASDAR  Masdar Institute of Science and Technology
NTU  Nanyang Technological University
NUS  National University of Singapore
NYSCF  The New York Stem Cell Foundation
SRC  Semiconductor Research Corporation
\textsuperscript{t}NEEDS  NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD  Singapore University of Technology and Design
TEPCO  Tokyo Electric Power Company
TSMC  Taiwan Semiconductor Manufacturing Company
# Principal Investigator Index

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