

Microsystems Annual Research Report



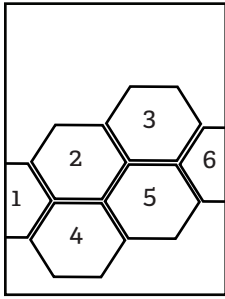
2023

MTL ● MICROSYSTEMS
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1. "Chip micrograph of energy-adaptive transformer accelerator for low power IoT applications," submitted by Alex Ji, EECS
2. "A biomimetic robot module that has landed on a cactus," submitted by Suhan Kim, EECS
3. "Mediating Cell Adhesion Using Microtextured Polystyrene Surfaces," C. McCue, A. Atari, S. Parks, M. Tseng, and K. K. Varanasi, p. 5.
4. "THz transceiver chip to be used inside the refrigerator of future quantum computers," submitted by Jinchen Wang, EECS
5. "A GaN arithmetic logic unit (ALU) based on MIT's high temperature GaN-on-Si platform," submitted by Qingyun Xie and Mengyang Yuan, EECS.
6. "Chamber Design of a Portable Breathalyzer for Disease Diagnosis," D. Morales, M. Xue, and T. Palacios, p. 6.

Microsystems Annual Research Report 2023

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Tomás Palacios, Vladimir Bulović
Meghan Melvin, Jami L. Mitchell
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CONTENTS

Foreword i

Acknowledgments ii

RESEARCH ABSTRACTS

Biology, Medical Devices, and Systems 1

Circuits and Systems 12

Devices (Electronic, Magnetic, Superconducting) 21

Energy and Sustainability 44

Integrated Photonics and Optoelectronics 50

Machine Learning and Other Accelerators 62

MEMS, Thermal, Fluidic Devices, and Robotics 79

Nanoscience, Nanotechnology, Nanomaterials 87

Quantum Science and Engineering 106

Semiconductor Manufacturing and Supply Chain 111

Research Centers 116

Faculty Profiles 120

Theses Awarded 158

Startups Affiliated with MTL and MIT.nano Faculty 160

Glossary 162

Principal Investigator Index 165

Foreword

We are happy to announce the publication of the 2023 Microsystems Annual Research Report, a joint publication between the Microsystems Technology Laboratories (MTL) and MIT.nano, for the academic year July 1, 2022 to June 30, 2023.

This annual report summarizes some of the many accomplishments of the MIT microsystems community during the last year. This fall we mark the 5th anniversary of MIT.nano and in 2024 we will acknowledge the 40th anniversary of MTL's founding. As we celebrate these milestones, we are proud to celebrate the many ways that we continue to promote and advance research in semiconductor materials, technology, devices, circuits, and systems, as well as other frontiers in nanoscale science and engineering. We are at a very exciting time for microelectronics, and we all have an important call to action to help push the field to new limits. MTL, in close partnership with MIT.nano and its amazing fabrication and characterization facilities, is ready for the challenge.

MTL has served as a model for interdisciplinary and collaborative research, education, and industrial outreach at MIT since its founding 40 years ago. This report summarizes this year's progress on more than 100 different research projects in many areas of micro- and nanotechnology from advanced semiconductor materials, new devices, integrated photonics, and circuits, to insect-scale micro robots, biomedical systems, and AI hardware accelerators, among many others.

On behalf of MTL and MIT.nano, we would like to thank every contributor to this year's Microsystems Annual Research Report, as well as the staff of both organizations who worked tirelessly to produce this exciting snapshot of our research.

Tomás Palacios
Director, Microsystems Technology Laboratories

Vladimir Bulović
Director, MIT.nano

July 2023

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Biology, Medical Devices, and Systems

Model-based Noninvasive Intracranial Compliance and Vascular Resistance Estimation	2
CNT-coated Paper Electrospray Sources for Mass Spectrometry	3
Heart Rate Varies with Mental Workload and Performance in Virtual Reality Flight Tasks.....	4
Mediating Cell Adhesion Using Microtextured Polystyrene Surfaces.....	5
Chamber Design of a Portable Breathalyzer for Disease Diagnosis.....	6
Feedback Regulator and Estimation Filter Implementable Using Bio/Nano Chemistry and Useful for “Intelligent Design”	7
Accelerating the Optimization of Vertical Flow Assay Performance Guided by a Rational Systematic Model-based Approach.....	8
Cvb Machine Learning for Arterial Blood Pressure Prediction.....	9
Progress and Challenges with Implantable Microphones for Cochlear Implants.....	10
A High-throughput Open-well Microfluidic Organ-on-chip System for Blood-brain Barrier	11

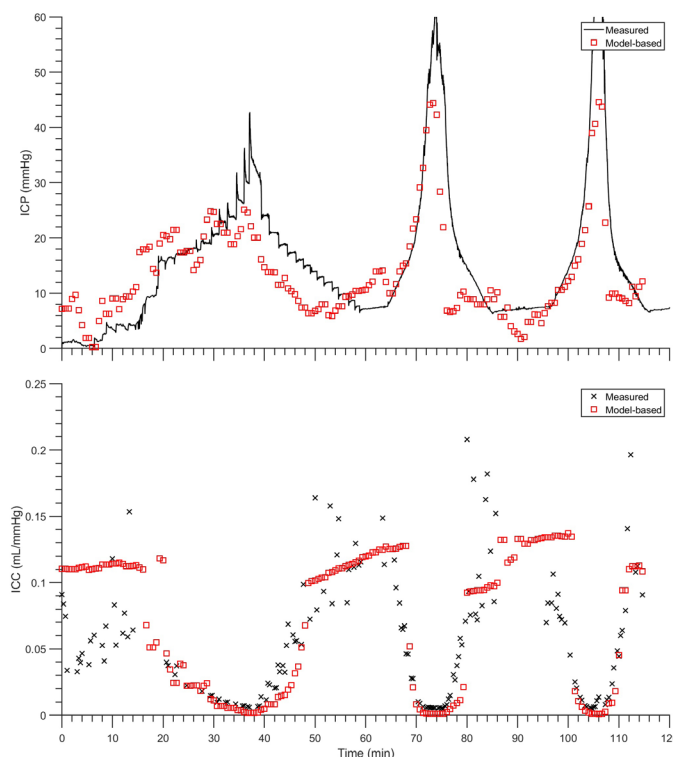
Model-based Noninvasive Intracranial Compliance and Vascular Resistance Estimation

S. M. Imaduddin, C. G. Sodini, T. Heldt

Sponsorship: Analog Devices, Inc. via MIT Medical Electronic Device Realization Center

Existing neuromonitoring methods used for patients with severe head injury tend to be highly invasive and carry a risk of tissue damage and infection. In particular, fluid infusion/withdrawal studies via indwelling catheters are needed to determine intracranial compliance (ICC)—an index of the propensity of rise in intracranial pressure (ICP) in response to changes in cranio-spinal volume. Despite their potential to serve as early indicators of intracranial hypertension, ICC measurements are rarely performed owing to time-consuming, invasive measurement protocols. In addition, measurements of cerebrovascular resistance (CVR) to blood flow are useful in assessing cerebral autoregulation and tracking pathological vascular narrowing such as in moyamoya disease. Like ICC, however, CVR is not regularly obtained at the bedside as the requisite measurements—arterial blood pressure (ABP), cerebral arterial blood flow (CBF), and ICP—are rarely monitored simultaneously.

We have developed a noninvasive, model-based approach for ICP, ICC, and CVR estimation that is driven by subjects' ABP and CBF measurements. Our system was initially validated qualitatively in healthy adult volunteers undergoing head-up tilts. We are now in the process of quantitatively validating our approach in an animal model. ICP is raised experimentally and measurements of the ABP, CBF, ICP, ICC, and CVR are acquired. Model-based estimates of the ICP, ICC, and CVR are then compared to invasive reference measurements. Initial results suggest that our model-based estimates are close to the reference measurements; further validation is now underway. Simultaneously, we have deployed our data collection approach at Boston Children's Hospital to evaluate the system's efficacy in pediatric patient cohorts. If proven successful, our approach can pave the way towards convenient and safe neuromonitoring across a wide spectrum of pathologies, patient age, and disease severity.



▲ Figure 1: Illustration of invasive measurements and model-based estimates of ICP and ICC, respectively, for one subject in the rabbit model.

CNT-coated Paper Electrospray Sources for Mass Spectrometry

A. Kachkine, L. F. Velásquez-García
Sponsorship: Empiriko Corporation

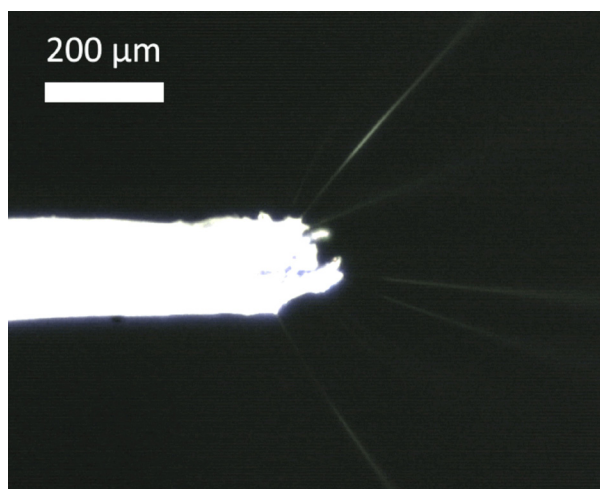
Clinical mass spectrometry (MS) requires high-performance and low-cost ion sources. Classical electrospray, based on jetting of ions from an electrically stressed liquid, can be accomplished with carbon nanotube (CNT)-coated paper as a substrate. In this study we investigated the properties of such emitters, finding unambiguous classical behavior in opposition to reported low-voltage activation of some CNT paper sources in the literature. We suspect that nebulization or other statistical ion formation phenomena, but not electrospray, underly their behavior.

CNT-coated paper sources are made by dip-coating grade 5 chromatography paper triangles in a 0.04 wt% dispersion of CNTs in N-N dimethylformamide. Emitters were positioned 1 mm away from a cylindrical capillary inlet of a portable MS instrument (Bayspec Continuity). Five- μL droplets of 95% methanol and 5% water spiked with 10 pharmaceutically relevant compounds at 1 $\mu\text{g}/\text{ml}$ were deposited on the emitters

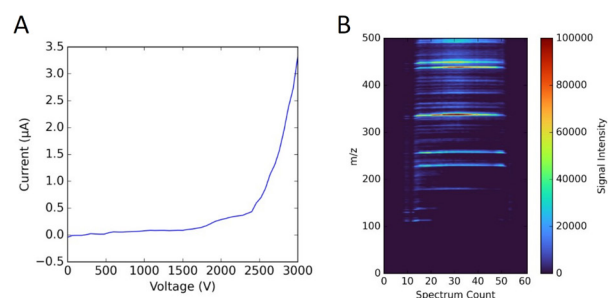
prior to voltage application.

Optical characterization (Figure 1) shows the formation of many jets at the protrusions of individual paper fibers, with solvent reaching them via the surface porosity introduced by the CNTs. Electrical and MS characterization (Figure 2) shows a startup voltage of about 1.5 kV and sufficient signal intensity for compound identification. No ionization is observed at low voltages.

The oft-repeated hypothesis that electric fields at CNT tips drive ambient ionization is incommensurate with fluid physics and optical results here; solvents fully wet forests of nanoscale features. We suspect that low-voltage ionization mechanics underly results reported in the literature, with potential relevance of vibrating edge nebulizers and the specific targets being analyzed. Further characterization, especially optical, is needed of low-voltage CNT paper sources to corroborate any conclusions on ionization mechanics.



▲ Figure 1: Optical image showing steady state electrospray at 2.5 kV, with several jets emerging from paper follicles.



▲ Figure 2: A) I-V plot of 5 replicates showing electrospray formation beginning at 1.5 kV. B) MS transient spectrum showing clear peaks of targets during steady state operation at 3.0 kV. We record no ionization at voltages <1 kV.

FURTHER READING

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Heart Rate Varies with Mental Workload and Performance in Virtual Reality Flight Tasks

J. Koerner, H. M. Rao, K. McAlpin, G. Ciccarelli, T. Heldt

Sponsorship: MIT Presidential Fellowship, NSERC Doctoral Scholarship (Application ID PGSD3-547366-2020), U.S. Air Force Research Laboratory and U.S. Air Force Artificial Intelligence Accelerator (Cooperative Agreement No. FA8750-19-2-1000)

Heart rate (HR) has been shown to correlate with cognitive metrics, particularly mental workload, in a variety of settings. In real aviation settings, there is broad consensus that HR is positively correlated with mental workload which makes HR an ideal signal to track as a potential surrogate for mental workload. With the growing use of virtual reality (VR) in different areas of training and education, including pilot training, the question arises if the same relationship between HR and mental workload holds in VR-simulated environments. To this end, this work investigates HR responses derived from electrocardiogram (ECG) recordings in 20 subjects performing flight maneuvers in a VR setting and explores the relationship between HR, mental workload, and flight performance. We find that mean HR increases by 2% ($p < 0.05$) across difficulty levels of the virtual flight scenario, decreases by 5% ($p < 0.01$)

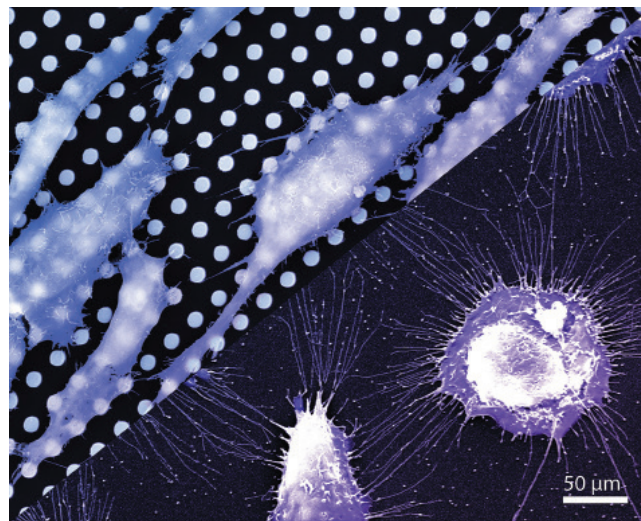
across repeated runs of the same difficulty level, and increases by 3% ($p < 0.01$) during the final landing period (with respect to the beginning of the flight). We observe HR to mirror the trend in mental workload and find a statistically significant correlation between HR and flight performance across different flight phases. Although the effect size observed is moderate, the findings are statistically significant and consistent across participants' experience levels. Our findings lend credence to the use of VR simulators for training purposes, and to the idea of titrating training difficulty based on real-time physiological responses in VR-simulated environments. Finally, we show that the ECG-derived HR trends can similarly be derived from photoplethysmography (PPG) signals. Given the existence of PPG sensors approved for cockpit use in real aircraft, our findings have significance beyond the VR setting.

Mediating Cell Adhesion Using Microtextured Polystyrene Surfaces

C. McCue, A. Atari, S. Parks, M. Tseng, K. K. Varanasi
Sponsorship: Broad SPARC Grant, MIT-Takeda Fellowship

Enzymatic cell detachment strategies for cell culture are popular, but are labor-intensive, can potentially lead to accumulation of genetic mutations, and produce large quantities of waste. Thus, there is a need for surfaces that lower cell adhesion strength while maintaining cell growth to enable enzyme-free cell culture. In this study, we investigated the use of microtexture alone to control cell adhesion. We developed a fast, simple, and inexpensive process for creating microtextured polystyrene surfaces. This fabrication method can transform any design produced with traditional lithography into a PDMS stamp with which we can mold polystyrene, and can be easily scaled for high throughput cell culture as well as create high aspect ratio mi-

cron-sized features with high precision and reproducibility. These cell culture surfaces enable decreased cell adhesion strength while maintaining high cell viability and proliferation through a simple reduction in the cell-surface contact area. Using image analysis to quantify cell morphology, we found that surface textures decreased cell area by half and led to much more elongated cell shape compared to flat surfaces. We designed a microfluidic shear force measurement platform to quantify the removal of cells from these surfaces, and showed that significantly more cells were removed from the microtextured surfaces than the flat surfaces, demonstrating that our surfaces lead to decreased cell adhesion.



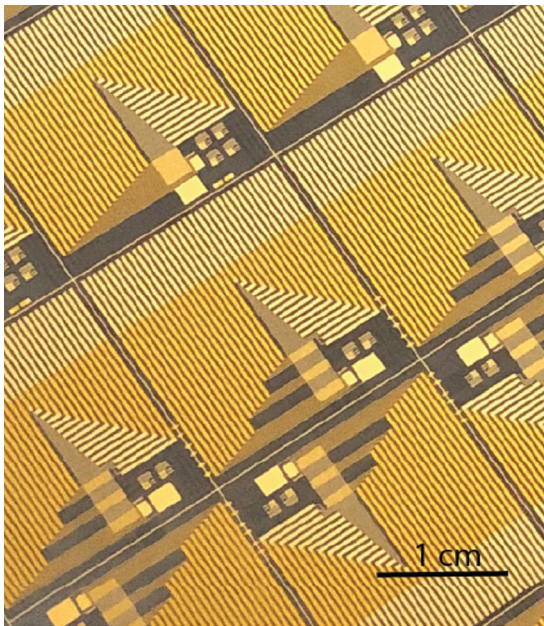
▲ Figure 1: SEM image of MG63 cancer cells grown on microtextured polystyrene (left), compared with cells grown on flat polystyrene (right), showing how surface texture alone can significantly change cell morphology.

Chamber Design of a Portable Breathalyzer for Disease Diagnosis

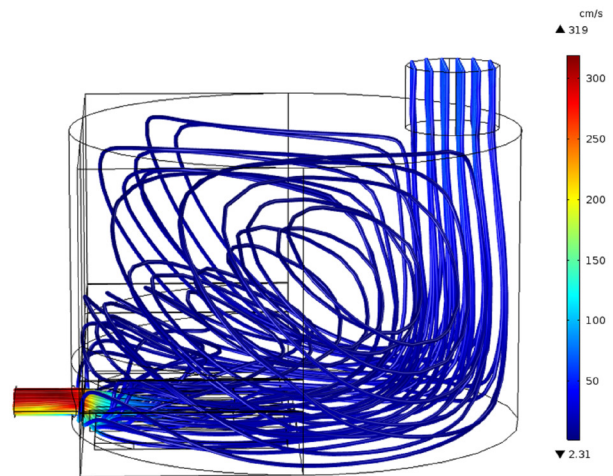
D. Morales, M. Xue, T. Palacios
Sponsorship: NSF Center for Integrated Quantum Materials

Our group has built a graphene-based sensor array that can accurately measure the concentration and type of different chemicals of interest. In this project, we have developed a chamber design that allows using this sensor as a portable breathalyzer for non-invasive, cheap, and fast diagnosis of diseases. Although significant research has been made in this field over the years, none has focused on the optimal chamber design of these devices, which has to optimize contact between sensors and air samples and address issues such as moisture, air velocity control, recirculation, and turbulence. Our work studies the airflow properties in different cylindrical chamber models and, with the help of fluid mechanics simulations and experiments with the analysis sensors, attempts to create a reusable in situ breathalyzer design. These results will help develop devices for use in clinical trials; in the future, the devices may be used to diagnose diabetes, Parkinson's Disease, and other conditions.

The current device consists of two chambers that are separate but connected by a piece that acts as the roof of the bottom chamber and the base of the top chamber. The measuring sensor is placed on this piece. The top chamber is designed to house a heater that can enhance the sensor's performance and accelerate drying when necessary. It also contains a humidity sensor, which is crucial for correctly interpreting the results obtained. The bottom chamber contains three stacked printed circuit boards that are screwed to the middle piece. The cables for all the components of the top chamber pass through this piece and are connected to the boards. The device is completely wireless and has a Bluetooth antenna, which allows it to send data to a mobile app that is connected to a database which is used for storing, visualizing, and analyzing the data.



▲ Figure 1: Microscope image of the graphene-based sensor array fabricated on a 4-inch wafer.



▲ Figure 2: Upper chamber fluid mechanics simulations.

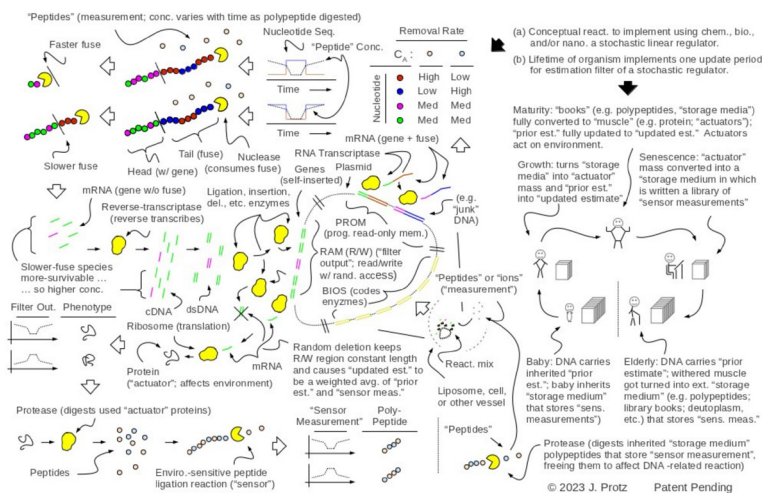
Feedback Regulator and Estimation Filter Implementable Using Bio/Nano Chemistry and Useful for “Intelligent Design”

J. Protz

Sponsorship: Protz Lab Group and the former BioMolecular Nanodevices, LLC

Information storage in polymers has been a focus of the performer for two decades and has recently become of greater interest at MIT. The present effort explores chemical and biological implementation of a stochastic linear regulator. It builds on a conceptual reaction mixture considered by the performer two years ago. First, “PROM”-type “junk DNA” in a plasmid transcribes into mRNA strands that are attacked by exonucleases coded for in a basic input/output system region of the plasmid; the activity of the nucleases depends jointly on the species of nucleotide being removed and on peptides pulled from polypeptides present alongside the plasmid. This activity causes the mix of surviving mRNA to depend on the polypeptide composition. The surviving mRNA reverse-transcribes into DNA that overwrites partly a random-access memory region of coding DNA in the plasmid, evolving it from a “prior estimate” of the environmental state to an “updated estimate” of it. This DNA expresses phenotypically as “actuator” proteins that are

assembled by ribosomes from the free peptides and that “actuate” the surrounding environment. Separately, a “sensor” reaction uses proteases and environmentally-sensitive peptide ligation reactions to recycle used “actuator” proteins back into free peptides that are then assembled into the aforementioned “sensor measurement”-storing polypeptides. One period of this cycle represents one update interval for an estimation filter. Implemented in a cell or organism, with the “sensor measurement”-storing polypeptides doubling as, e.g., a spindle apparatus or yolk, the lifetime of one cell or organism could constitute one update cycle of a stochastic regulator implemented by way of a cell line, organism family line, or society. Progress on this effort may allow the engineering of cell lines that evolve themselves and their environment deterministically according to “intelligent design” and also explain the existence of aging, death, reproduction, and variable life expectancy.



▲ Figure 1: (a) Schematic illustration of a conceptual reaction that implements a feedback regulator and estimation filter; (b) when implemented in a multi-generation cell line, one generation's lifetime implements one update period of a stochastic regulator useful in “intelligent design.”

FURTHER READING

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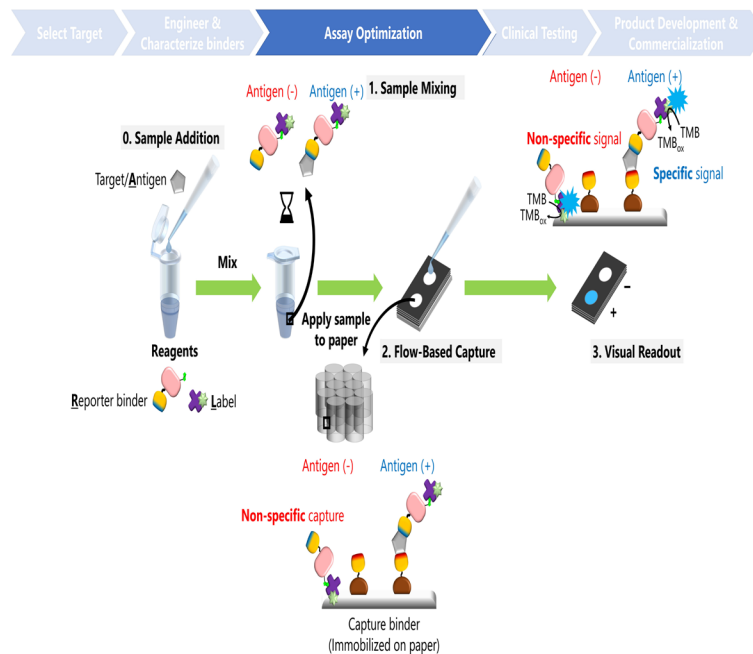
Accelerating the Optimization of Vertical Flow Assay Performance Guided by a Rational Systematic Model-based Approach

D. M. Y. Tay, S. Kim, Y. Hao, E. H. Yee, H. Jia, J. Voldman, H. D. Sikes

Sponsorship: HKUST-MIT Research Alliance Consortium, Singapore's National Research Foundation, MIT Summer Research Program (MSRP)

Rapid diagnostic tests (RDTs) have shown to be instrumental in healthcare and disease control. However, the laborious and empirical, yet necessary, development and optimization process for the attainment of clinically relevant sensitivity remains inefficient. While various studies have sought to model paper-based RDTs, they do not encompass all possible operation regimes. It is also unclear how the model predictions may be utilized for optimizing assay performance. Here, we propose a streamlined and simplified model-based framework for the acceleration of assay optimization, which relies on minimal experimental data. These models are

based on physically rational formulations accounting for relevant physical phenomena such as mixing and diffusion. We show that our models can recapitulate experimental data and estimate of several pertinent assay performance metrics such as limit-of-detection, sensitivity, signal-to-noise ratio and difference. We believe that our proposed workflow would be a valuable addition to the toolset of any assay developer, regardless of the amount of resources they have in their arsenal, and aid assay optimization at any stage in their assay development process.



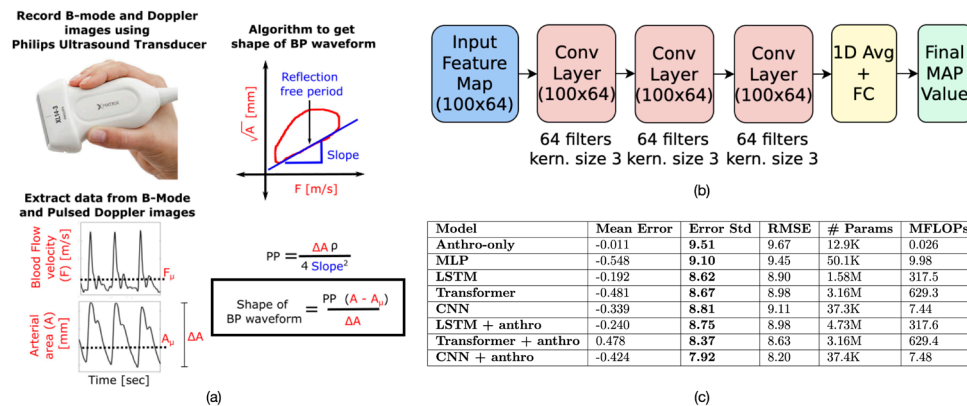
▲ Figure 1: Schematic of proposed assay optimization workflow

Cyb Machine Learning for Arterial Blood Pressure Prediction

H. Wang*, J. Zheng*, A. Chandrasekhar, J. Seo, A. Aguirre, S. Han, C. G. Sodini, H.-S. Lee
 Sponsorship: MIT J-Clinic, Philips, Analog Devices, MIT-IBM Watson AI Lab, NSF CAREER Award

High blood pressure is a major risk factor for cardiovascular disease. As such, accurate blood pressure (BP) measurement is critical. Clinicians measure BP with an invasive arterial catheter or via a non-invasive arm or finger cuff. However, an arterial catheter can be painful for the patient and not ideal outside an intensive care unit (ICU). Cuff-based devices are non-invasive, but they cannot provide continuous measurement, and they measure from peripheral blood vessels whose BP waveforms differ significantly from those closer to the heart. Hence, there is an urgent need to develop a measurement protocol for converting easily measured non-invasive data into accurate BP values. In this work, we propose a non-invasive approach to predict BP from arterial area and blood flow velocity signals measured from a Philips ultrasound transducer (XL-143) on large arteries close to heart. We developed the protocol and collected data from 72 subjects. The shape of BP (relative BP) can be theoretically calculated from these

waveforms, but there is no established theory to obtain absolute BP values. Therefore, we further employ data-driven machine learning models to predict the mean arterial blood pressure (MAP), from which the absolute BP can be deduced. We propose several different machine learning algorithms to optimize the prediction accuracy. We find that long short-term memory (LSTM), transformer, and one-dimensional convolutional neural network (1D-CNN) algorithms using the BP shape and blood flow velocity waveforms as inputs can achieve 8.6, 8.7, and 8.8-mm Hg average standard deviation of the prediction error, respectively, without anthropometric data (age, sex, heart rate, height, weight). Furthermore, the 1D-CNN model can achieve 7.9-mm Hg when anthropometric data are added as inputs, improving upon an anthropometric-only model of 9.5-mm Hg. This machine-learning algorithm can be a software modality that converts ultrasound data to MAP values to help physicians make clinical decisions.



▲ Figure 1: (a) The whole pipeline of using machine learning-based algorithms to get BP waveforms from ultrasound data (b) CNN model architecture (c) Performance summary.

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Progress and Challenges with Implantable Microphones for Cochlear Implants

E. F. Wawrzynek, J. Z. Zhang, A. Yeiser, C. I. McHugh, L. Graf, M. E. Ravicz, E. S. Olson, I. Kymissis, H. H. Nakajima, J. H. Lang
Sponsorship: National Institute on Deafness and Other Communication Disorders/NIH R01DC016874, NSF Graduate Research Fellowship Program Grant No. 1745302, the Edwin S. Webster Graduate Fellowship

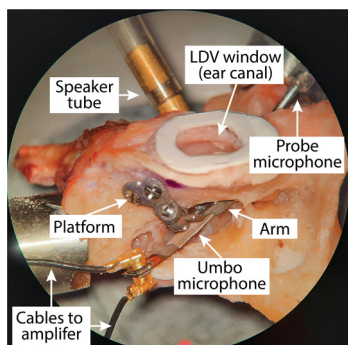
We have developed two microphone designs for a fully implantable cochlear implant. The Umbo Microphone (UM) (Figure 1) senses the motion of the umbo, while the Cochlear Microphone (CM) detects sound via intracochlear pressure. Implantable microphones utilize the natural filtering of the ear and enable the use of hearing assistive devices in all environments.

The transduction mechanism of our implantable microphones is based on the piezoelectric properties of polyvinylidene fluoride (PVDF), a common plastic that can be manufactured as a film. PVDF is biocompatible and used in medical devices. The UM is two layers of PVDF separated by a backing and detects sound signals via bending. This output is the amplified difference between the two signals from the PVDF layers, thus providing good common mode rejection. The signal-to-noise characteristics of the cantilever microphone are comparable to those of hearing aid external microphones (Figure 2-3). The CM works through deformation of the PVDF material due to fluid pressure in the scala tympani. A strip of

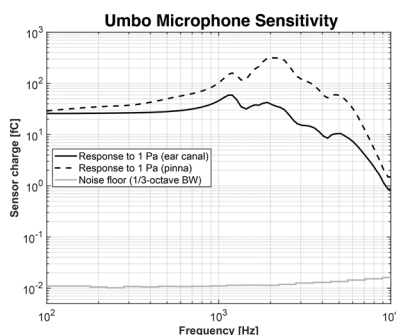
PVDF is inserted into the scala tympani alongside an electrode array. This design is attractive because it can be directly integrated with cochlear implant electrode arrays.

Our recent research focuses on making our current UM biocompatible without sacrificing performance. We have replaced the aluminum conductive layers of our earlier prototype with biocompatible titanium. Furthermore, we have developed a titanium mounting structure that holds the microphone against the umbo and can be implanted during tympanotomy surgery. For the CM, we have investigated novel designs that use different geometry and piezoelectric material to improve sensitivity. We are developing designs that can be integrated with existing electrode arrays of cochlear implants.

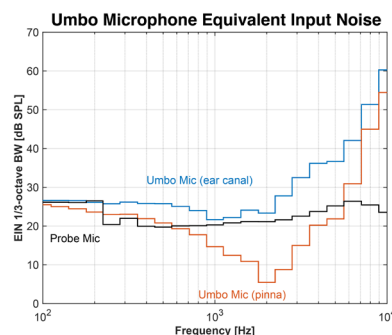
By focusing on material choice, integration, and structural methods for implanting our sensors, we are taking important steps towards an implantable microphone for fully implantable assistive hearing devices.



▲ Figure 1: Experimental setup for testing UM in human cadaver. Custom “mounting structure” holds UM inside middle ear cavity. Tip of UM contacts umbo and sound pressure is introduced at eardrum. Commercial probe microphone measures sound pressure for referential data.



▲ Figure 2: Sensitivity of UM in human cadavers. Charge output is referenced to 1 Pa sound pressure and shows that UM has relatively flat frequency response up to 1 kHz. Dotted line simulates pressure gain provided by external ear structure. Commercial probe microphone measures sound pressure for referential data.



▲ Figure 3: Equivalent Input Noise (EIN) of UM compared to EIN of commercial Knowles microphone. Orange line simulates pressure gain provided by external ear structure. Including pressure gain, EIN of our UM is comparable to that of commercial probe microphone.

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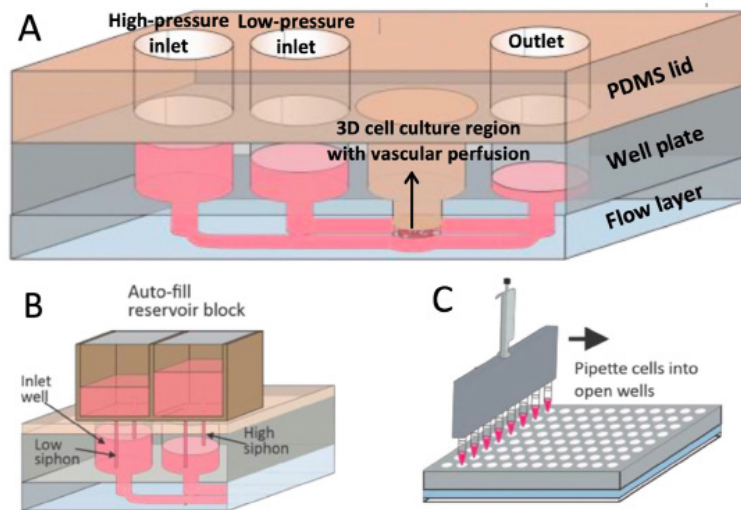
A High-throughput Open-well Microfluidic Organ-on-chip System for Blood-brain Barrier

F. Xue, U. Lee, W. Liao, J. Voldman
Sponsorship: NIH

Blood-brain barrier (BBB) on-chip constructed by microfluidic technology has assisted researchers in understanding BBB physiology and developing therapies for neurological diseases. However, the existing systems typically account for the biological relevance of BBBs at the expense of robustness, throughput, or ease of operation.

In this work, a BBB on-chip is developed incorporating all four factors above. The system aims to maintain biological sophistication by modeling the

architecture of in-vivo BBB and enabling vascular perfusion. The open-well design eliminates bubble-prone tubing operations and improves robustness, and coupling with a standard 96-well plate enables high-throughput operation. A siphon-based design maintains fluid levels at the inlets to ensure gravity-driven flow at a constant perfusion rate. The system can be used to investigate BBB functioning robustly and productively, enabling faster development of therapies for neurological diseases such as Alzheimer's.



▲ Figure 1: Open-Well Microfluidic Organ-on-Chip System. A) Perfusion culture region. B) Siphon-based autofill reservoir maintains a constant fluid level at the inlets. C) Open-well design allow easy access to fluid and culture region.

Circuits and Systems

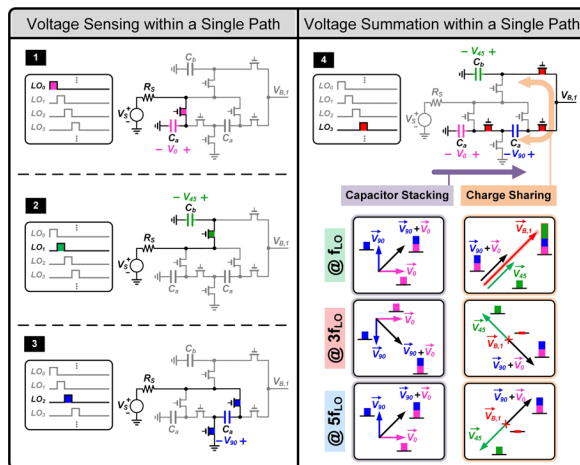
Harmonic-resilient Fully Passive Mixer-first Receiver for 5G NR Applications.....	13
Sniff-SAR: A 9.8fJ/c.-s 12b Secure ADC with Detection-driven Protection Against Power and EM Side-channel Attack	14
A 260GHz Transceiver with High-efficiency Antenna-in-package on 22nm FinFET Process.....	15
Retro-backscatter THz ID: With Energy Harvester and BPSK Backscatter.....	16
A Physically Unclonable Anti-tampering THz-ID Tag	17
Memory-efficient Gaussian Fitting for Depth Images in Real Time	18
A Continuous-time Pipelined ADC with Time-interleaved Sub-ADC-DAC Path in 16-nm FinFET.....	19
THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface	20

Harmonic-resilient Fully Passive Mixer-first Receiver for 5G NR Applications

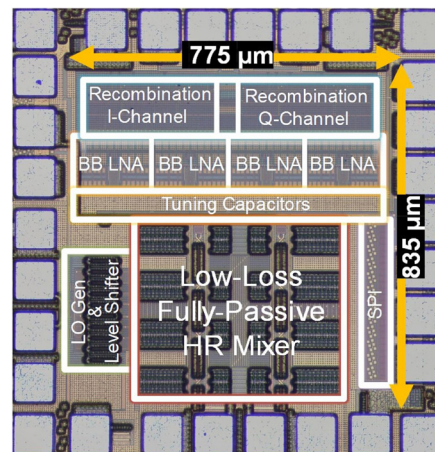
S. Araei, S. Mohin, N. Reiskarimian

Software-defined radios (SDRs) are versatile radio receivers that offer the promise of an all-in-one communication radio for multiple standards such as Bluetooth, Wi-Fi, and 5G new radio. To tackle the issue of interference, SDRs require a band-select filter with a widely tunable center frequency and bandwidth. However, integrating such a filter on-chip is challenging. In recent years, the mixer-first architecture has emerged as a promising candidate for SDRs as the passive mixer's reciprocity nature provides such a filter at the antenna interface by upconverting the base-band impedance to the radio-frequency (RF) domain. This inductor-less sharp-filtering scheme enhances the receiver's tolerance to near out-of-band blockers in a small form factor. Additionally, the mixer-first approach allows for precise and independent control over the center frequency and bandwidth of the filter. However, harmonic mixing can cause signals located at or around the harmonics of the local oscillator (LO) to downconvert to the baseband and readily saturate the subsequent baseband amplifiers. Thus, it is essential to suppress the LO signal's harmonic content.

In this work, we propose a low-loss all-passive harmonic-resilient and blocker-tolerant mixer-first receiver. This design exploits a co-design of charge-sharing and capacitor stacking to form a harmonic rejection filter right inside the mixer, thus eliminating the harmonic blockers before hitting the active stages. The proposed harmonic filtering technique requires no additional circuitry beyond extra switches and benefits from technology scaling. The fabricated 45-nm silicon-on-insulator (SOI) prototype RX, with a silicon area of 0.65 mm², operates across a wide frequency range, from 250MHz to 2.5GHz, and tolerates >10dBm 3rd harmonic blocker power, which is 40× larger than a state-of-the-art broadband harmonic rejection receiver. The proposed architecture offers high linearity against close-in and far-out blockers while also maintaining the widely tunable nature of mixer-first receivers, bringing us one step closer to realizing the vision of all-in-one communication radios.



▲ Figure 1: Time-domain operation of the proposed low-loss fully passive harmonic rejection mixer.



▲ Figure 2: Die micrograph of the proposed harmonic rejection receiver.

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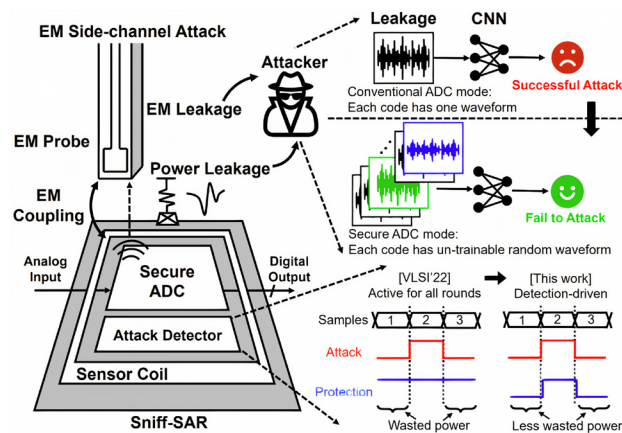
Sniff-SAR: A 9.8fJ/c.-s 12b Secure ADC with Detection-driven Protection Against Power and EM Side-channel Attack

R.-C. Chen, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Center for Integrated Circuits and Systems, DARPA

As shown in Figure 1, sensitive and confidential information can be stolen from an analog-to-digital converter (ADC) by electro-magnetic side-channel attacks (EMSA) or power side-channel attacks (PSA). An EM probe can measure the EM side-channel information of the ADC. An attacker can obtain the power side-channel information by measuring the power traces of the ADC. There are two challenges for secure ADCs. First, to address the security concerns, secure ADCs have non-negligible overheads in energy and area, which is not ideal for resource constrained applications such as the Internet of Things. The protection scheme is typically always-on even if the side-channel attacks are not performed. Second, neural network-based side-channel attacks are becoming more powerful, making existing protection less robust. To address these two challenges, this work proposes the first detection-driven ADC secure against both power and EM side-channel attacks. The ADC normally operates in an energy-efficient switching mode. When an EMSA or PSA is detected, secure switching is enabled that renders the ADC very

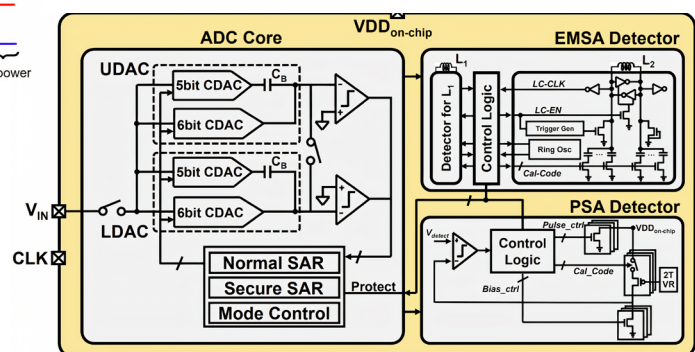
protected from neural network-based attacks. Figure 2 shows the system architecture of the Sniff-SAR with detection-driven protection. The EMSA and PSA detectors capture the attempt of side-channel attacks. The ADC core normally operates in the unprotected SAR mode, which is faster and more energy-efficient. EMSA and PSA detectors check for the side-channel attacks periodically; once they notice that the ADC is under attack, the ADC activates the secure SAR mode against both EMSA and PSA.

Fabricated in the 65-nm LP process, the Sniff-SAR occupies 0.075 mm² (Figure 2). Compared with always-on protection, we introduced detection-driven protection. Moreover, a new switching scheme is implemented, which is practically untrainable using neural networks. This work also demonstrates the highest sampling rate and best figure of merit (FoM) in secure ADCs by a duty cycling for both detectors. The secure SAR achieves an FoM of 9.8fJ/c.-s, which is comparable to the state-of-the-art energy-efficient unprotected ADC using similar technology.



◀ Figure 1: Side-channel security challenges of ADCs and detection-driven protection based on randomization

▼ Figure 2: System architecture of the side-channel-secure ADC with detection-driven protection



FURTHER READING

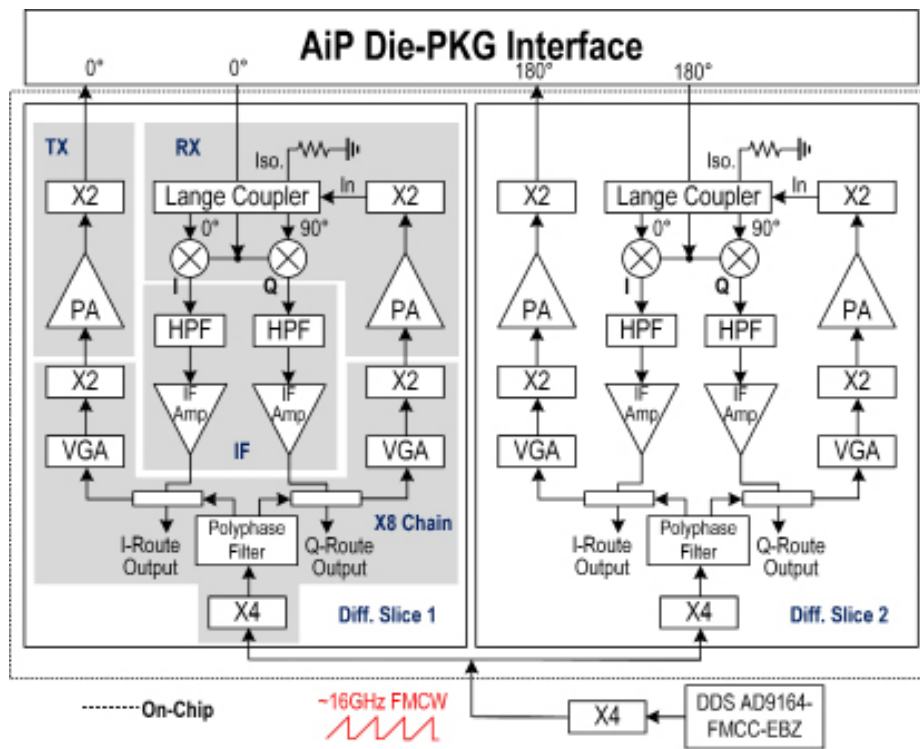
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A 260GHz Transceiver with High-efficiency Antenna-in-package on 22nm FinFET Process

X. Chen, G. Dogiamis, R. Han
Sponsorship: Intel Corporation

CMOS-based on-chip antenna for sub-THz radiation suffers from its inherently low radiation efficiency, due to extremely small thickness of dielectric stack, and lossy silicon substrate. Transistor cut-off frequency (f_{max}) in nowadays mainstream CMOS processes further introduces significant hurdles for generating high radiated power at sub-THz regime, especially when the operating frequency exceeds 200GHz. This work shows a 260GHz transceiver design with high-efficiency an-

tenna-in-package (AiP) design, based on Intel 22nm FinFET process. Simulation shows the highest radiation efficiency among all other reported CMOS works under the same frequency. An on-chip 260GHz transceiver is designed to pair with the AiP. The whole system shows a simulated wide bandwidth and decent radiated power, which translates to high ranging resolution with long detection range for FMCW radar detection.



▲ Figure 1: 260GHz Transceiver System Diagram.

Retro-backscatter THz ID: With Energy Harvester and BPSK Backscatter

M. Jia, D. Sheen, R. Han, A. P. Chandrakasan
Sponsorship: Intel University Shuttle, NSF

Radio-frequency identification (RFID) tags have become a ubiquitous technology for tracking, authentication, localization, supply-chain management, and more. Nevertheless, commercial RFID chips currently rely on the external antenna or inductor packaging to enable efficient coupling of RF waves. Unfortunately, this design significantly increases the tag's overall size, rendering it unsuitable for attachment to small objects like medical pills, tooth implants, and semiconductor chips. An additional cost is associated with the chip packaging, which takes up to two-thirds of the total tag cost. Therefore, there is a pressing need for fully passive, particle-sized cryptographic chips that require no external packaging to allow secure and ubiquitous asset tagging. Besides, we want users to be able to read our tags at a long distance and from a flexible angle. At the same time, a single source input will significantly reduce the cost of the tag reader itself.

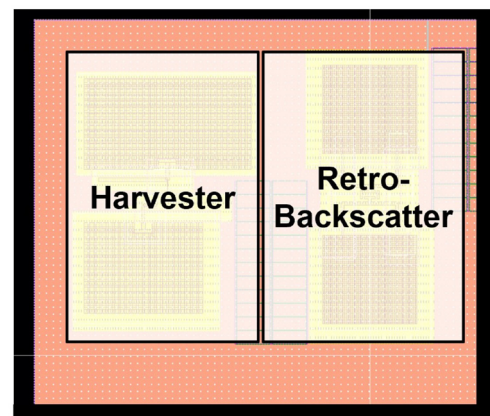
To address these challenges, we propose an entirely new version of the terahertz (THz) ID called Retro-backscatter THz ID. Firstly, we proposed a

fully passive retro-backscatter system with binary phase-shift keying (BPSK) modulation to enhance the operating distance of the tag. Currently, RFID systems suffer from a major drawback whereby reflected power is radiated omnidirectionally, dissipating valuable re-radiated power away from the desired receiving reader, which drastically limits the tag's operating range. Additionally, our proposed retro-backscatter design effectively mitigates the problem of phase sensitivity of the backscatter array and offers users the ability to read the tag from a more flexible angle.

Furthermore, we introduce a THz harvester and direct current-direct current converter that enables a single THz signal input, thus allowing for both energy harvesting and tag functionality, to also reduce the cost of the reader. We also integrate an ultra-low-power digital dedicated processor into the THz-ID chip, which provides high-security compact asymmetric encryption.



▲ Figure 1: Multi-functional electromagnetic design.



▲ Figure 2: Partial layout of the proposed Retro-backscatter THz ID.

A Physically Unclonable Anti-tampering THz-ID Tag

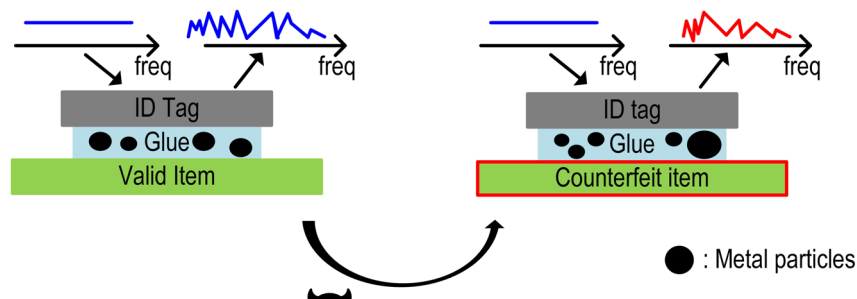
E. Lee, M. Jia, A. P. Chandrakasan, R. Han

Sponsorship: Korea Foundation for Advanced Studies, NSF (SpecEES ECCS-1824360)

Wireless radio-frequency identification (RFID) tags are becoming more popular, particularly in supply chain management and item authentication. For these tags to be widely used, they must be small, cost-effective, and easily adaptable to any object without requiring complicated packaging. Recently, the first demonstration of a 1.6 mm² terahertz (THz) wireless tag that can authenticate items without packaging was presented. This tag is enabled through the on-chip antennas and low-power bi-directional communication via zero-power THz detecting and THz backscattering. Despite its ability to authenticate items, the wireless tag is still susceptible to tampering since an attacker could remove the ID tag from the authentic item and attach it to a counterfeit one. This could make it difficult for the reader to distinguish between genuine and fake items.

The study aims to address this security vulnerability of wireless tags by developing a small, packaging-free tag that has anti-tampering features. Our approach

involves utilizing the material properties of the adhesive interface between the THz-ID tag and item to generate and extract a distinctive THz electromagnetic signature. Once affixed to an item, the anti-tampering ID tag generates a distinct electromagnetic signature. This signature is obtained by interrogating the tag using a reader, and THz response is stored within the data set. If a hacker attempts to remove and reattach the tag to a different surface, the electromagnetic signature will be disrupted. The reader can detect this tampering (Figure 1). Replicating the unique THz signature generated by the interaction between the ID tag, surface, and adhesive materials is a difficult and expensive task for hackers due to the random distribution of the signature. This makes it impractical for them to clone the tag. While this project is still in-progress, this system will advance the utilization of the THz spectrum for secure authentication of self-powered Internet of Things and wireless tags.



▲ Figure 1: The scenario of tampering attacks on THz anti-tampering ID tags.

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Memory-efficient Gaussian Fitting for Depth Images in Real Time

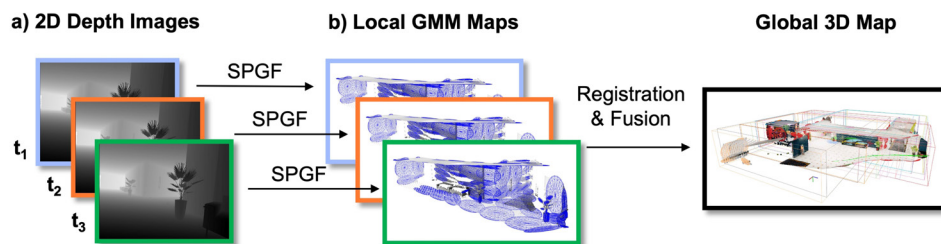
P. Z. X. Li, A. Wojtyna, S. Karaman, V. Sze
Sponsorship: NSF RTML 1937501, NSF CPS 1837212

We explore methods to enable motor systems to utilize sensor data to assess installation and detect or predict anomalous events before possible breakdown. Here, we use an autoencoder neural network model for unsupervised anomaly detection on an air-handling system driven by a switched-reluctance motor (Figure 1). The motor system consists of a belt-driven blower-motor unit with a 6/10 stator/rotor pole configuration.

Our model (Figure 2) takes the Fourier transform of recorded sensor time signals and trains one autoencoder per feature. The sum of the reconstruction errors is used as an anomaly score for prediction. The autoencoder has been effective on time series datasets in multiple fields. We generate datasets with differences in various parameters (e.g., belt tightness, motor speed, blower output valve condition) and label the data according to the anomalous scenarios. For instance, if a dataset is used for anomaly detection of belt tightness, we label the time series generated with normal belt tightness “normal” and an over tight/loose

belt “anomalous.” We choose three kinds of sensor data (line current, motor current, vibration) as the time series for anomaly detection. We assume that the system operates normally during training and that sensor data used for training purposes contain few, if any, anomalies.

The base frequencies of motor current and vibration are identical and consistent with the 6:10 pole ratio. Characteristic curves are found in randomly ordered runs for transient sensor data during activation (Figure 3). Results of stable sensor data show 100% area under curve (AUC) / 98% accuracy for anomaly detection of belt tightness, and 95% AUC / 82% accuracy for speed; 52% AUC / 34% accuracy for valve condition indicates that this condition remains difficult to detect. Combining the labels for the three parameters achieves 94% AUC / 87% accuracy. Our model detects anomalies on motor systems for one or several aggregated failure modes.



▲ Figure 1: (a) A depth image from a depth camera, and (b) a GMM (blue) generated using the proposed SPGF algorithm with a root-mean-square error of 9 cm, a memory overhead of 43 KB, a throughput of 32 fps, and an energy consumption of 0.11 J per frame using the low-power ARM Cortex-A57 CPU.

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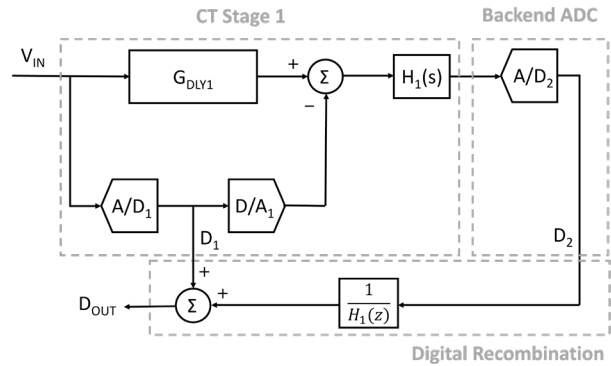
A Continuous-time Pipelined ADC with Time-interleaved Sub-ADC-DAC Path in 16-nm FinFET

R. Mittal, H. Shibata, S. Patil, E. Krommenhoek, P. Shrestha, G. Manganaro, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Analog Devices Inc.

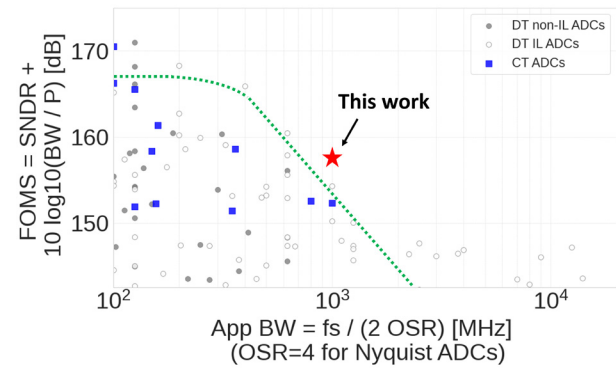
With the advent of the fifth-generation (5G) standard for cellular networks, direct radio frequency receivers are popular in applications such as cellular base stations. Such systems require analog-to-digital converters (ADC) with a high dynamic range over a large digitization bandwidth (> 500 MHz). For high-speed high-resolution ADCs with an upfront sampler, the clock jitter poses a fundamental bottleneck for the maximum achievable signal-to-noise ratio (SNR). In applications requiring 10-12 bit resolution for 1 GHz digitization bandwidth, the clock jitter values must be no more than a few tens of femtoseconds. This poses significant design challenges for the clock generator.

The continuous-time (CT) pipeline ADC is an emerging architecture that combines the benefits of a discrete-time pipeline ADC and a continuous-time $\Delta\Sigma$ ADC architecture. In this project, we explore the clock jitter sensitivity of the CT pipeline ADC. We derive the SNR limitations in a CT pipeline ADC and propose a new CT pipeline ADC design with improved tolerance to clock jitter. We also present a design methodology for the delay line and propose a novel inductor-less delay line that provides a good amplitude and phase matching between the stage 1 signal path and the sub-ADC-DAC path from DC to 1.6 GHz to minimize the signal leakage in the first stage residue.

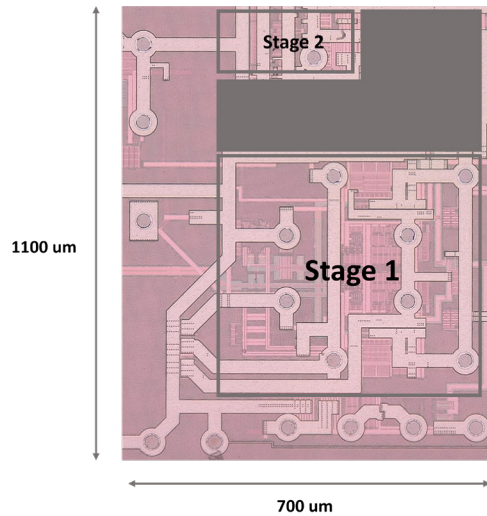
A prototype ADC was fabricated in 16-nm fin field-effect transistor process. The ADC achieves 61.7/60.8dB (low/high frequency) SNR over 1-GHz bandwidth. The active area is 0.77mm² the ADC consumes 240mW. The Schreier figure-of-merit (FOM) is 157.9dB, which is among the best in comparison to other state-of-the-art continuous-time ADCs with digitization bandwidth greater than 500MHz.



▲ Figure 1: Block diagram of a 2-stage CT pipeline ADC. Stage 1 is a continuous-time stage, and stage 2 is a discrete-time ADC.



▲ Figure 2: Die photo of the prototype ADC. The ADC occupies 0.77mm² and consumes 240mW power.



▲ Figure 3: FOMS vs. application bandwidth plot.

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THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface

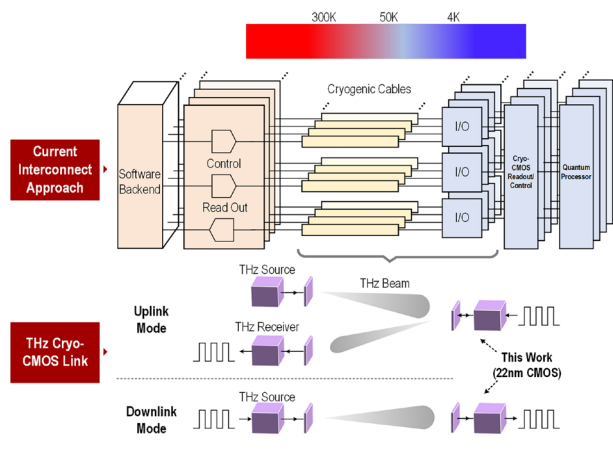
J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. W. Khan, X. Yi, D. R. Englund, R. Han
Sponsorship: Intel University Shuttle

Modern low-temperature large-scale systems, such as high-sensitivity terahertz (THz) imaging arrays and quantum computers, require large-scale data interfaces between the cryogenic system core and room-temperature (RT) electronics. An error-protected quantum computer needs thousands or even millions of qubits operating at cryogenic temperature. However, its scalability is still largely limited by the cables connecting the quantum cores and peripheral control/processing units due to the heat load of cables. For example, a stainless-steel UT-085-SS-SS cable could pose close to one mW of heat load to the 4K stage, and tens of mW to the 50K stage in a dilution refrigerator. A 50-qubit quantum computer already has hundreds of cryogenic radio frequency (RF) cables, while the total power budget is limited to ~ 1 W or even less.

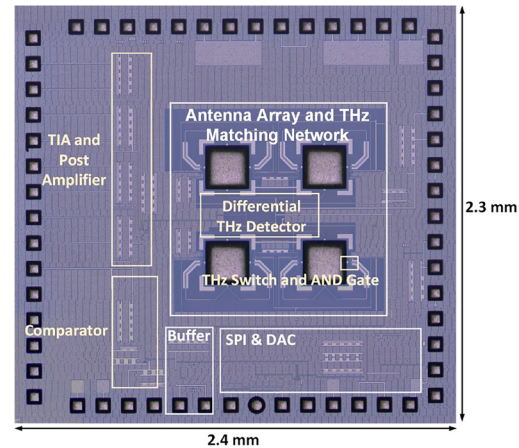
In this project, we present a complementary metal-oxide semiconductor (CMOS) THz transceiver chip operating at 4K as a fully integrable alternative

to the cryogenic RF cables. We determined an optimal carrier frequency of 260GHz based on the trade-off between the antenna dimension and the efficiency of the transistors. This frequency is sufficiently high to minimize the link footprint and to avoid potential disturbance of qubits, such as the superconducting or nitrogen-vacancy qubits, that typically operate at gigahertz; it also leads to much lower quantum noise ($\sim \hbar\omega$) compared to that in photonic links.

The transceiver avoids the power-hungry THz generation by using a passive backscatter communication scheme. A 4Gbps uplink is demonstrated with only 176fJ/b added heat load. In the downlink, we adopted a zero-power-consumption THz square-law detector. The receiver heat load is further reduced to 34fJ/b at 4.4Gbps. This fully contactless 4K-RT interface can be used to deliver digitized control/readout data, and even some analog/RF signals such as low phase noise clocks.



▲ Figure 1: Overview of the proposed contactless link replacing cryogenic cables in a cooled system.



▲ Figure 2: Die micrograph.

FURTHER READING

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Devices (Electronic, Magnetic, Superconducting)

Fully 3D-printed, Soft-magnetic Cored Solenoids	22
Identification of Multiple Failure Mechanisms for Reliability Analysis	23
Ultra-high Magnetic Field Resilience of Tunneling Magnetoresistance in an Antiferromagnetic Tunnel Junction	24
Monolithic, Additively Manufactured Quadrupole Mass Filters Nearing Unity Mass Resolution	25
Electrical Manipulation of Dissipation in Microwave Photon-magnon Hybrid System through the Spin Hall Effect	26
Optically Controlled Vertical GaN Fin Transistor.....	27
Densely Packed, Additively Manufactured Carbon Nanotube Field Emission Electron Sources.....	28
Capacitance-Voltage Characteristics of Ferroelectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Structures in the GHz Regime	29
High-p Performance P-type 2D Transistors with Low-r Resistance Contacts.....	30
In-situ Monitoring of GaN Power Transistor Parameters Under Continuous Hard-switching Operation.....	31
Use of Ion Implantation to Engineer the Electric Field Profiles in GaN Superjunctions.....	32
High-power AlGaN FinFET for mm-Wave Applications	33
Highly-scaled Vertical Nanowire GaSb/InAs Tunnel FETs.....	34
GaN Field-emission-based Vacuum Transistors	35
Cold-source FET with Graphene/MoS ₂ Heterojunction	36
Towards Design Technology Co-optimization (DTCO) in High-temperature GaN-on-Si Electronics	37
GaN Complementary Transistor Technology	38
GaN Memory Operational at 500 °C.....	39
GaN Ring Oscillators Operational at 500 °C	40
Enhancement-mode GaN Transistor Technology for Harsh Environment Applications	41
First Demonstration of GaN RF HEMTs on Engineered Substrate	42
Epitaxial Perovskite Ferroelectric-based Capacitive Memory.....	43

Fully 3D-printed, Soft-magnetic Cored Solenoids

J. Cañada, L. F. Velásquez-García
Sponsorship: Empiriko Corporation, “la Caixa” Foundation

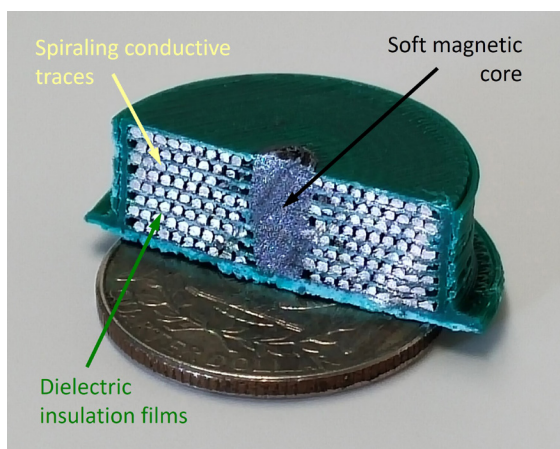
Additive manufacturing can readily produce freeform-compatible, mechanically functional parts. However, the three-dimensional (3D) printing of electronic components that could enable the monolithic manufacture of integrated electromechanical devices is lagging. Material extrusion, also known as fused filament fabrication (FFF), is one of the most accessible additive manufacturing techniques. FFF allows the monolithic fabrication of parts comprising multiple materials, e.g., dielectric and conductive.

Reports of 3D-printed resistors, capacitors, and inductors demonstrate the feasibility of 3D-printing electronic components via dielectric-conductive material extrusion. However, the 3D-printed inductors reported in the literature are limited to two-dimensional designs. This work aims at attaining improved versatility and performance of 3D-printed solenoids through their expansion to truly 3D designs, and through the addition of soft magnetic cores.

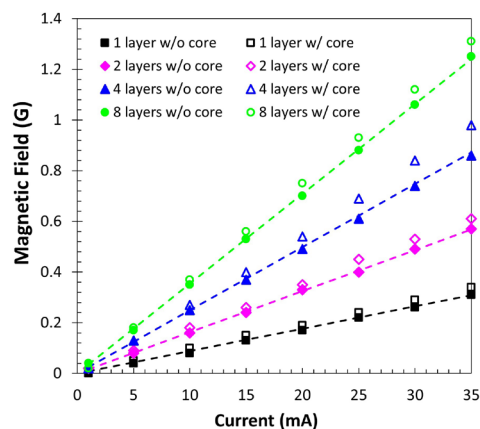
The 3D-printed solenoids have been fabricated

through material extrusion using three polylactic acid (PLA)-based materials: dielectric PLA was used to produce insulation films and structural support features; copper nanoparticle-doped PLA was used to create a spiraling conductive trace; iron-doped PLA was used to fabricate an embedded soft magnetic core at the center of the structure. By stacking conductive spirals and insulation films, solenoids with as many as 10 layers have been created (Figure 1).

Magnetic field measurements reveal that the 3D-printed solenoids can generate Gauss-order magnetic fields while drawing tens-of-mA currents (Figure 2). Moreover, the introduction of the soft magnetic core results in a 10% increase in the measured magnetic flux with respect to the flux generated by 3D-printed solenoids with nonmagnetic cores. Current work focuses on improving material properties and manufacturing capabilities (e.g., minimum feature size) to yield more capable devices.



▲ Figure 1: 3D-printed solenoid cut in half showing its different structures, on top of a U.S. quarter.



▲ Figure 2: Measured magnetic field vs. current from solenoids with soft magnetic core (empty markers), with nonmagnetic core (filled markers), and computed estimates with non-magnetic core (dashed lines).

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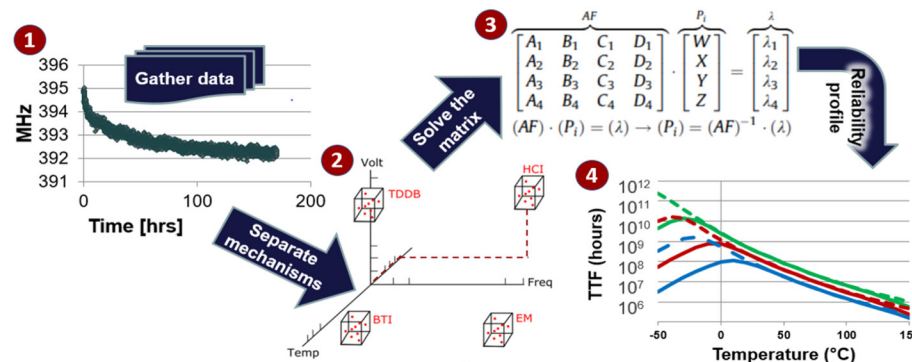
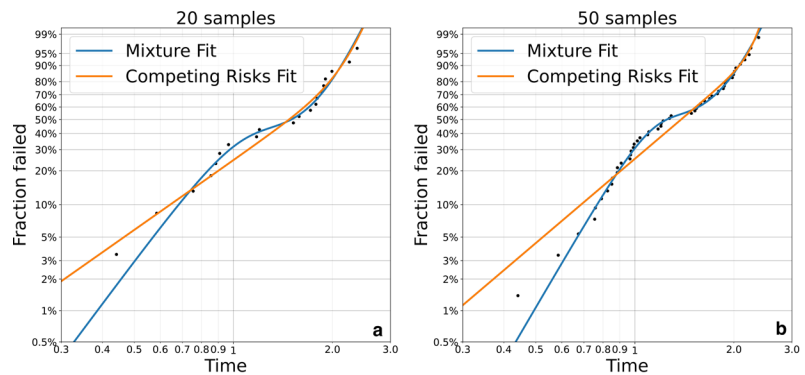
Identification of Multiple Failure Mechanisms for Reliability Analysis

U. Chakraborty, E. Bender, C. V. Thompson, D. S. Boning
Sponsorship: SRC

To extend Moore’s Law, heterogeneous integration promises enhanced functionality through two-and-a-half dimensional (2.5D) and three-dimensional (3D) system architectures, offering high-bandwidth and power-efficient solutions across a wide range of electronic and photonic applications. The identification of distinct failure mechanisms and optimization for reliability of heterogeneously integrated systems hold paramount importance since the common assumption of only a single underlying failure mechanism usually leads to overly optimistic or pessimistic reliability estimates. We explore both mixture models (where each device is subject to one of several independent failure mechanisms) and competing risks models (where each device is subject to multiple failure mechanisms simultaneously) using synthetic data sets to represent failure times due to multiple mechanisms (Figure 1). We apply techniques based on statistical learning and optimization algorithms to estimate the distribution parameters of the underlying failure mechanisms and evaluate the accuracy of our estimates across a range of data sets.

We also implement the multiple temperature operational life (MTOL) testing method, which is tailor-made for generating reliability profiles of devices assuming that multiple failure mechanisms are present. With MTOL, device data are gathered in multiple stress modes to isolate failure mechanisms and extract the mechanisms’ failure rates. A matrix is formulated from the failure rates, creating a time-to-failure assessment of the device across a wide temperature range (Figure 2). We use the MTOL method to characterize ring oscillator failure mechanisms including hot carrier injection, bias temperature instability and electromigration in 45-nm, 28-nm and 16-nm silicon technologies. Isolation of failure mechanisms in hybrid bonds is challenging due to the similarity of stress conditions for the different mechanisms. Currently the methodology is being developed to extract relative weights of common hybrid bond failure mechanisms such as fatigue, stress-voiding, and electromigration in heterogeneously integrated systems. A hybrid bond testing system on field-programmable gate arrays is also in development.

► Figure 1: Mixture distribution datasets of sizes (a) 20 and (b) 50, fitted with mixture and competing risks models. Competing risks model provides inaccurately pessimistic reliability projections for early failure times in this case.



◄ Figure 2: MTOL testing method. (1) Data acquisition from multiple stress modes. (2) Isolation of individual mechanisms. (3) Solution of failure rates using matrix with mechanisms’ pre-factors. (4) Failure profile generation with relative weights of mechanisms.

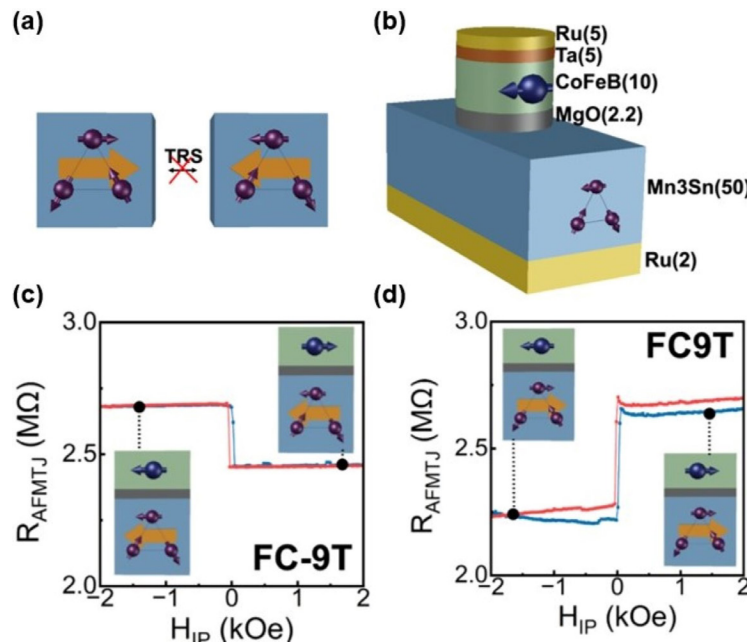
Ultra-high Magnetic Field Resilience of Tunneling Magnetoresistance in an Antiferromagnetic Tunnel Junction

C.-T. Chou, L. Liu
Sponsorship: SRC

Antiferromagnets (AFMs) have been actively pursued as active components in spintronic devices for their fast switching dynamics and absence of dipolar interactions. However, so far AFMs have not been widely used in memory devices due to lack of efficient means to read out the antiferromagnet ordering orientation. The readout is challenging because most AFMs possess translation-time reversal (T-TR) symmetry. The T-TR symmetry suggests that rotating each individual magnetic moment of AFM by 180° results in no macroscopically observable change and thus no usable readout signal. Recently it has been predicted and experimentally shown that Mn_3Sn , an AFM material with frustrated spin structure that breaks the T-TR symmetry (Figure 1a), can have finite tunneling magnetoresistance when made into an antiferromagnetic tunnel junction (AFMTJ). However, the physical mechanism of the tunneling magnetoresistance is not clear, and the

tunneling magnetoresistance ratio (TMR) still needs to be improved for practical applications.

In this work, by carrying out experiments with $\text{Mn}_3\text{Sn}/\text{MgO}/\text{CoFeB}$ AFMTJs (Figure 1b), we observed sizable TMR at low temperature which remains stable under magnetic fields as high as 4T. As shown in Figure 1c and d, the AFMTJ shows a $\sim 10\%$ TMR when the Mn_3Sn and CoFeB relative orientation changes between parallel and antiparallel. Further measurements at different working temperature show strong correlations between TMR and the cooling field-induced offset in magnetization loops, indicating decoupling of the magnetic ordering in the interfacial and bulk regions of Mn_3Sn . The role of field cooling or annealing in controlling the TMR and the strong immunity of the antiferromagnetic fixed layer to external fields point to useful schemes for developing practical antiferromagnetic spintronic devices.



▲ Figure 1 (a) Magnetic structure of antiferromagnetic Mn_3Sn . Purple arrows indicate individual Mn atomic magnetic moment; orange arrow indicates cluster octupole moment. (b) Schematic of AFMTJ structure, (c)-(d) TMR of AFMTJ measured after cooling to 10K under -9T (c) and 9T (d) magnetic field. Insets of (c) and (d) show orientation of CoFeB free layer dipolar moment and the Mn_3Sn fix layer octupole moment.

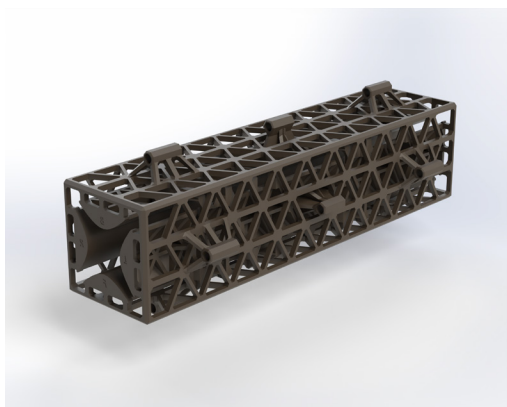
Monolithic, Additively Manufactured Quadrupole Mass Filters Nearing Unity Mass Resolution

C. C. Eckhoff, N. K. Lubinsky, R. E. Pedder, L. F. Velásquez-García
Sponsorship: Empiriko Corporation

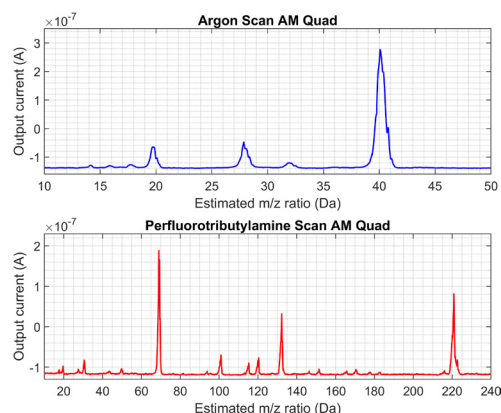
Quadrupole mass spectrometry is widely used in various fields, including healthcare, research, and defense. However, current efforts to reduce size and cost often come at the expense of performance. Across many industries, additive manufacturing (AM) is being explored as a potential solution for producing smaller and more affordable scientific instruments without compromising their performance. Thus, our work investigates whether AM can be used to create a miniature and inexpensive quadrupole mass filter that outperforms current alternatives.

Our quadrupole filter features a monolithic and skeletonized design, whereby the integration of each of the four electrode rods is done in one piece. This method enables accurate alignment of the rods

without the need for assembly, while also reducing production costs and increasing strength-to-weight ratio. We use digital light processing (DLP) to print parts using crystalline silica resin and then metallize them with an electroless nickel-boron coating. To isolate the four electrodes from one another, a lacquer-based maskant is applied, which is necessary with a monolithic design. The mass spectra obtained from this quadrupole demonstrate clearly resolved peaks with a full-width half-maximum (FWHM) of 1 Da at 69 m/z, the largest component of perfluorotributylamine (FC43). Our focus is on further enhancing this device to achieve the desired 0.7 Da FWHM peak threshold for unity mass resolution.



▲ Figure 1: Design of additively manufactured quadrupole mass filter, featuring a monolithic, skeletonized design.



▲ Figure 2: Scans of Ar and FC43 using the additively manufactured quadrupole filter.

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Electrical Manipulation of Dissipation in Microwave Photon-magnon Hybrid System through the Spin Hall Effect

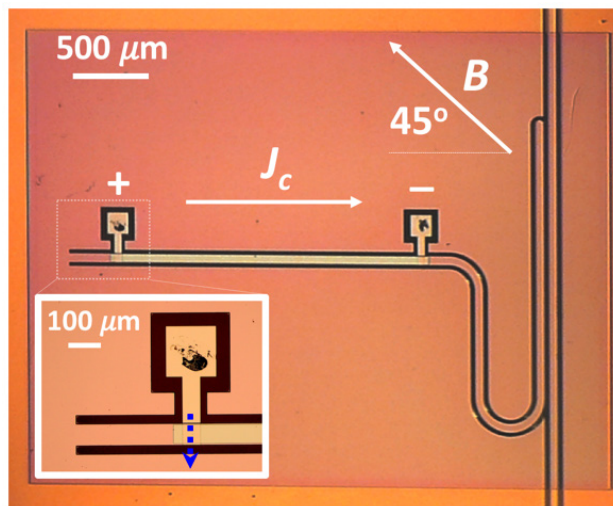
J. T. Hou, C. -T. Chou, J. Han, Y. Fan, L. Liu

Sponsorship: Air Force Office of Scientific Research (Grant No. FA9550-19-1-0048), NSF (Grant No. ECCS-1653553)

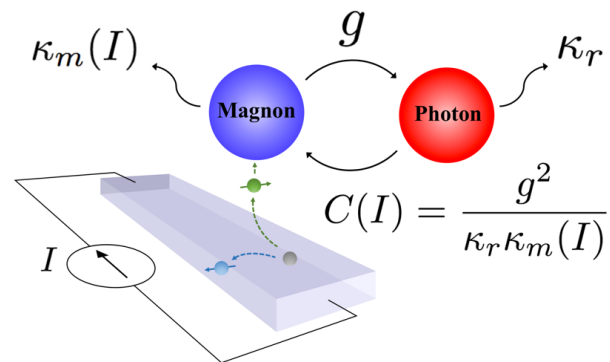
Hybrid dynamic systems combine advantages from different subsystems for realizing information processing tasks in both classical and quantum domains. However, the lack of controlling knobs in tuning system parameters becomes a severe challenge in developing scalable, versatile hybrid systems for useful applications. While various techniques have been developed for tuning the frequencies of hybrid systems, modulating the dissipation rates and coupling strengths represents more challenging tasks, with the former pre-determined by intrinsic material properties and the latter fixed by device geometries.

In this work, we report an on-chip microwave photon-magnon hybrid system (Figure 1) where the dissipation rates and the coupling cooperativity

can be electrically influenced by the spin Hall effect (SHE) (Figure 2). Through magnon-photon coupling, the linewidths of the resonator photon mode and the hybridized magnon polariton modes are effectively changed by the spin injection from an applied direct current into the magnetic wires, which exhibit different trends in samples with low and high coupling strengths. Moreover, the linewidth modification by the SHE shows strong dependence on the detuning of the two subsystems, in contrast to the classical behavior of a standalone magnonic device. Our results pave an avenue towards realizing tunable, on-chip, scalable magnon-based hybrid dynamic systems, where spintronic effects provide useful control mechanisms.



▲ Figure 1. Microscope photo of a quarter-wave planar resonator with a [Ta/Py/Pt]_n stripe on top.



▲ Figure 2. Schematic diagram showing a magnon-photon hybrid system where the magnon dissipation can be electrically adjusted by the SHE using a direct current, thereby further tuning the photon subsystem and the hybrid system cooperativity.

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Optically Controlled Vertical GaN Fin Transistor

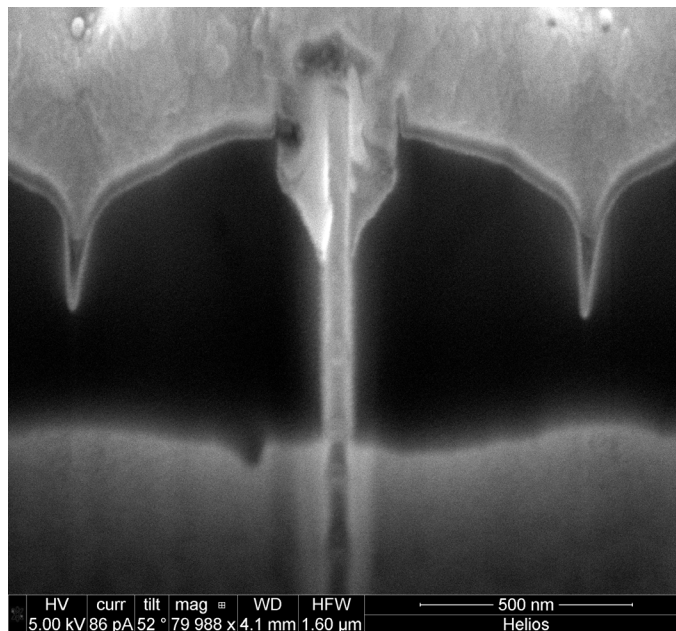
J.-H. Hsia, J. Perozek, R. Molnar, T. Palacios

Sponsorship: Office of Naval Research (Grant No. N00014-22-1-2468)

In recent years, the boost in consumer electronics, automotive, and data centers has significantly increased the electricity demand. The delivery and transformation of power through electric grids require many efficient power converters. Thanks to the advancements in wide band-gap (WBG) semiconductors like SiC and GaN, power devices are becoming more energy efficient and can withstand higher voltages. However, for medium-high voltage (1-50kV) applications, multiple power devices have to be stacked to achieve the required blocking voltage. The stacking of electrically triggered devices often demands a complex circuit design and poses reliability concerns due to significant electro-magnetic interference (EMI). The use of optically trig-

gered devices will simplify the circuitry design, reduce EMI and potentially increase the operating frequency.

Although optically triggered silicon devices have already been developed, there are no demonstrations on optically controlled GaN transistors, which have the potential to achieve higher power density. In this work, we develop, for the first time, optically controlled GaN transistors based on the vertical finFET structure. A large photo-responsivity is observed upon UV illumination, showing promising aspects of our proposed device structure in demonstrating a fully controllable, optically triggered GaN switch.



▲ Figure 1. Focused Ion Beam – Scanning Electron Microscopy (FIB-SEM) cross section image of the fabricated fin transistor.

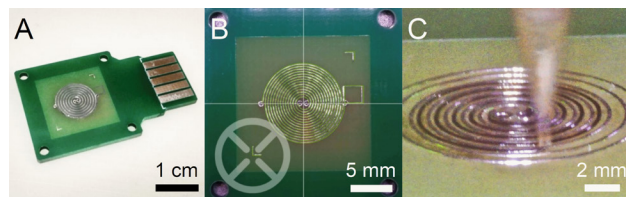
Densely Packed, Additively Manufactured Carbon Nanotube Field Emission Electron Sources

A. Kachkine, L. F. Velásquez-García

Sponsorship: NewSat (COMPETE2020, European Regional Development Fund, Federal Trade Commission, MIT Portugal Program)

Miniaturized spacecraft must neutralize ion thruster plumes to avoid charge-induced degradation. Field emission electron sources are preferred over state-of-the-art hollow cathodes due to their smaller size, lower power consumption, and lack of propellant requirements. We present additively manufactured, in-plane gated field emission electron sources with 35% lower startup voltage (~ 40 V) and 65% larger current density ($\sim 100 \mu\text{A}/\text{cm}^2$) than state-of-the-art, 3D-printed, in-plane gated field emission devices. Our sources hold further relevance to mass spectrometry of gases, x-ray imaging, and electron projection lithography.

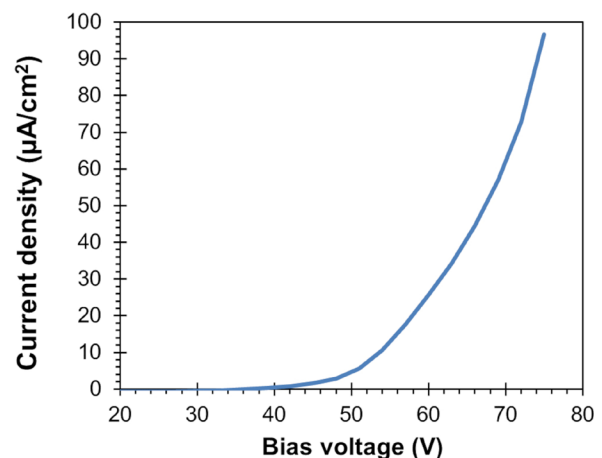
The reported sources (Figure 1) are made via direct ink writing (DIW) on a custom printed circuit board (PCB) and are composed of two concentric spiral traces: a trace made of a novel, high-concentration carbon nanotube (CNT) ink acting as the emitting electrode and a conventional PCB copper trace as the extractor gate. Printing is facilitated by a Voltera NOVA instrument with optical alignment and surface mapping, allowing increased trace packing density.



▲ Figure 1: Selected images of the manufacturing process. A) Spiraled, 3D-printed CNT field emission source on a bespoke PCB. B) Alignment procedure using hashes on PCB and Voltera NOVA's software. C) DIW of CNT ink. The nozzle moves at 1 cm/s, i.e., the device is printed in <30 seconds.

To avoid clogging 100 μm diameter printing nozzles, the CNT ink is prepared by ultrasonically dispersing CNTs in N,N-dimethylformamide, followed by filtration and addition of a stabilizer, ethyl cellulose. The resulting mixture is boiled, removing solvent and thus concentrating the ink while avoiding clumping of dispersed CNTs. Deposited CNT traces are activated via tape liftoff.

Data from devices tested in vacuum (Figure 2) follow the Fowler-Nordheim model, with the field enhancement factor estimated at $1.85 \times 10^6 \text{ cm}^{-1}$, corresponding to a tip diameter of 10.8 nm, which is similar to the diameters of the exposed CNT tips from metrology. Compared to cleanroom-fabricated counterparts, these devices can be made without etching or other processes with large amounts of hazardous waste. The short printing time, low material usage, and lack of cleanroom requirements posed by our devices greatly reduces the expenses required for rapid iteration of field emitter designs.



▲ Figure 2: I-V plot of 3D-printed field emission electron source, showing mean of 20 replicates with 5-V sample spacing. Startup voltage is ~ 40 V; peak current density is $\sim 100 \mu\text{A}/\text{cm}^2$.

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Capacitance-voltage Characteristics of Ferroelectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Structures in the GHz Regime

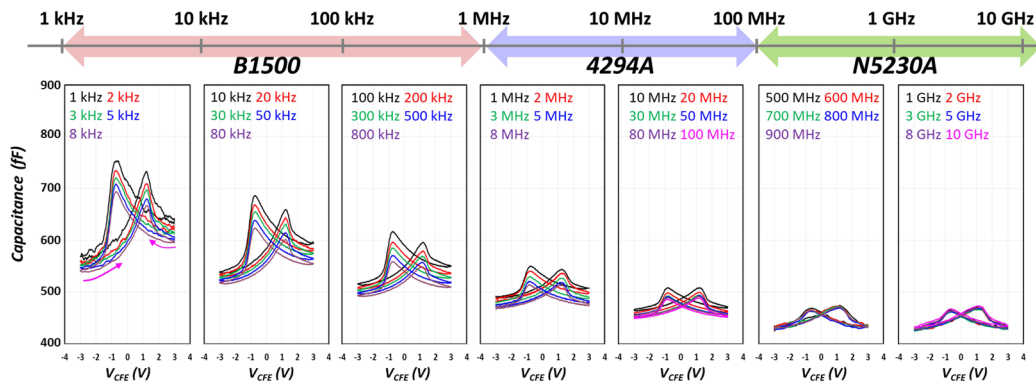
T. Kim, J. Grajal, I. S. Meiras, E. R. Borujeny, D. A. Antoniadis, J. A. del Alamo
Sponsorship: Semiconductor Research Corporation (2020-LM-3000), Samsung Electronics

Ferroelectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (FE-HZO) has attracted enormous interest as a material for future semiconductor devices due to its CMOS compatibility and highly scalable thickness, in contrast with conventional FE materials. FE-HZO has been extensively studied using time-domain large-signal transients at high frequencies to understand its switching behavior. However, its small-signal characteristics have yet to be explored at such frequencies. This is important because FE RF tunable capacitors are of practical interest due to their butterfly-shaped capacitance-voltage (C-V) characteristics and high permittivity. In addition, C-V characteristics constitutes a powerful technique for material and device characterization. Thus, we are exploring the small-signal C-V characteristics of FE-HZO Metal-Ferroelectric-Metal (MFM) structures in the GHz frequency range.

An impedance-matched layout and a precise de-embedding technique are crucial to obtaining accurate small-signal C-V curves in the GHz range. MFM structures were designed adopting a ground-signal-

ground (GSG) coplanar waveguide configuration to minimize reflected signals during RF measurements. After layout verification using electromagnetic simulations, devices were fabricated on sapphire wafers. We carried out measurements using three different tools to cover a frequency range spanning over 7 orders of magnitude, from 1 kHz to 30 GHz. Intrinsic C-V characteristics were extracted through de-embedding based on integrated calibration structures (Open, Short, and Thru) fabricated on the same chip.

Our results provide new information. First, the characteristic butterfly-shaped C-V curve remarkably persists into the GHz range with fixed peak capacitance positions in voltage across the entire frequency range. Second, the C-V curve becomes more symmetric and independent of frequency in the GHz range. This work will contribute to understanding the small-signal dynamics of the FE-HZO in the GHz regime and designing FE-HZO RF applications.



▲ Figure 1: C-V characteristics of intrinsic FE $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ MFM structures in a coplanar waveguide configuration measured from 1 kHz to 10 GHz.

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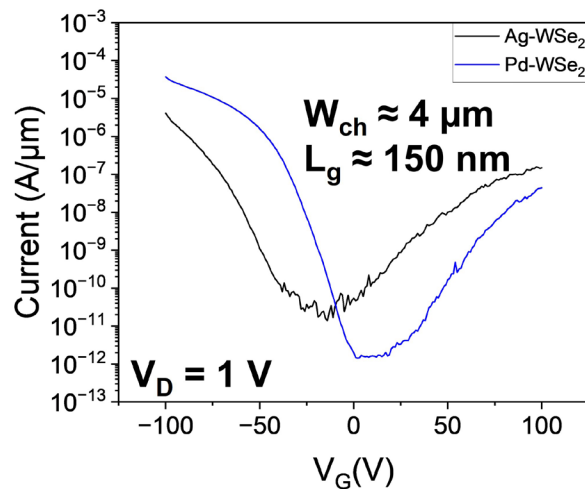
High-p Performance P-type 2D Transistors with Low-r Resistance Contacts

H. W. Lee, J. Zhu, J. H. Park, Y. Hou, J. S. Moodera, J. Kong, T. Palacios
Sponsorship: Intel (Intel Strategic Research Area)

Among all the emerging materials, two-dimensional (2D) semiconductors appear to be promising for the next generation electronics due to their atom layer thickness, relatively wide band gap, and high mobility. Whereas numerous extensive researches have been focused on n-type 2D semiconductors, e.g., molybdenum disulfide (MoS_2), in the past decades, p-type 2D materials, e.g., tungsten diselenide (WSe_2), have not been explored sufficiently but, which have equal importance in building 2D complementary metal-oxide-semiconductor (CMOS) circuits. In particular, reducing the contact resistance between a p-type 2D channel and a metal contact to a silicon transistor-comparable level is essential to achieve a high-performance p-type transistor.

In this work, we demonstrate a high-performance p-type WSe_2 transistor with palladium (Pd) contacts.

Monolayer WSe_2 film is directly synthesized on SiO_2/Si substrate using metal organic chemical vapor deposition (MOCVD). Pd contacts are sequentially formed with molecular beam epitaxy (MBE) technique, at a high vacuum level (3×10^{-10} Torr). This allows an ultra-clean interface between the WSe_2 and Pd, which results in low contact resistance. Moreover, we analyze the quality of contacts formed at different pressure levels by two different methods, i.e., using MBE and conventional electron beam evaporation ($10^{-6} \sim 10^{-7}$ Torr). This research on high-performance p-type 2D transistor with reduced contact resistance will be an important step for the using 2D materials in CMOS circuits. For future work, we will expand our research on ohmic contact by exploiting semi-metal contacts which can reduce metal-induced gap states (MIGS) between semiconductors and contact materials.



▲ Figure 1: Transfer curve of Ag- WSe_2 device and Pd- WSe_2 device under $V_D = 1$ V. Pd- contacted device shows p-type performance with sharp threshold swing.

FURTHER READING

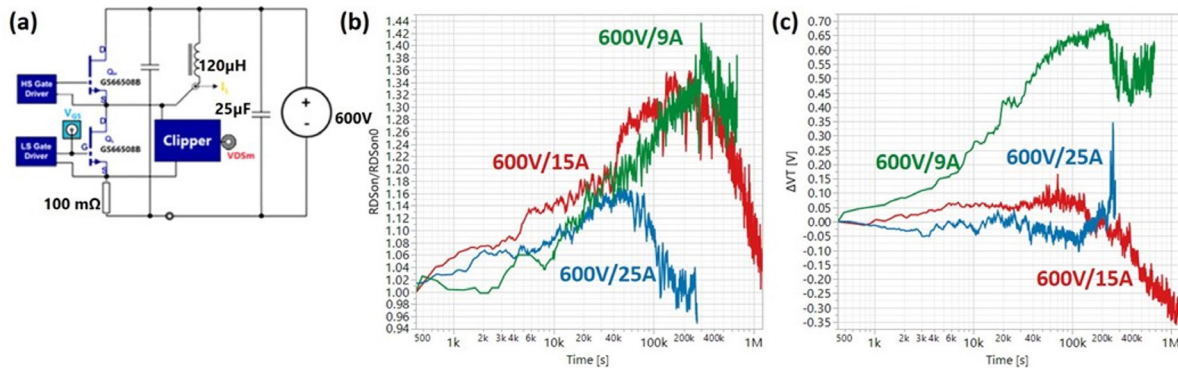
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In-situ Monitoring of GaN Power Transistor Parameters Under Continuous Hard-switching Operation

A. Massuda, J. A. del Alamo
Sponsorship: Analog Devices

GaN high-electron-mobility transistor (HEMT) technology is a promising candidate for next-generation power devices. Since power management applications involve operating the transistors under repeated switching, reliability and robustness are significant concerns. Under switching operation, critical parameters such as the dynamic on resistance, $R_{DS(ON)}$, and the turn-on gate threshold voltage, V_T , are subject to the influence of various trapping effects. When operating under hard-switching conditions, the device is subjected to high current and high voltage levels simultaneously. This operation mode causes a drift in important device parameters, which presents a limitation to the large-scale application of GaN power devices.

This work aims to devise techniques to continuously monitor V_T and $R_{DS(ON)}$ under hard-switching operation and to investigate the role of switching transitions on device parameter drift. To this end, we have constructed a unique experimental setup capable of repeating the double-pulse testing technique multiple times and measure device parameters in situ. Figure 1 demonstrates the evolution of V_T and $R_{DS(ON)}$ under hard-switching conditions and various stress conditions. V_T and $R_{DS(ON)}$ drift markedly, and a correlation between V_T and $R_{DS(ON)}$ degradation is observed. This suggests that a single underlying mechanism may be responsible for both drifts.



▲ Figure 1: (a) Schematic diagram for the double pulse test (b) $R_{DS(ON)}/R_{DS(ON0)}$ and (c) ΔV_T degradation during hard-switching operative mode.

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Use of Ion Implantation to Engineer the Electric Field Profiles in GaN Superjunctions

M. Oh, J. Perozek, J. Hsia, T. Palacios
Sponsorship: ARPA-E

Power electronics play a significant role in various applications, such as power grids and electric vehicles. Power transistors are required to block high voltages while having a low resistance to reduce power consumption during operation. Gallium Nitride (GaN) is highly promising in this context due to its wide band-gap and excellent transport parameters compared to other semiconductors such as Si. Additionally, superjunction structures consisting of alternating n- and p-type columns have significantly improved the performance of Si-based power transistors, since they can overcome the limitation on the trade-off between high breakdown voltage and low ON resistance. However, GaN vertical superjunctions have never been reported so far due to the difficulties in the epitaxial growth and fabrication.

In this work, the feasibility of fabricating GaN superjunctions through ion implantation is explored through simulation. Stopping and Range of Ions in Matter (SRIM) is used to acquire the estimated Si doping profiles in p-GaN substrate for several sets of ion implantation parameters. Technology Computer Aided Design (TCAD) simulation is conducted using Silvaco ATLAS simulator with the doping profiles from SRIM to verify the two-dimensional electric field profiles in the superjunction structure. Finally, the ion implanted lateral superjunction structures were proposed to investigate the charge balance between p-doped and n-doped regions.

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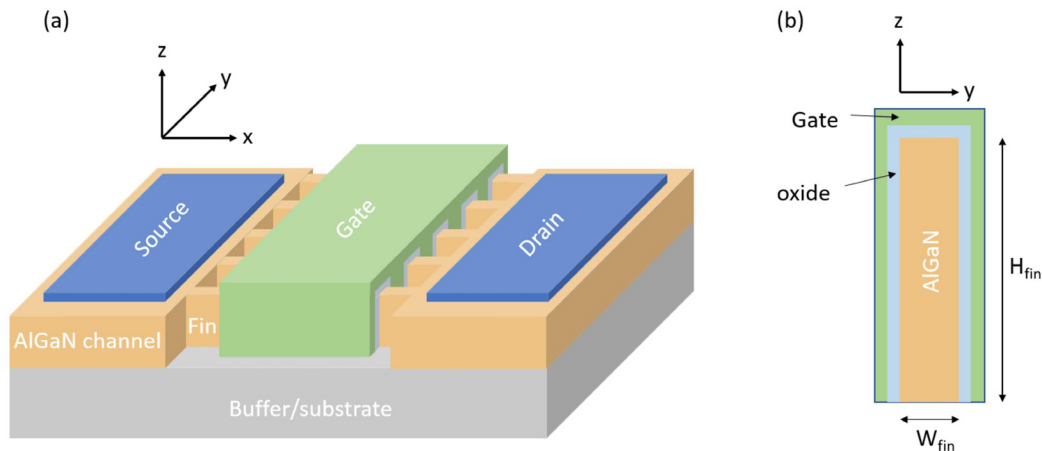
High-power AlGaN FinFET for mm-Wave Applications

H. Pal, P.-C. Shih, J. Niroula, Q. Xie, T. Palacios
Sponsorship: U. S. Army Research Office

High-frequency electronics is becoming increasingly important for today's commercial, military, and space communication needs. To enable the mm-wave 5G network, power amplifiers need to provide high power density, gain, efficiency, and linearity; but the performance of state-of-the-art GaN high-electron-mobility transistors (HEMTs) is limited for frequencies > 30 GHz. AlGaN is an ultra-wide band gap material that has 3-5 times higher Johnson's figure of merit (JFOM) than GaN due to its much higher breakdown electric field (> 8 MV/cm). Therefore, AlGaN devices have the potential to surpass

GaN HEMTs and achieve a much higher power density at frequencies > 90 GHz as well as better linearity and efficiency at lower frequencies.

In this project, we propose to leverage the superior material properties of high-Al content AlGaN to fabricate a fin field-effect transistor (finFET) with fins of aspect-ratio (H_{fin}/W_{fin}) > 20:1. The tall fin structure increases the effective width of the channel and hence would lead to a higher current density and power density, thus enabling mm-wave applications.



▲ Figure 1: (a) Schematic of the proposed AlGaN finFET. (b) Cross section of the fin, target $H_{fin} > 2 \mu\text{m}$.

Highly-scaled Vertical Nanowire GaSb/InAs Tunnel FETs

Y. Shao, J. A. del Alamo
Sponsorship: Intel Corporation

Tunnel field-effect transistors (TFETs) have attracted great attention due to their ability to operate with a sub-thermal subthreshold swing (S), which promises significant reduction in supply voltage and static power consumption in logic circuits. III-V materials are of particular interest in designing TFETs, thanks to the flexibility of band engineering and their superior transport properties. To date, III-V n-type TFETs with $S < 60$ mV/dec and decent drive current have been demonstrated. Looking forward, stringent logic transistor scaling forces a sub-10-nm critical dimension, which requires a detailed study of the potential of TFETs in this strong quantum-confinement regime.

In this work, we have fabricated sub-10-nm diameter vertical nanowire (VNW) GaSb/InAs broken-

band TFETs through a top-down approach. Negative differential resistance is clearly observed, which confirms the band-to-band tunneling operation of our transistors. An exemplar device demonstrates an on-state current of $300 \mu\text{A}/\mu\text{m}$ with a peak transconductance of $\sim 900 \mu\text{S}/\mu\text{m}$ at $V_{\text{ds}} = 0.3$ V, a record on-state performance of any TFET. Average S (calculated over 1 decade of current or more) breaking thermionic limit at room temperature is also obtained, demonstrating the potential of achieving combined high performance in on-state and subthreshold regimes. This work shows the great potential of ultra-scaled III-V VNW TFETs for future logic circuit applications.

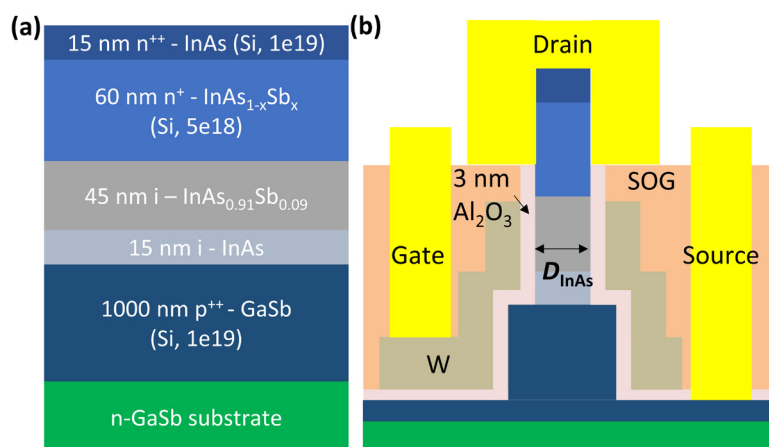
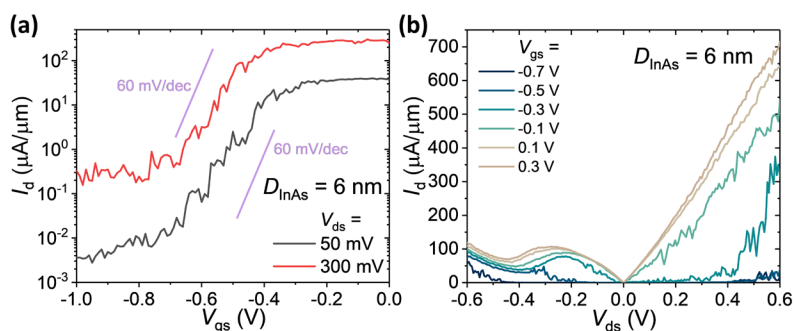


Figure 1: Schematics of (a) starting heterostructure and (b) device cross-sectional view.

Figure 2: (a) Output and (b) subthreshold characteristics of a VNW TFET.



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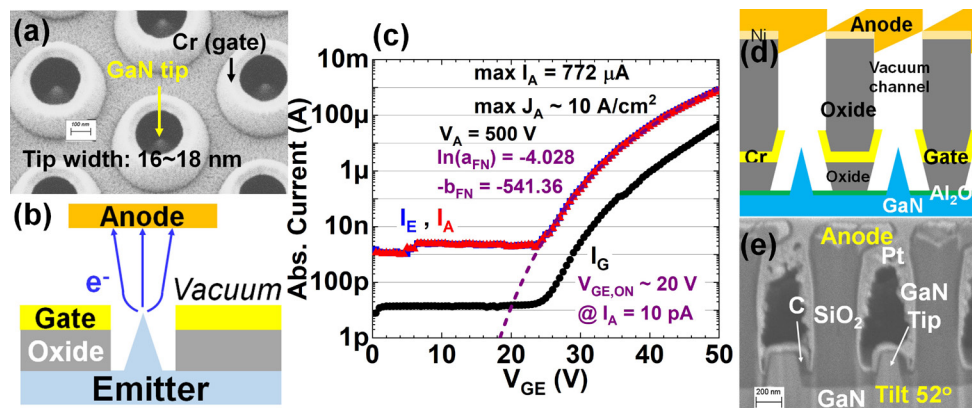
GaN Field-emission-based Vacuum Transistors

P.-C. Shih, J. Perozek, T. Palacios in collaboration with A. I. Akinwande
Sponsorship: U.S. Air Force Office of Scientific Research through Multidisciplinary University Research Initiative Empty State Electronics Project

Though vacuum electronics have been replaced by solid-state electronics in most commercial applications, the vacuum channel has intrinsic benefits, such as high electron saturation velocity and high breakdown field. Therefore, vacuum electronics, such as traveling wave tubes and gyrotrons, are still the main options for ultra-high power and high frequency (>100 GHz) applications. Furthermore, since the vacuum channel is theoretically robust toward radiation, vacuum electronics are also good candidates to build integrated circuits for space applications. However, current vacuum electronics are bulky and energy-consuming, which is a bottleneck for vacuum-electronic-based circuit applications.

III-Nitride semiconductors can improve vacuum transistors' performance and power consumption thanks to their engineerable electron affinities and high bonding energies. In this work, the state-of-the-

art GaN field-emission-based vacuum transistors are demonstrated with uniform and sub-20-nm-width emitter tips. The best GaN vacuum transistor has turn-on voltage ($V_{GE,ON}$) of 20 V and drive current (I_A) of 770 A at $V_{GE} = 50$ V, corresponding to current density (J_A) of 10 A/cm². Its drive current density and gate leakage are better than state-of-the-art Si vacuum transistors at the same bias condition. In the future, by combining devices with anode-integrated structures, the in-situ vacuum cavity packaging is possible. Compact and high-performance GaN field-emission-based vacuum transistors are thus promising for high-frequency and high-power electronics in harsh environments. Vacuum-electronics-based integrated circuits are also great candidates in tiny spacecrafts with laser sails for future space exploration and femto-satellites.



▲ Figure 1: (a) Scanning electron microscopy (SEM) image of finished device, (b) illustration of measurement setup, (c) transfer characteristics of state-of-the-art GaN field-emission-based vacuum transistor, (d) proposed fully integrated vacuum transistors, and (e) cross-sectional SEM image of preliminary experiments on anode-integration structure.

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Cold-source FET with Graphene/MoS₂ Heterojunction

P. Wu, X. Ji, J. Kong

Sponsorship: MIT Lincoln Laboratory Advanced Concept Committee

Transistors with steep subthreshold slopes (SS) are of interest for reducing the supply voltage and thus the power consumption of integrated circuits. However, existing steep-slope device concepts, such as tunnel FET (TFET), nanoelectromechanical (NEM) relay and impact-ionization MOSFET (I-MOS), have limitations in terms of on-current, switching speed, reliability, etc. In this work, we investigate cold-source field-effect transistor (CS-FET) based on graphene/MoS₂ heterojunction as a candidate for steep slope transistor, which relies on low-pass energy filtering from the graphene source to enable cold carrier injection. Since no band-to-band tunneling (BTBT) is involved in the transport, CS-FET could potentially achieve higher on-current than TFET. We study chemical vapor deposition (CVD)

synthesis of in-plane stitched graphene-MoS₂ heterojunction as a route to reduce the contact length between the graphene source and the MoS₂ channel and minimize the rethermalization of the cold carriers caused by inelastic scattering. We demonstrate a baseline local-bottom-gated MoS₂ FET without graphene source that exhibits SS of 70mV/dec, highlighting the excellent electrostatic gate control. Finally, we discuss possible strategies to further scale down contact length, providing a guideline for realization of CS-FET.

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Towards Design Technology Co-optimization (DTCO) in High-temperature GaN-on-Si Electronics

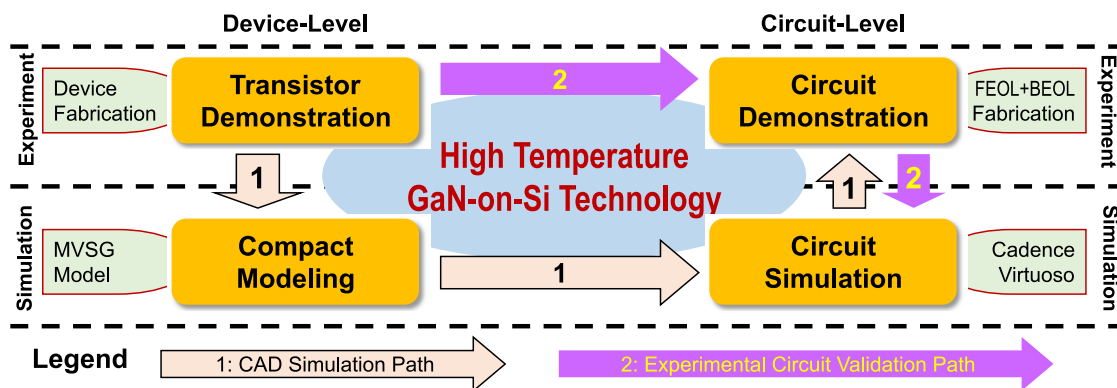
Q. Xie, M. Yuan, J. Niroula, B. Sikder, S. Luo, K. Fu, N. S. Rajput, A. B. Pranta, P. Yadav, Y. Zhao, N. Chowdhury, T. Palacios
 Sponsorship: NASA (Award No. 80NSSC17K0768), Lockheed Martin Corp. (Award No. 025570-00036), Air Force Office of Scientific Research (Award No. FA9550-22-1-0367), Qualcomm, Inc. (Award No. MAS-492857), Samsung Electronics Co., Ltd. (Award No. 033517-00001)

High-temperature (HT) electronics is critical for emerging applications in automotive (electric vehicles), renewable energy (geothermal), oil and gas exploration (deep drilling), and aerospace (hypersonic aircraft). Such harsh environments (> 250 °C) exceed the typical rating of silicon-on-insulator (SOI) technology. Recently experimental research has demonstrated the tremendous potential of high-temperature (HT) GaN transistors and basic circuits. At this critical juncture in the research of HT GaN technology, a computer-aided design (CAD) framework is needed to facilitate the development of larger, more integrated systems based on the proposed technology.

This work advances HT GaN-on-Si technology by taking important steps towards design technology co-optimization (DTCO). A CAD framework was established and experimentally validated up to 500 °C, the highest temperature achieved by such a framework for GaN technology. This framework was

made possible thanks to (1) demonstration of multiple key functional building blocks (e.g., arithmetic logic unit (ALU)) by the proposed technology at HT and (2) experimentally calibrated transistor compact models up to 500 °C (highest temperature modeled for an enhancement-mode GaN transistor). Excellent agreement was achieved between experimental and simulated circuits in the static characteristics (<0.1 V difference in voltage swing), and trends of dynamic characteristics (timing) were accurately captured.

By adopting complementary approaches in experiment and simulation, this work lays the foundation for the scaling-up of HT GaN-on-Si technology for mixed-signal applications at HT (>300 °C) electronics. In the broader context, this work offers insights for the scaling-up of nascent semiconductor technologies (as exemplified by the proposed GaN technology) to deliver practical microsystems.



▲ Figure 1: Roadmap for research on the proposed GaN HT technology. The green boxes indicate the key task or tool necessary to accomplish each module. The numbered arrows highlight the two complementary pathways adopted in this work to scale up the proposed technology.

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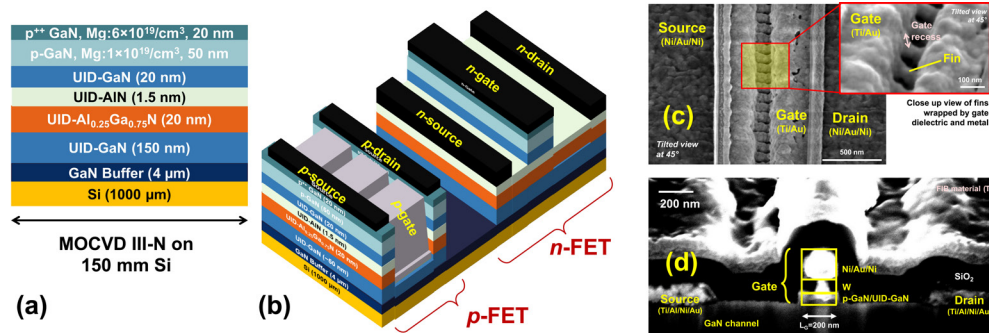
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GaN Complementary Transistor Technology

Q. Xie, M. Yuan, J. Niroula, B. Sikder, J. A. Greer, N. S. Rajput, N. Chowdhury, T. Palacios
 Sponsorship: Samsung Electronics Co., Ltd. (Award No. 033517-00001), Qualcomm, Inc. (Award No. MAS-492857), Intel Corp. (Award No. 027196-00001), Advanced Research Projects Agency-Energy (Award No. DE-AR0001591)

The rising performance of GaN power integrated circuits (ICs) has offered compactness and record levels of efficiency and power for data centers, power adapters, electric vehicles (EVs), and 5G telecommunication systems. However, the lack of a practical GaN p-channel field-effect transistor (FET) significantly increases the static power dissipation (resulting from the use of n-type enhancement-mode/depletion-mode logic), resulting in an important roadblock towards all-GaN integration (e.g., control loops, analog mixed-signal blocks). Furthermore, the availability of high-side switching GaN p-FETs would circumvent the switching speed bottleneck (limited common-mode transient immunity (CMTI) in the level shifter), therefore enabling more efficient power converters.

In recent years, extensive research has been pursued at MIT in the emerging domain of GaN complementary technology (CT), including: (1) integration of p-FET and n-FET on the same platform without the need of regrowth of III-N material; (2) a scalable platform for eventual commercialization; (3) ability to withstand the large heat generation in EVs, data centers, and base stations; and (4) high p-FET and n-FET performance. The reported progress has been enabled by a combination of new device structures (e.g., self-aligned p-FinFET) and process optimization (e.g., techniques to reduce etch-induced damage). Current research effort is focused on advancing device-level performance and exploration of novel GaN complementary circuits.



▲ Figure 1: Highly-scaled GaN CT. (a) Epitaxial structure. (b) Device structures of p-FET (SA FinFET) and n-FET (SA-gate p-GaN-gate HEMT) based on the same GaN-on-Si platform as in Figure 1(a), (c), (d) Scanning electron microscopy (SEM) images of representative p-FET and n-FET, respectively.

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GaN Memory Operational at 500 °C

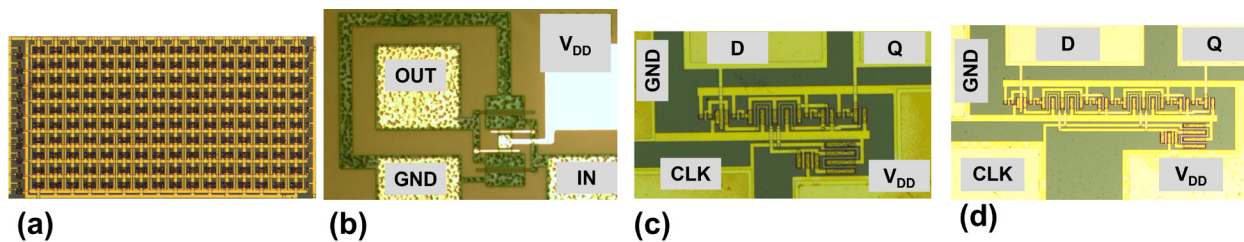
M. Yuan, Q. Xie, J. Niroula, K. Fu, S. Luo, N. Chowdhury, Y. Zhao, T. Palacios

Sponsorship: NASA (Award No. 80NSSC17K0768), Lockheed Martin Corp. (Award No. 025570-00036), Air Force Office of Scientific Research (Award No. FA9550-22-1-0367)

The rapid growth of high temperature (HT, >300 °C) electronic applications in the fields of aerospace, automotive, oil and gas exploration, and more requires fundamental advancements in semiconductor technology, among which GaN stands out as a leading material candidate. The focus of high-temperature (HT) GaN electronics has thus far been basic combinational logic building blocks. Memory, which is the storage of state information, is a fundamental requirement of any complex digital system, and is realized using sequential logic circuits.

The most commonly used memory cells, namely a 32-bit × 10-bit read-only memory, a 1-bit 4-transistor static random-access memory (SRAM), D latch, and

D flip-flop (DFF), were demonstrated using HT GaN technology on a monolithically integrated GaN-on-Si platform and n-field-effect transistor (FET)-only enhancement (E)/depletion (D)-mode logic. The memory cells exhibit stable operation at 300 °C. A maximum clock frequency of 36 MHz at 300 °C was estimated for the DFF using the measured setup time. Recently, the operational temperature of the DFF was pushed to 500 °C. To the best of the authors' knowledge, the operational temperature of the reported prototypes represents the highest value for GaN memory, paving the way for the realization of robust mixed-signal systems operating at HT.



▲ Figure 1: GaN memory cells demonstrated to work at HT. (a) 32-bit × 10-bit read-only memory (ROM). (b) 1-bit 4-transistor SRAM. (c) D latch. (d) DFF.

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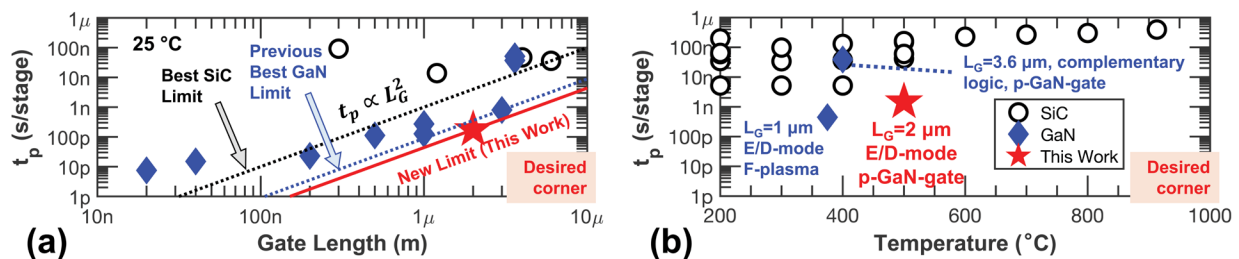
GaN Ring Oscillators Operational at 500 °C

M. Yuan, Q. Xie, K. Fu, T. Hossain, J. Niroula, J. A. Greer, N. Chowdhury, Y. Zhao, T. Palacios
 Sponsorship: NASA (Award No. 80NSSC17K0768), Lockheed Martin Corp. (Award No. 025570-00036), Air Force Office of Scientific Research (Award No. FA9550-22-1-0367)

Emerging applications such as deep well oil drilling, hypersonic aircrafts, and exploration of Venus require high temperature (HT)-rated electronics components beyond the silicon-on-insulator (SOI) technology's typical temperature limit of 250 - 300 °C. Wide band gap semiconductors (SiC and GaN) are well suited to meet this demand thanks to their wide band gap, which is responsible for negligible carrier thermal generation at these temperatures. While early research has demonstrated the promising potential of GaN transistors for HT application, their use in HT digital and analog circuits remains a relatively unexplored area.

A study of GaN for HT (up to 500 °C) digital circuits was conducted. An HT-robust GaN-on-Si technology based on enhancement-mode p-GaN-gate AlGaIn/GaN high electron mobility transistors (HEMTs) and depletion-mode AlGaIn/GaN HEMTs was proposed

and used to implement different digital circuit configurations, namely E/D-mode and E/E-mode (E: enhancement, D: depletion). The E/D-mode inverter was found to offer significantly better performance in terms of voltage swing, noise margin, and gain across temperature and power supply voltage (V_{DD}) scaling. As calculated from E/D-mode ring oscillators (ROs) with $L_G=2 \mu\text{m}$, a 7-stage RO exhibited a propagation delay (t_p) of $< 1.48 \text{ ns/stage}$ at 500 °C. The best RO achieved $t_p < 0.18 \text{ ns/stage}$ at 25 °C. To the best of the authors' knowledge, the proposed technology sets a new boundary of t_p vs. L_G^2 in wide band gap digital logic and is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology for emerging HT applications at 500 °C and beyond.



▲ Figure 1: Summary of ROs based on wide band gap electronics (GaN and SiC). (a) t_p vs. L_G . General scaling trends ($t_p \propto L_G^2$) for best SiC demonstration, previous best GaN demonstration, and best result of this work. L_G of pull-down transistor is chosen. (b) t_p vs. temperature.

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Enhancement-mode GaN Transistor Technology for Harsh Environment Applications

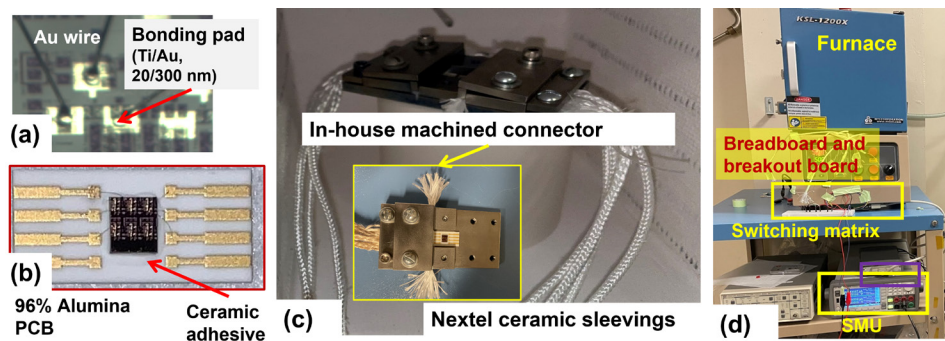
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Sponsorship: NASA (Award No. 80NSSC17K0768), Lockheed Martin Corp. (Award No. 025570-00036), Air Force Office of Scientific Research (Award No. FA9550-22-1-0367)

Enhancement-mode (E-mode) GaN transistor technology could significantly increase the performance of GaN power electronics as well as enable complex analog mixed-signal circuits through n-field-effect transistor (FET)-only logic or complementary logic. In this work, the suitability of E-mode p-GaN-gate AlGaN/GaN high-electron-mobility transistors (HEMTs) for harsh environment operation, specifically high temperature (HT), was systematically evaluated. To this end, two rounds of tests were conducted.

First, the device under test (DUT) was placed in a furnace at 500 °C in nitrogen ambient. In-situ measurements from room temperature (RT) to 500 °C show that trends in transistor performance are largely as expected based on first-order changes in the semiconductor properties. The DUT exhibited stable performance over 20 days at 500 °C.

Second, the DUT was placed in the NASA Glenn Extreme Environment Rig (GEER, located in Cleveland, Ohio) in a simulated Venus ambient (460 °C, ~90 atm., corrosive gases) for 10 days. The robustness of the DUT was evaluated by two complementary approaches: (1) in-situ electrical characterization, where proper transistor operation (including E-mode V_{TH} with < 0.09 V variation) was demonstrated in extreme environments; and (2) advanced microscopy investigation of the device after test, which revealed the effect of the testing on the epitaxial structure.

To the best of the authors' knowledge, this is the first demonstration and comprehensive analysis of E-mode GaN transistors in such harsh environments. The results establish the reported technology as a leading option for harsh environment mixed-signal applications.



▲ Figure 1: Experimental setup for in-house HT (up to 500 °C) measurement, illustrating from DUT to overview. (a) DUT. (b) Printed circuit board (PCB) of 98% alumina. Bare die is attached using ceramic adhesive. (c) Custom-made packaging for HT measurement wrapped in 3M™ Nextel™ sleeveings. (d) Overview.

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First Demonstration of GaN RF HEMTs on Engineered Substrate

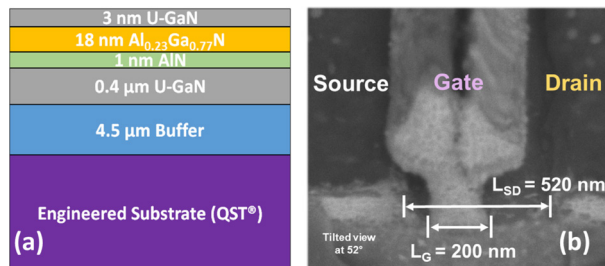
P. Yadav, Q. Xie, J. Niroula, G. K. Micale, H. Pal, T. Palacios

Sponsorship: Air Force Office of Scientific Research, SRC, Advanced Research Projects Agency–Energy

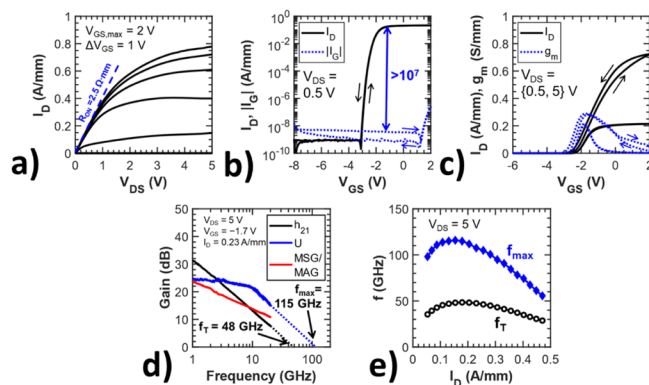
GaN transistors have continued to push the limits of high-power-density, high-frequency semiconductor devices. Novel GaN devices have been developed with engineered linearity, novel heterogeneous integration with state-of-the-art Si control circuits, complementary n- and p-channels, and advanced physics-based modeling. Such devices will contribute to the foundation of the next generation of radio-frequency (RF) and mixed-signal circuits for a diverse set of applications, from 6G to hypersonic vehicles. For these RF applications, silicon carbide has long been the substrate of choice for GaN high-electron-mobility transistors (HEMTs) due to its low lattice mismatch with GaN, high thermal conductivity, and extremely high substrate resistivity; however, it remains one of the most expensive growth substrates, and scalability to large wafer diameters is a major concern. On the other hand, Si is also a common substrate for GaN HEMTs as it is cost effective and scalable but suffers from a high lattice mis-

match. The engineered substrate (Qromis QST®) offers a cost-effective, scalable solution similar to Si but with thermal lattice matching and lower dislocation density. Early device experiments on GaN-on-engineered substrates have focused on power transistors, but RF applications remain to be explored.

The epitaxial structure of the engineered substrate used in this work is shown in Figure 1(a). A scanning electron microscope (SEM) image of the fabricated transistor is presented in Figure 1(b). The reported HEMT featured a source-to-drain distance, L_{SD} , of 520 nm and a gate length, L_G , of 200 nm. Figure 2(a-c) shows the DC characteristics of the HEMT with a gate width of $2 \times 25 \mu\text{m}$. Given the promising RF performance of $f_T/f_{\text{max}} = 48/115 \text{ GHz}$ as seen in Figure 2 (d-e) and the availability of large diameter (8 in.) substrates, GaN HEMTs on engineered substrates have strong potential for use in applications such as 6G.



▲ Figure 1: (a) AlGaIn/GaN epitaxial structure on engineered substrate (QST®). (b) Cross section of a fabricated transistor, showing $L_{SD}=520 \text{ nm}$, $L_G=200 \text{ nm}$.



▲ Figure 2: DC characteristics of a fabricated transistor and cut-off frequencies f_T and f_{max} as a function of drain current with $L_G = 200 \text{ nm}$. (a) Output characteristics. (b)–(c) Transfer characteristics, in logarithmic and linear scales, respectively. (d) Small-signal gain without de-embedding. (e) Cut-off frequencies f_T and f_{max} as a function of drain current.

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Epitaxial Perovskite Ferroelectric-based Capacitive Memory

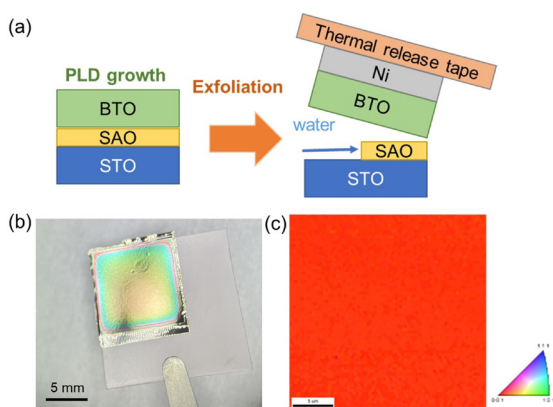
X. Zhang, M-K. Song, C. S. Chang, S. Lee, J. Kim

Sponsorship: Intelligence Advanced Research Projects Agency MicroE4AI Program

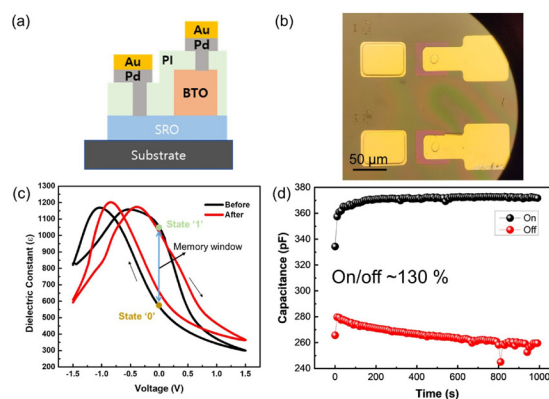
Nowadays, development of artificial intelligence requires more power-efficient memory devices. Compared to the conventional resistive memory, capacitive memory devices are quite promising as they eliminate static power consumption and prevent IR drop by leveraging charge transfer. However, the widely used $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) is polycrystalline and has high coercive field, resulting in significant variations when scaled to nanoscale and high write energy. On the other hand, single-crystalline perovskite ferroelectric oxides like BaTiO_3 (BTO) have better uniformity and a coercive field 2~3 orders of magnitude lower than HZO. Furthermore, the 100x higher dielectric constant can also enlarge the memory window. Previous study used buffer layer for silicon compatibility, resulting in poor performance.

This project investigates epitaxial perovskite ferroelectric material for an energy-efficient, high-performance, and complementary metal-oxide

semiconductor (CMOS)-compatible capacitive memory device. As shown in Figure 1, freestanding single-crystalline BTO is obtained by chemical lift-off technique using $\text{Sr}_3\text{Al}_2\text{O}_6$ as the sacrificial layer. Good crystallinity is confirmed by electron backscatter diffraction (EBSD). Then the BTO membrane is transferred onto polymer-coated silicon and fabricated into capacitors. Polarization switching in BTO film leads to a butterfly-shaped capacitance-voltage curve with 1.5V switching voltage (Figure 2). An asymmetric electrode is designed to achieve curve shift with an on/off ratio of 150% at zero bias. Both the coercive voltage and memory window we propose are better than in HZO-based devices. Our device also shows stable performance with over 1000 cycles of endurance and over 1000s of retention. This capacitor memory device serves as a good element in crossbar array for the next generation of in-memory computing.



▲ Figure 1: (a) Schematic process of freestanding BTO fabrication; (b) Optical image and (c) EBSD image of freestanding BTO.



▲ Figure 2: (a) Schematic structure and (b) optical image of capacitive memory device based on single-crystalline BTO; (c) Dielectric constant-voltage butterfly loops before and after exfoliation; (d) Retention time characteristics of memory device.

Energy and Sustainability

- A New Semiconducting Perovskite Alloy System Made Possible by Gas-source Molecular Beam Epitaxy..... 45
- Vapor Transport Co-deposition of Perovskite Photovoltaics 46
- Fabric Integration of Organic Photovoltaics 47
- Monte-Carlo-based Techno-economic Analysis of OPV and PSC Thin-film Solar Cells 48
- Predicting Next-generation Perovskite Solar Cell Performance through Machine Learning-induced Algorithms 49

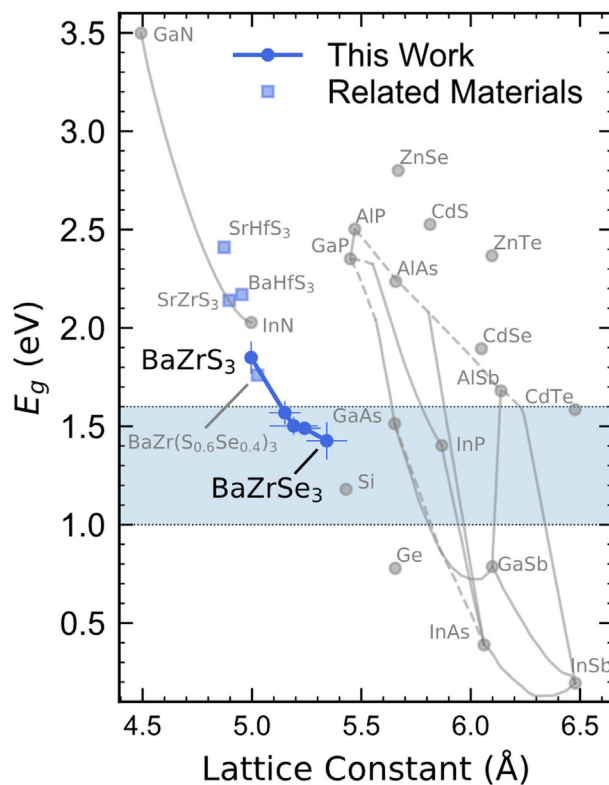
A New Semiconducting Perovskite Alloy System Made Possible by Gas-source Molecular Beam Epitaxy

I. Sadeghi, J. V. Sambeek, T. Simonian, M. Xu, K. Ye, V. Nicolosi, J. M. LeBeau, R. Jaramillo

Sponsorship: NSF (grant numbers 1751736, 1745302); Air Force Office of Scientific Research (Grant No. FA9550-20-0066)

Chalcogenide (sulfide and selenide) semiconductors in the perovskite crystal structure are anticipated to have favorable structural, optical, and electronic characteristics for solar energy conversion. The most studied compound is BaZrS_3 , with a band gap of 1.9 eV. Alloying on the anion or cation sites has been explored to lower the band gap into a range suitable for single-junction solar cells. The pure selenide perovskite, BaZrSe_3 , has been theoretically predicted to have band gap 0.5 eV lower than the sulfide. However, BaZrSe_3 may form in different polymorphs; theory predicts that the needle-like (non-perovskite) phase with band gap below 1 eV is the most stable, and solid-state synthesis attempts have resulted in a semi-metallic hexagonal ordered defect phase.

In 2021, we reported the first epitaxial synthesis of chalcogenide perovskite thin films by gas-source molecular beam epitaxy (MBE): BaZrS_3 film on LaAlO_3 substrate. Now we report alloying BaZrS_3 with Se, including the first report of a pure selenide perovskite. We confirm that this alloy system features a direct band gap that is tunable in the range 1.4 – 1.9 eV. This work sets the stage for developing chalcogenide perovskites as a family of semiconductor alloys with properties that can be tuned with composition in high-quality thin films made by heteroepitaxy, as has been long-established for other semiconductor materials. The band gap of high-selenium-content $\text{BaZrS}_{(3-y)}\text{Se}_y$ suggests applications in thin-film solar cells.



◀ Figure 1: Cho plot representing chalcogenide perovskites as new family of semiconductor alloys. Deep blue points represent $\text{BaZr}(\text{S},\text{Se})_3$ alloy series reported here as epitaxial thin films. Light blue points represent other chalcogenide perovskites, reported elsewhere as solid-state synthesis of bulk powders. Other data are established semiconductors and alloy families. Direct (indirect) band gap alloys are indicated by solid (dashed) lines. Colored band indicates range of appropriate for single-junction solar cells. For chalcogenide perovskites, abscissa is pseudo-cubic lattice constant (\AA); horizontal error bars represent composition variation through film thickness.

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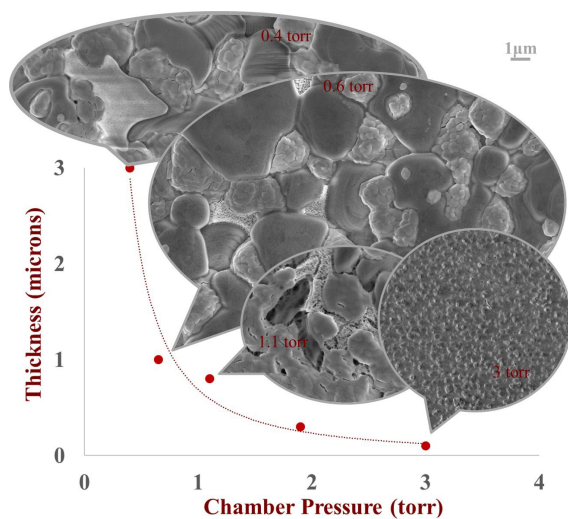
Vapor Transport Co-deposition of Perovskite Photovoltaics

T. K. Zhitomirsky, E. L. Wassweiler, H. L. Tuller, V. Bulović
Sponsorship: U.S. Department of Energy

Halide perovskites have demonstrated remarkably high solar-to-electrical energy conversion efficiencies and are therefore of great interest for rapid commercialization. Popular solution-based fabrication routes do not lend themselves to rapid scale-up as required. Vapor transport deposition (VTD) can be considered as a readily scalable, low-cost technique alternative method for perovskites production. Vapor-based processes promise to overcome many challenges imposed by solution-based techniques. Being solvent-free, they bypass solvent related challenges, namely uniform coverage of large areas, chemical compatibility, and toxicity. As a low-cost alternative to thermal evaporation, VTD has the potential to deposit organic and inorganic perovskite precursor materials either sequentially or via co-deposition. Furthermore, VTD potentially offers higher tunability of deposition parameters, to enable

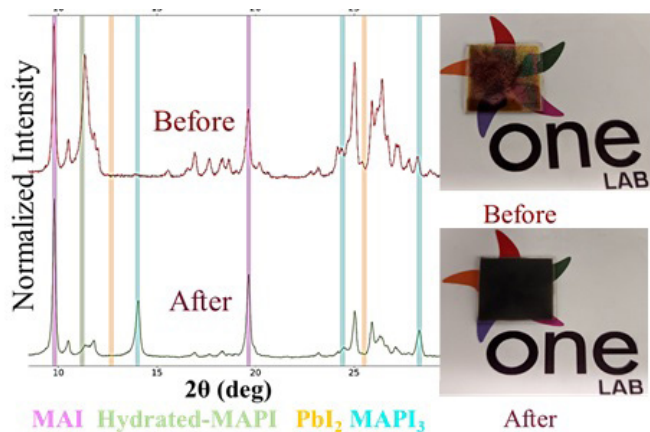
film growth with improved composition and microstructure control. However, since it is a newly developing technique, we still need to prove its viability in producing high-quality perovskite films.

We are currently working with a custom-made VTD system, focused on optimization of co-deposition of lead iodide and methylammonium iodide with the aid of a carrier gas. Figure 1 shows the influence of chamber pressure on deposition rate and film microstructure. We found that there is an inverse relation between chamber pressure and deposition rate, hence deposition of a 500-nm active layer required for a solar cell should take no more than 30 minutes, for pressures below 1 torr. Figure 2 demonstrates the importance of post-deposition treatments in forming the perovskite phase. These findings can serve us in fabricating solar cells utilizing this new technique.



◀ Figure 1: Film thickness as a function of chamber pressure.

► Figure 2: Before and after annealing of as-deposited perovskite films in 100C/5minutes. As shown by XRD, (X-ray diffraction) the treatment leads to improved crystallization of the perovskite material and eliminates the hydrated phase.



Fabric Integration of Organic Photovoltaics

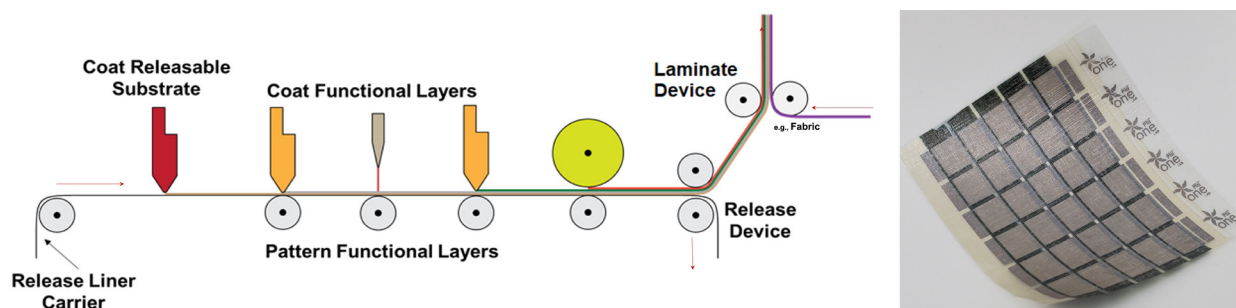
M. Saravanapavanantham, J. Mwaura, V. Bulović

Sponsorship: Eni S.p.A. through the MIT Energy Initiative, NSF, Natural Sciences and Engineering Research Council of Canada

The ubiquitous and imperceptible integration of optoelectronics into the world around us allows for novel modes of energy harvesting, communications, sensing, information display, and computing. To date, owing to the availability of foundries and scalable processing modalities, this integration has been achieved via fabrication of discrete elements that are then deterministically positioned throughout the world via pick-and-place assembly. Alternatively, the availability of large-area, ultra-thin, and continuous elements could enable seamless integration of electronics onto surfaces around us much like a second skin. Thin-film electronics, often fabricated with sub-micron device-functional layer thicknesses, present an avenue toward such mechanically imperceptible, large-area, and continuous integration of electronics onto any surface of choice—a paradigm that we refer to as "active surfaces."

In particular for power generation, the wet-solution processability of organic thin film

photovoltaics (PVs), through cheaper and less energy-intensive additive coating/printing techniques, presents an avenue towards seamlessly integrating power onto any surface of interest without significant addition in weight and topography. In this project, we demonstrate large-area, ultra-thin organic PV (OPV) modules produced with scalable solution-based coating/printing process for all the functional layers. We further demonstrate their transfer lamination onto lightweight and high-strength composite fabrics (Dyneema), resulting in durable fabric-PV systems ~50 microns thin, weighing under 1 gram over the module area (corresponding to an area density of 105 g/m²), and having a specific power of 370 W/kg. Integration of the ultra-thin modules onto composite fabrics lends mechanical resilience to allow these fabric-PV systems to maintain their performance even after hundreds of roll-up cycles.



▲ Figure 1: (Left) Schematic of the photovoltaic module printing and transfer lamination process, with a photo of the finished fabric-PV module (right).

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Monte-Carlo-based Techno-economic Analysis of OPV and PSC Thin-film Solar Cells

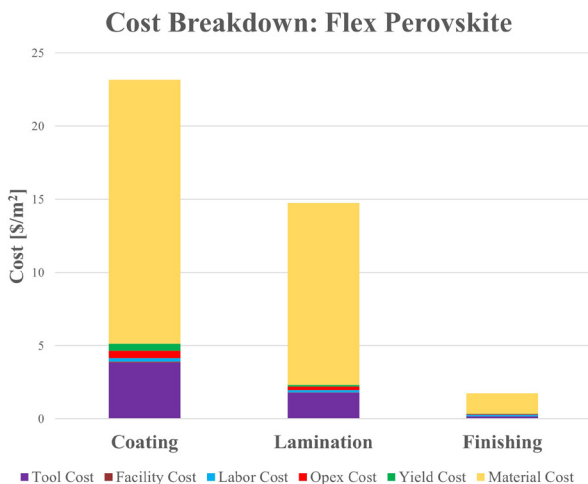
K. Yang, J. Mwaura, V. Bulović
Sponsorship: Tata Power

Although solution processed solar cells such as organic photovoltaics (OPVs) and perovskite solar cells (PSCs) have experienced rapid development in the past 10 years as a promising supplement to the already technologically mature silicon photovoltaics, these thin-film technologies are still in their infancy. Thus, few companies have commercialized OPVs, and limited demonstrations of large-scale manufacturing of PSCs have been done. It is prudent, therefore, to perform techno-economic analyses on setting up such a manufacturing plant before investing millions of dollars to build a factory.

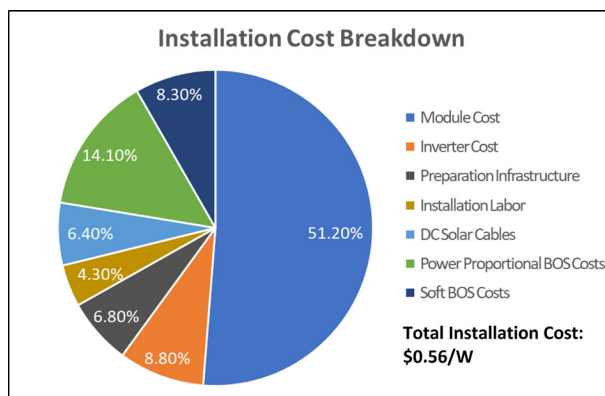
We implement Monte-Carlo simulation to model the cost of manufacturing OPV and PSC modules on a 100MW capacity level. The bulk of the OPV values are sourced from Sunew, a Brazilian company manufacturing OPVs with roll-to-roll technology. PSC values are sourced from the literature with a special focus on toxic solvent and humidity air handling. Because manufacturing comprises only a fraction of the overall deployment cost, we also calculated the

total installation cost of a solar array.

Because the manufacturing cost breakdown is similar across flexible and rigid OPVs and PSCs, a representative breakdown is shown in Figure 1 for flexible PSCs. Flexible PSCs cost $\$0.29/W_{pk}$, and flexible OPV costs $\$0.77/W_{pk}$, with the materials comprising the overwhelming majority. Although these values are higher than the $\$0.24/W_{pk}$ for silicon, the cost for raw materials will decrease with economies of scale. Figure 2 shows the contributions to the total installation cost beyond the module cost. Of particular note are the installation labor, preparation infrastructure, and racking hardware when comparing rigid and flexible films. Flexible films require fewer trucks for transportation, less labor for installation, and little to no racking, saving ~17% of the balance of system costs. Provided the current degradation issues regarding PSCs are fixed, this shows that emergent thin-film technologies are economically competitive with silicon.



▲ Figure 1. Manufacturing cost breakdown of flexible PSCs obtained using Monte Carlo simulation.



▲ Figure 2. Installation cost breakdown for flexible PSCs including balance of system (BOS) and module costs.

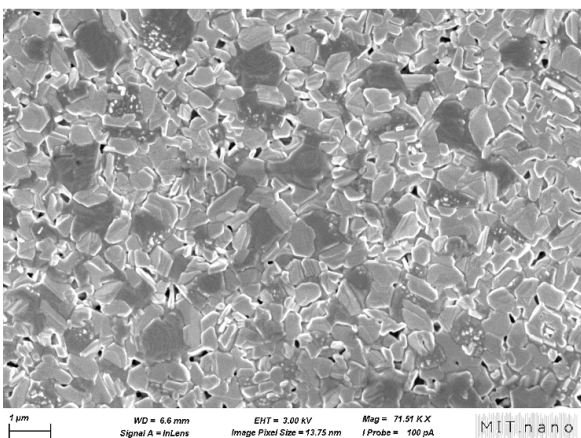
Predicting Next-generation Perovskite Solar Cell Performance through Machine Learning-induced Algorithms

R. Zhang, M. G. Bawendi, V. Bulović
Sponsor: U.S. Department of Energy

Organic-metal halide perovskites have promising optoelectronic properties, making them stand out in next-generation photovoltaic devices. However, the performance of a solar cell largely depends on the fabrication process or various film recipes. Specifically, most perovskite cells with record performance are laboratory-sized and not fabricated by large-area compatible printable methods like slot-die coating or roll-to-roll coating, etc. Hence, it is essential to predict the possible performance beforehand while investigating various novel perovskite inks. To better incorporate interfacial recombination between layers in the solar cell stack, band-bending, and internal electric fields developed due to the charge extraction layers and charge transport losses, models like drift-diffusion were employed to determine the relevant simulation parameters. Nevertheless, the number of free parameters in these models require extensive measurements and fitting models that hinder their usefulness as a predictive tool. Therefore, we have begun exploring the use of machine learning to take the measured physical parameters of

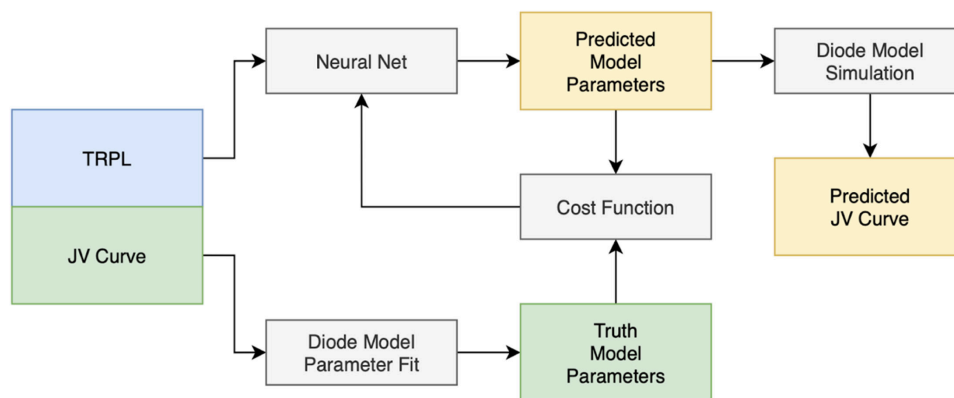
the cell as input and directly predict the current-voltage curve, thereby predicting the cell efficiency performance. These black box models (like neural networks) allow us to potentially predict the performance of full devices with data that might contain many physical processes which could be too complex to predict accurately with a physics-based model.

Various structures of the solar cell are fabricated through spin-coating and presented in the scanning electron microscope (SEM) picture below (left). We consider using percent transmission (%T), spectrum-resolved photoluminescence (SRPL) and time-resolved photoluminescence (TRPL) as representative characteristics for the algorithm. We have developed a neural network (simple architecture shown in right figure below) that inputs these three spectra to predict the output values of open-circuit voltage, short-circuit current and fill factors. A less than 10% of percent error between the predicted results and the ground truth performance is reached.



◀ Figure 1: SEM image of Perovskite thin film.

▼ Figure 2: Example of machine learning architecture in predicting output.



Integrated Photonics and Optoelectronics

Robust Bayesian Optimization for Integrated Photonics	51
Silicon Photonics for Chip-based 3D Printing	52
Underwater Free-space Optical Communications Using Integrated Optical Phased Arrays	53
Automatic Realization of Light Processing Functions for Programmable Photonics	54
Design of Quantum-dot Lasers using Plasmonic Nanocavities	55
Asymptotically Fault-tolerant Programmable Photonics.....	56
High-efficiency Mid-infrared InGaAs/InP Arrayed Waveguide Gratings.....	57
Flexible Wafer-scale Silicon-photonics Fabrication Platform	58
Dual-band Optical Collimator Based on Deep-learning Designed, Fabrication-friendly Metasurfaces.....	59
Optical Probes of Triplet Exciton Sensitization of Silicon	60
Metasurface for 3-D Depth Sensing.....	61

Robust Bayesian Optimization for Integrated Photonics

U. Chakraborty, D. Weninger, Z. Gao, L. C. Kimerling, A. Agarwal, D. S. Boning

Photonic integrated circuits are a promising platform for a wide range of applications, from quantum information processing to biosensing. However, packaging of photonic integrated circuits presents many challenges, such as achieving low-loss coupling of light from fibers (large optical modes) to on-chip waveguides (small optical modes). Novel design of fiber-chip couplers is an area of great interest for the future of photonic packaging. Optimizing the performance of couplers and other photonic devices using gradient-free heuristics typically requires the repeated use of the finite-difference-time-domain (FDTD) method to solve Maxwell's equations at a large number of discrete mesh points. However, FDTD simulations can be extremely time-consuming, necessitating alternative methods to optimize device designs using fewer simulations.

Bayesian optimization has emerged as a computationally-efficient approach which relies on Gaussian process regression to build surrogate models that predict device performance and thus significantly reduce the number of time-consuming FDTD simulations. It is essential to optimize photonic devices not only to maximize their peak performance, but also to render them robust to fabrication process variations. Here, we explore robust Bayesian optimization methods that allow the user to specify a trade-off between the device's peak performance and its insensitivity to parameter variations. We apply our methods to the design of photonic structures such as fiber-chip couplers, and evaluate the variation-insensitivity of devices optimized using our robust Bayesian algorithms.

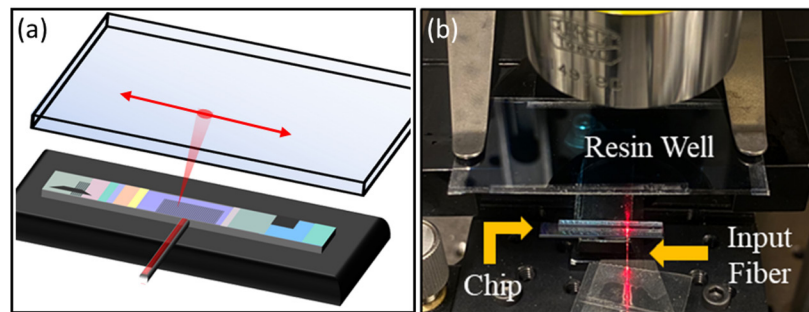
Silicon Photonics for Chip-based 3D Printing

S. Corsetti, M. Notaros, T. Sneh, A. Stafford, Z. Page, J. Notaros

Sponsorship: MIT Rolf G. Locher Endowed Fellowship, NSF Graduate Research Fellowship

Three-dimensional (3D) printing has facilitated diverse scientific advancements ranging from rapid prosthetic prototyping to forensic sample reconstruction. To maximize build speed while maintaining print quality, modern 3D printers rely on complicated systems for mechanical laser routing and specialized build platforms for strain reduction. The cost and upkeep of these systems, in addition to the UV-light printing standard, have prevented 3D printing from contributing to low-cost and biocompatible applications.

In this work, we develop an on-chip integrated photonic system that enables dynamic non-mechanical control of visible light and controllably cures a visible-light-curable liquid resin. This research takes the first step towards a form of 3D printing that will allow for non-mechanical, volumetric 3D printing with interference patterns generated by a single chip. The complete development of this technology would allow for inexpensive, rapid 3D printing in the biocompatible visible-light regime.



▲ Figure 1: (a) Conceptual diagram showing a photonic chip radiating visible light onto liquid resin, with an arrow to indicate beam-steering. (b) Photograph of the experimental setup and photonic chip.

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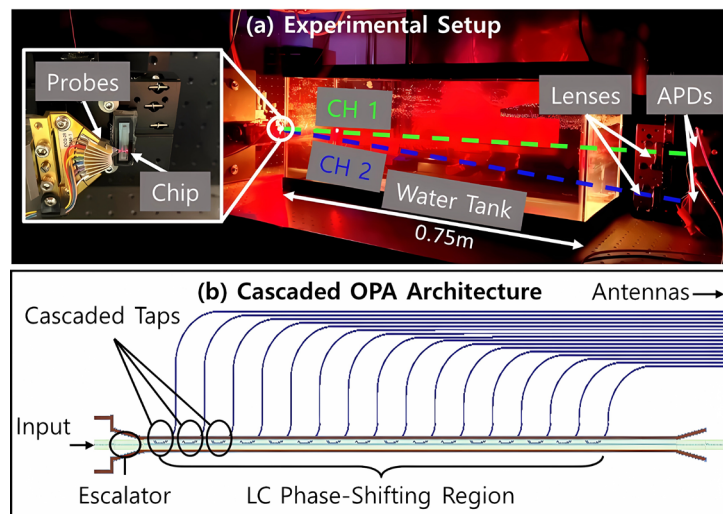
Underwater Free-space Optical Communications Using Integrated Optical Phased Arrays

D. DeSantis*, M. Notaros*, J. Notaros

Sponsorship: Defense Advanced Research Projects Agency Visible Integrated Photonics for Enhanced Reality program (Grant No. FA8650-17-1-7713), NSF Graduate Research Fellowship (Grant No. 1122374), MIT Rolf G. Locher Fellowship

Optical signals can transmit large quantities of data quickly, which has inspired the historic field of fiber-optic communications. Recently, free-space optical communications links have been demonstrated with infrared integrated optical phased arrays (OPAs) with speeds up to gigabits per second. However, a capability gap exists for underwater communications, where infrared optical links are heavily attenuated and radio-frequency or acoustic links are limited to low bandwidths and high latencies. A promising alternative is operation at visible wavelengths, where water is highly transparent.

In this work, we propose a silicon-photonics-based chip-scale solution to underwater communications that leverages visible-light liquid-crystal-based OPAs (Figure 1b) to enable electronic steering of high-speed data-modulated optical beams through water with lower loss. Using this visible-light liquid-crystal-based OPA, we demonstrate a 1-Gbps on-off-keying link and an electronically switchable point-to-multipoint link through water (Figure 1a). Such capabilities enable underwater applications, such as improved submarine communication capabilities and underwater antenna remoting.



▲ Figure 1: (a) Photograph of the experimental setup with the chip-based transmitter system on the left, water-filled tank, and a photodetector array on the right (inset showing photograph of photonic chip and probes). (b) Partial simplified top-view schematic of the integrated optical phased array highlighting major components.

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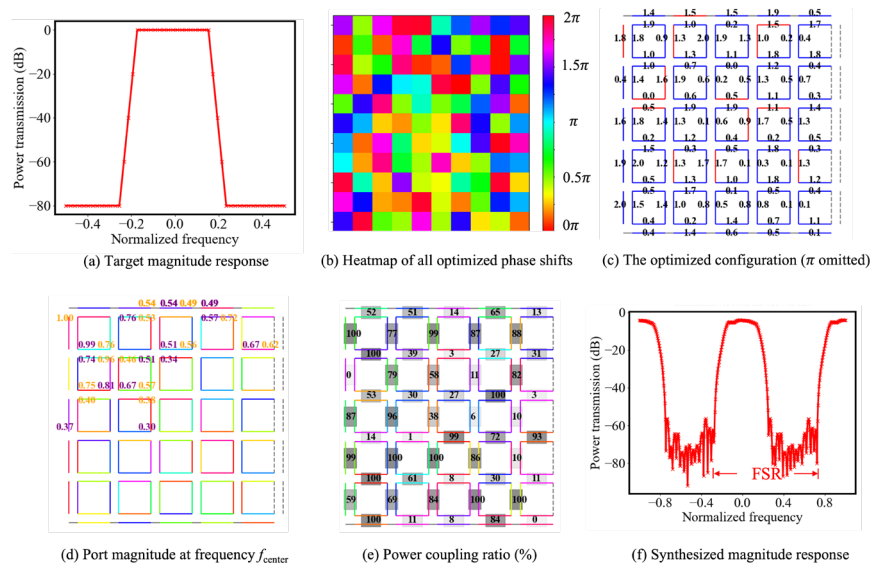
Automatic Realization of Light Processing Functions for Programmable Photonics

Z. Gao, Z. Zhang, U. Chakraborty, D. S. Boning
Collaborators: Xiangfeng Chen and Wim Bogaerts, Ghent University

Programmable integrated photonic circuits (PPICs) are an alternative paradigm to application-specific integrated photonics, exploiting run-time manipulation of light after a photonic chip is fabricated. Such reconfigurability is achieved by controlling active components (e.g., optical phase shifters) with electrical/thermal signals. Current published literature usually relies on hand-crafting to configure the PPIC so that certain light processing functions can be realized.

In this work, we have developed an automatic technique to implement light processing functions

on a recirculating square-mesh PPIC. At its heart is an automatic differentiation subroutine built upon analytical expressions of scattering matrices that enables gradient descent optimization for functional circuit synthesis. Our simulations demonstrate that our method can realize complex light processing functions in a matter of minutes and has the potential to work as a fundamental synthesis paradigm for programmable photonics.



▲ Figure 1: Synthesizing an optical filter on a 5-by-5 square programmable photonics mesh.

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Design of Quantum-dot Lasers using Plasmonic Nanocavities

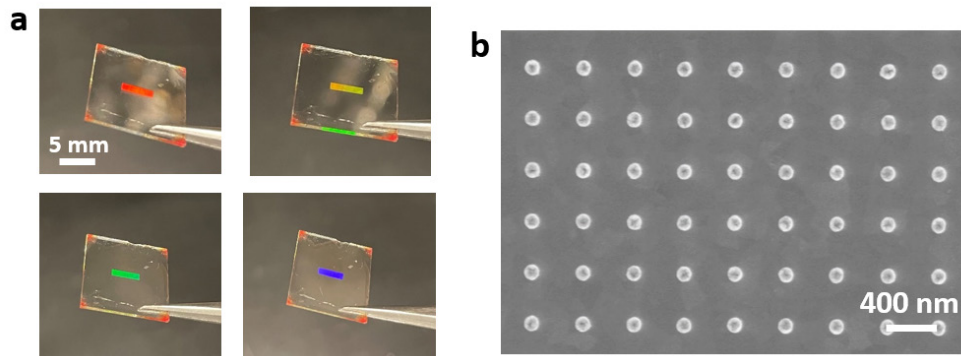
J. Guan, V. Bulović
Sponsorship: Samsung Electronics

Compact photonic structures are essential components in a variety of modern technologies, including high-speed optical communication, biochemical sensing, and quantum computing. The development of nanoscale lasers requires the advancement of efficient, nanoscale gain materials and the design of optical cavities. Colloidal quantum dots (QDs) represent promising gain materials for lasers because of their high photoluminescence quantum yields, tunable emission colors by particle size, and solution processibility. However, controlling the quantum lasing characteristics of QDs has been challenging, requiring the design of cavity structures.

Metal nanostructures offer a powerful platform for confining light into subwavelength volumes. When metal nanoparticles are arranged in an ordered array, surface lattice resonance (SLR) modes can be generated through the diffractive coupling of the nanoparticles. Our previous studies have integrated colloidal QDs with silver lattices, which resulted in QD lasing from the plasmonic cavities. In our laser structures, waveguide modes from the high-refractive-

index QD film can hybridize with the SLR modes from the lattice, resulting in a hybrid mode that provides optical feedback for QD lasing emission. Controlled radially and azimuthally polarized lasing has been demonstrated from the laser architecture. Moreover, the lasing emission angles can be manipulated by the lattice design.

Here, we designed QD-plasmon nanolasers by using indium phosphide QDs as gain media and two-dimensional aluminum lattices as optical cavities. We constructed nanolasers by spin-coating QD films on top of the aluminum nanoparticle lattices to ensure near-field coupling between the QDs and the plasmonic nanoparticles. Due to the high refractive index of the QD film, waveguide modes can form inside the QD film and hybridize with the plasmonic surface lattice resonances supported by the aluminum lattices, resulting in waveguide-plasmon modes as cavity modes. Our investigations into QD-plasmon interactions hold significant potential for the development of commercial QD laser devices and quantum-optical technologies.



▲ Figure 1: Design of QD-plasmon lasers. (a) A photo of the QD-plasmon laser device shows different diffracted colors at different view angles. (b) A scanning electron microscopy image of the plasmonic nanoparticle lattice.

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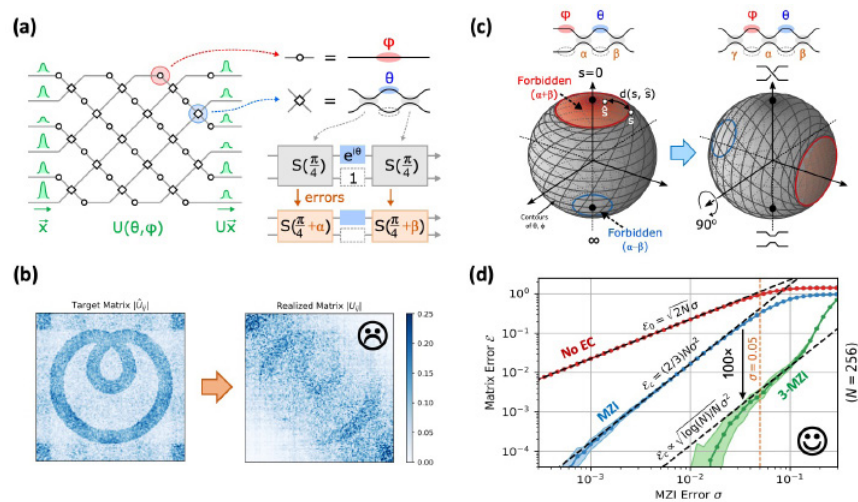
Asymptotically Fault-tolerant Programmable Photonics

R. Hamerly, S. Bandyopadhyay, S. K. Vadlamani, D. Englund

Sponsorship: NTT Research, Inc. (R.H.), NSF GRFP (S.B.), AFOSR No. FA9550-20-1-0113, FA9550-16-1-0391 (D.E.).

Photonics is a promising platform for special-purpose computing, but is only competitive when scaled up to large circuits. Unfortunately, component errors limit the scaling of programmable photonic devices. These errors arise because the standard tunable photonic coupler—the Mach-Zehnder interferometer (MZI)—cannot be perfectly programmed to the "cross" state. Here, we introduce two modified circuit architectures that overcome this limitation: (1) a 3-splitter MZI mesh for generic errors, and (2) a broadband MZI+Crossing

design for correlated errors. Because these designs allow for perfect realization of the cross state, the matrix fidelity no longer decreases with mesh size, allowing scaling to arbitrarily large meshes. The proposed architectures support progressive self-configuration, are more compact than previous MZI-doubling schemes, and do not require additional phase shifters. This eliminates a major obstacle to the development of very-large-scale photonic circuits.



▲ Figure 1: (a) 6x6 programmable photonic circuit. (b) Effect of component errors is to reduce circuit fidelity. (c) Proposed 3-MZI design, which shifts the "forbidden regions" away from the density peak. (d) Resulting 100x reduction in matrix error.

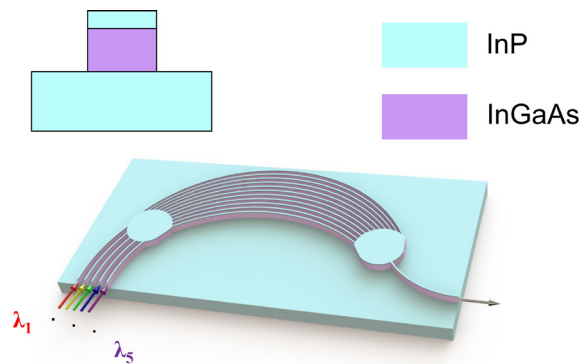
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High-efficiency Mid-infrared InGaAs/InP Arrayed Waveguide Gratings

T. S. Karnik, K. P. Dao, Q. Du, L. Diehl, C. Pflüegl, D. Vakshoori, J. Hu
Sponsorship: Naval Sea Systems Command (N68335-20-C-0845).

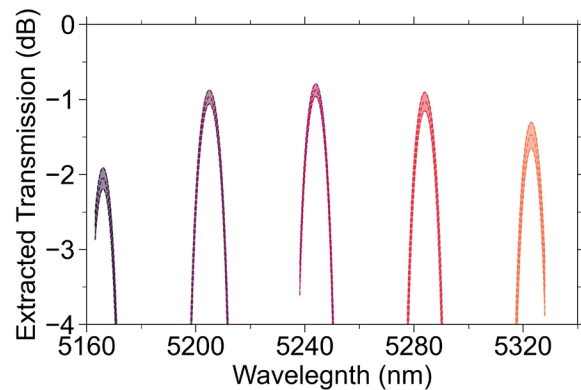
High-power infrared lasers are crucial for many applications, including infrared countermeasures and laser surgery. Quantum cascade lasers (QCLs) have emerged as an effective solution to produce coherent beams in the infrared regime operating at room temperature and spanning a wavelength range of 4-20 μm . While QCL design and materials processing improvements are essential for further increasing their output power, beam-combining offers a straightforward solution. Spatially overlapping laser beams from multiple sources can achieve power levels well beyond the capacity of a single emitter. However, free space beam-combining setups consist of bulky components covering a large footprint and are prone to beam misalignment due to vibrations, making them cumbersome for practical on-field application. Photonic integrated circuits (PICs) provide alternate on-chip components like arrayed waveguide gratings (AWGs) for wavelength beam combining (WBC), which can reduce the size and cost of such systems, offering a compact solution for fabricating high-power lasers. The current PICs rely on



▲ Figure 1: Schematic of a 5×1 AWG that can be used to wavelength-beam combine 5-element MWIR laser arrays. Waveguide cross section is depicted in the top left corner.

the heterogeneous integration of III-V semiconductor QCLs with AWGs made on silicon chips to realize a fully on-chip operation. However, the maximum laser power is limited due to the low thermal conductivity of silicon and the bonding material.

Hence, we focus on fabricating AWGs on the same III-V semiconductor platform used for QCLs and use InGaAs and InP as the waveguide core and cladding materials (Figure 1). The photonic chips are patterned using e-beam lithography and reactive ion etching. The low background doping levels and smooth waveguide sidewalls result in low propagation losses of 1.17 dB/cm. The AWG features 0.88 dB insertion loss and 0.6 dB non-uniformity, the lowest reported values in this wavelength range of 5.16-5.34 μm (Figure 2). Our work demonstrates a promising solution for the monolithic integration of AWGs (1.87 mm^2 footprint) with QCLs to achieve efficient WBC. The low-loss platform and fabrication technology developed is also equally applicable to other III-V-based PICs enabling new functionalities.



▲ Figure 2: AWG transmission vs. wavelength for all input channels.

FURTHER READING

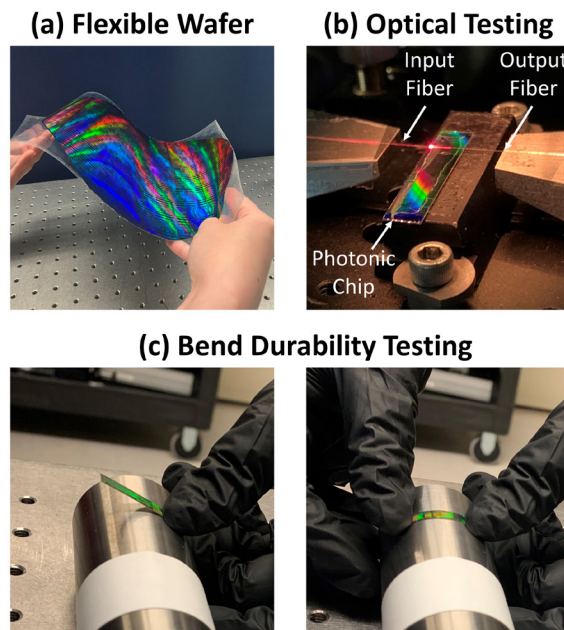
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Flexible Wafer-scale Silicon-photonics Fabrication Platform

M. Notaros, T. Dyer, A. Hattori, K. Fealey, S. Kruger, J. Notaros
Sponsorship: Defense Advanced Research Projects Agency VIPER program (Grant No. FA8650-17-1-7713)

The field of silicon photonics has advanced rapidly, enabled by advanced wafer-scale platforms and fabrication processes. However, these processes have been focused on fabrication on silicon substrates that result in rigid photonic wafers and chips, which restrict the possible application areas. There are many applications that would benefit from flexible photonic solutions, such as wearable healthcare monitors and pliable displays. However, prior demonstrations of flexible optical devices have been limited to die-scale fabrication, which is not easily scalable.

To address the need for scalable flexible photonics, in this work, we develop a wafer-scale CMOS-compatible platform and fabrication process that results in 300-mm-diameter flexible wafers. We experimentally demonstrate key functionality, including waveguide routing, passive devices, and bend durability. This work enables silicon photonics to delve into expanded applications, including healthcare monitors and pliable displays.



▲ Figure 1: Photographs of (a) a fabricated flexible silicon-photonics wafer, (b) a flexible photonic chip on the experimental setup, and (c) a flexible photonic chip undergoing bend durability testing.

FURTHER READING

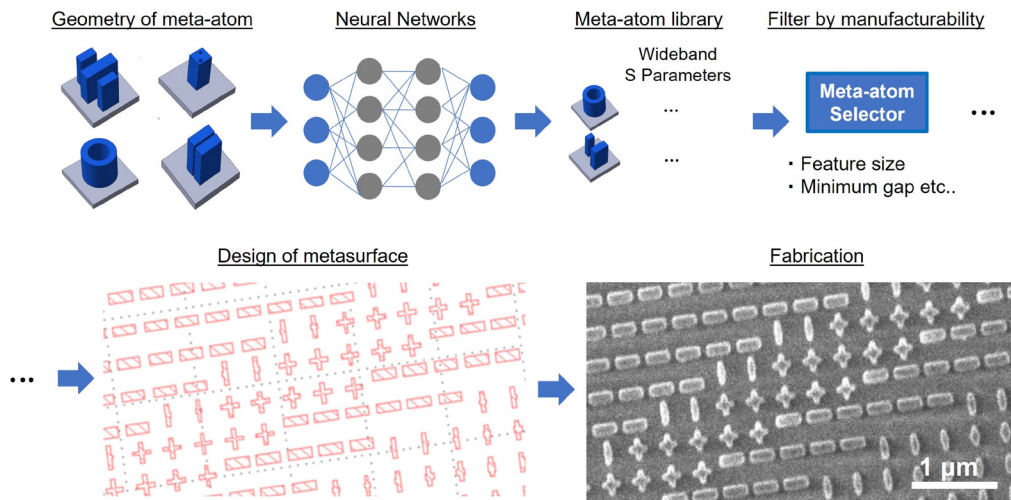
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Dual-band Optical Collimator Based on Deep-learning Designed, Fabrication-friendly Metasurfaces

A. Ueno, F. Yang, H. Lin, M. Y. Shalaginov, L. Martin-Monier, S. An, T. Gu, J. Hu
Sponsorship: AGC, Inc.

Metasurfaces, which are ultrathin planar optical structures, offer immense potential for use in high-performance optical devices through precise manipulation of electromagnetic waves with subwavelength spatial resolution. However, designing meta-atom structures that simultaneously meet multiple functional requirements (e.g., for multi-band or multi-angle operation) is an arduous task that poses a significant design burden. Therefore, it is essential to establish a robust method for producing intricate meta-atom structures as functional devices. To address this issue, we developed a rapid construction method for a multi-functional and fabrication-friendly meta-atom library using deep neural networks (DNNs) coupled with a meta-atom selector that accounts for realistic fabrication constraints.

The meta-atom library was generated using a predictive neural network (PNN) based on a convolutional neural network (CNN) architecture. The objective of the PNN is to predict the phase and amplitude responses of a given meta-atom design. In addition, our approach considers high depth-of-field (DOF) meta-atom structures and imposes fabrication constraints, such as pattern aspect ratio and minimum dimensions, to ensure manufacturability of the design. This processability-aware DNN-based method proposed is a fast and accurate modeling tool that provides a practical link between an extensive and sophisticated parametric space and the corresponding physical response and can be applied to realize innovative multi-functional optical devices.



▲ Figure 1: Concept of a fabrication-friendly metasurface design via processability-aware DNN-based method.

Optical Probes of Triplet Exciton Sensitization of Silicon

N. Wong*, C. F. Perkinson*, A. Q. Wu, W. A. Tisdale, M. G. Bawendi, M. A. Baldo
Sponsorship: DoE

With the climate changing, solar power is a major contender as a renewable energy resource. To match the growing global energy demand while meeting space and cost limitations, efficiencies of solar cells need to improve. However, the efficiencies of crystalline silicon solar cells, the current industry standard, are approaching the maximum theoretical limit. One method of going beyond this limit is to sensitize the silicon (Si) by using a material that can perform singlet exciton fission (SF), a carrier multiplication process that can create two triplet excitons (electron-hole pairs) from a single photon. Successful transfer of these two triplet excitons to silicon can result in increased photocurrent and improved efficiencies.

Recent work has shown coupling between Si and the archetype SF material tetracene (Tc) in the presence of passivating interfacial layers of Hafnium oxynitride [1]. Excitation spectra show a boost in the photoluminescence from Si when Tc is photoexcited that may be caused by energy transfer or changes in the

silicon passivation [1]. To experimentally distinguish between these phenomena and understand the complex dynamics of excited states and charges at silicon/SF interfaces, we have developed a spectroscopy technique that is robust to the weak and intensity-dependent photoluminescence from silicon. Using combinations of biasing optical pumps and selective modulation of SF rates using a magnetic field, we study structural variations at the interface to probe the mechanism of coupling at Hafnium oxynitride interfaces and other rationally-designed heterostructures. We demonstrate positive contributions from tetracene to silicon photoluminescence that suggest a key role for charge transfer states in realizing solar cell efficiency enhancements from singlet exciton fission. These results can help identify important material parameters for enhancing silicon solar cell efficiencies beyond the theoretical limit.

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Metasurface for 3-D Depth Sensing

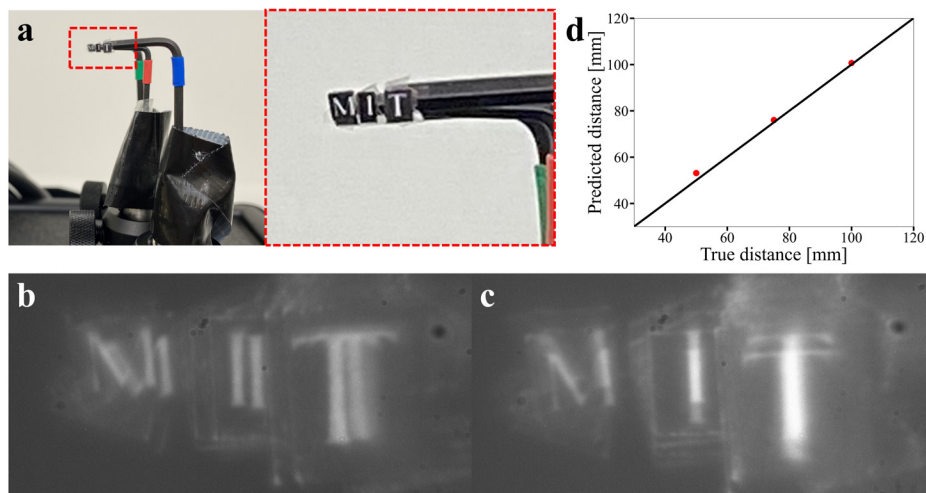
F. Yang, H. I. Lin, P. Chen, J. Hu, T. Gu
Sponsorship: DARPA, MIT Skoltech Seed Fund Program

Three-dimensional (3-D) depth sensing is a crucial requirement for many optical imaging applications. The passive depth sensing technique with double-helix (DH) point-spread-function (PSF) engineering shows high depth estimation precision, reduced power consumption, and system complexity compared to active depth sensing methods. We propose a novel polarization-multiplexed DH metalens design, which utilizes two DH PSFs with opposite rotation directions in the two polarization states to achieve depth sensing and scene reconstruction at the same time. The design exhibits optimal compactness, minimum distortion, and high resolution in all three dimensions.

The proposed metasurface design combines two phase profiles using polarization-multiplexing. It generates a DH PSF with two foci rotating as a function of point source distance in one polarization state and

another DH PSF rotating along the reversed direction in the orthogonal polarization state. Therefore, the depth information can be obtained through comparison of the images captured in the different polarization states.

The imaging and depth mapping demonstrations are shown in Figure 1, where we displace the letters “M,” “I,” and “T” printed on cardboards at different distances as shown in Figure 1(a). The images recorded in the two polarization states are shown in Figures 1(b) and (c), which are the convolution between the original pattern and the corresponding DH PSF. We then use a deconvolution algorithm to obtain both the original pattern and the underlying DH PSF. The extracted depths are shown in Figure 1(d), which agrees well with the ground truth.



▲ Figure 1: Experimental demonstration of depth sensing. (a) Photos of printed letters of “M,” “I,” and “T,” each placed at a different distance. (b, c) Captured images in (b) the x-polarization state and (c) the y-polarization state. (d) Inferred object distances (red dots) compared to the ground truth (solid line).

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Machine Learning and Other Accelerators

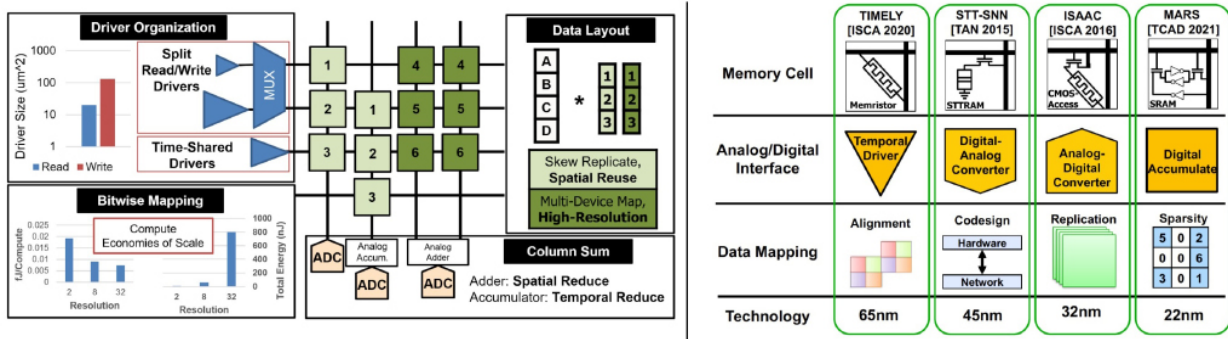
Architectural Evaluation of Processing-in-memory Accelerators.....	63
EfficientViT: Lightweight Multi-scale Attention for On-device Semantic Segmentation.....	64
AI-Row: A Real-time Mobile ML Analytics Application for Para- and Non-para Rowers.....	65
ADCs for Analog Neural Nets	66
A Fully-integrated Energy-scalable Transformer Accelerator Supporting Adaptive Model Configuration and Word Elimination for Language Understanding on Edge Devices	67
Unsupervised Time Series Anomaly Detection via Point/Sequential Reconstruction.....	68
Lego-like Reconfigurable Sensor Computing System.....	69
LEGO: Spatial Accelerator Generation and Optimization for Tensor Applications	70
On-device Training Under 256KB Memory	71
Efficient Camera-radar Fusion for 3D Perception	72
Neuromorphic Computing with Probabilistic Nanomagnets.....	73
CMOS-Compatible Ferroelectric Materials and Structures.....	74
Circular TLM Characteristics of WO ₃ for Protonic Programmable Resistors	75
Training Meta Neural Networks for Concept Drift Adaptation in Time Series.....	76
Algorithm and Hardware Co-design for Efficient Video Understanding on the Edge	77
Noise Resilience Deep Reconstruction for X-ray Tomography.....	78

Architectural Evaluation of Processing-in-Memory Accelerators

T. Andrulis, J. S. Emer, V. Sze
 Sponsorship: Ericsson, TSMC, MIT Artificial Intelligence Hardware Program

Processing-in-memory (PIM) accelerators are a promising approach to efficiently run deep neural networks (DNNs) as they move compute into memory and reduce high DNN data movement costs. Unfortunately, research has mainly focused on devices (e.g., memristors), circuits (e.g., analog converters), or architecture (e.g., dataflow) in isolation. It is desirable to see how innovation at any level, such as new devices, may change the efficiency and performance of whole accelerators. This would enable fair comparison of innovations and yield

insight into the vast number of ways to combine them. We present a framework that models PIM at an architectural level. With fast simulation and easy-to-change PIM device, circuit, and architecture models, our framework enables researchers to see how innovations affect the efficiency and performance of PIM accelerators. Further, we simulate up to 10,000x faster, enabling fast evaluation of different PIM accelerators and exploration of the vast design space.



▲ Figure 1: (Left) PIM analog crossbar design showing options in drivers/column sum (Circuit) and in data layout/bit mapping (Architecture) (Right) Previous works' design choices. The number of combinations is large and needs a rapid framework to explore.

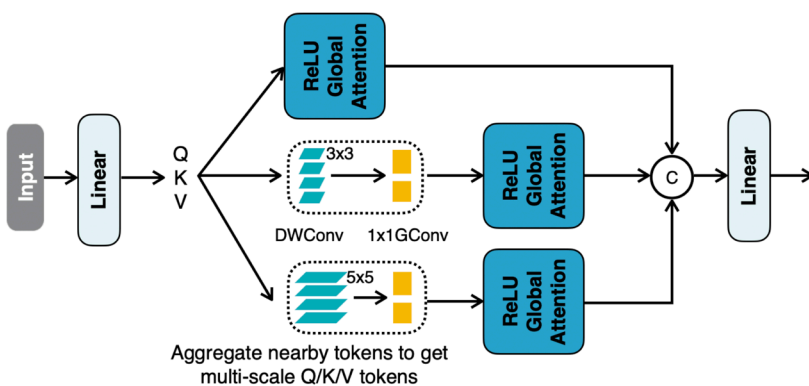
EfficientViT: Lightweight Multi-scale Attention for On-device Semantic Segmentation

H. Cai, J. Li, M. Hu, C. Gan, S. Han

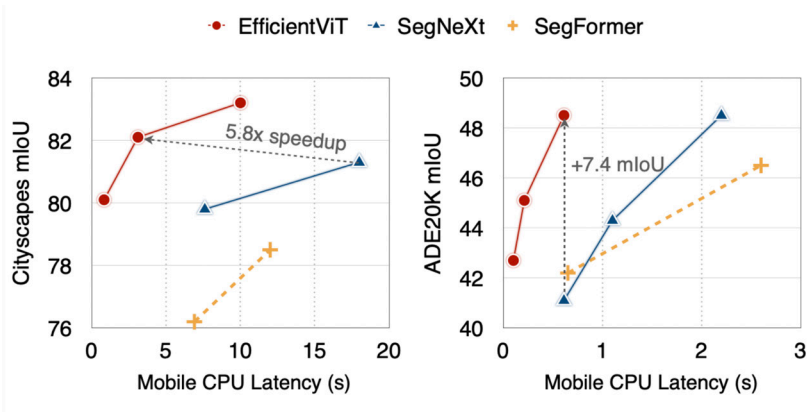
Sponsorship: NSF, MIT-IBM Watson AI Lab, Ford, Intel, Qualcomm

Semantic segmentation enables many appealing real-world applications, such as computational photography, autonomous driving, etc. However, the vast computational cost makes deploying state-of-the-art semantic segmentation models on edge devices with limited hardware resources difficult. This work presents EfficientViT, a new family of semantic segmentation models with a novel lightweight multi-scale attention for on-device semantic segmentation. Unlike prior semantic segmentation models that rely on heavy self-attention, hardware-inefficient large-kernel convolution, or complicated topology structure to obtain good performances, our lightweight multi-scale attention achieves a global receptive field and

multi-scale learning (two critical features for semantic segmentation models) with only lightweight and hardware-efficient operations. As such, EfficientViT delivers remarkable performance gains over previous state-of-the-art (SOTA) semantic segmentation models across popular benchmark datasets with significant speedup on the mobile platform. Without performance loss on Cityscapes, our EfficientViT provides up to 15x and 9.3x mobile latency reduction over SegFormer and SegNeXt, respectively. Maintaining the same mobile latency, EfficientViT provides +7.4 mIoU gain on ADE20K over SegNeXt.



► Figure 2: EfficientViT provides significant performance boosts compared with prior state-of-the-art semantic segmentation models.



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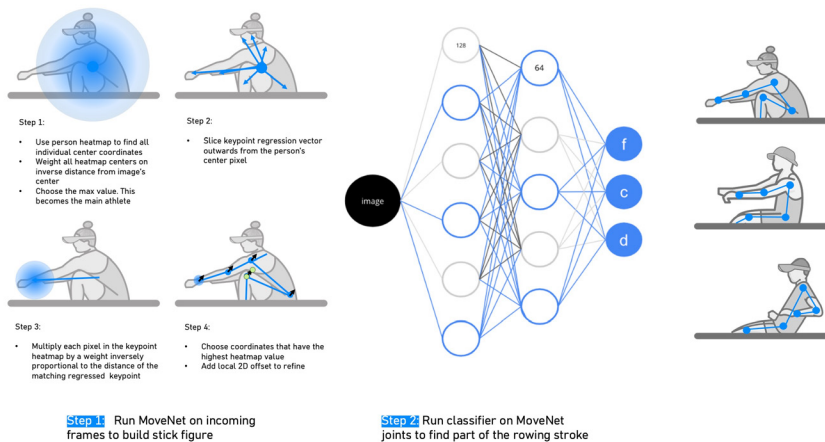
AI-Row: A Real-time Mobile ML Analytics Application for Para- and Non-para Rowers

E. Eldracher, V. Muriga, S. Rodríguez, Y. Lin, Z. Liu, S. Han

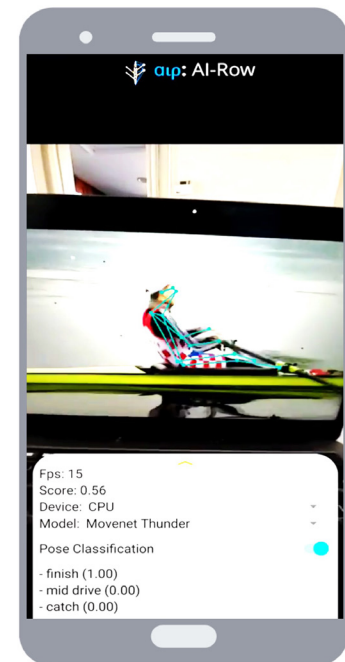
Lightweight machine learning (ML) models can learn how to deliver elite rowing coaching to anyone, regardless of that individual's skill or physical ability. Despite the sport's predictability and angle-based technique, few tools exist to deliver data analytics on performance. Those that do are often expensive, not frequently optimized for both on-the-water and ergometer video, and trained without para inclusivity. This work harnesses the power of artificial intelligence to deliver technical insights in real time on a mobile device. This mobile application is the first use of mobile pose estimation ML for para-optimized rowing. It works for all athletes: those who use only their arms, those who use their

arms and upper body, and those who use their legs, body, and arms.

By utilizing TensorFlow's MoveNet for mobile two-dimensional (2D) pose estimation combined with a simple classifier, we categorized three specific rowing poses both on the water and on the rowing machine. After locating an athlete's joints through MoveNet, our 26kb classifier predicts what part of the stroke a rower is in. At 18 frames/second, this classifier achieves around 89% accuracy. Because we built our own dataset of images (935 training, 235 testing, YouTube and USRowing images), this model is diverse and inclusive of both para and non-para athletes.



▲ Figure 1: Rendering of how our model predicts parts of the rowing stroke. Step 1 demonstrates MoveNet, Step 2 details our classifier, and the right-most side shows the three potential rowing positions categorized.



▲ Figure 2: Real-time screen recording of AI-Row. An android device correctly classifies a rower in the layback finish position.

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ADCs for Analog Neural Nets

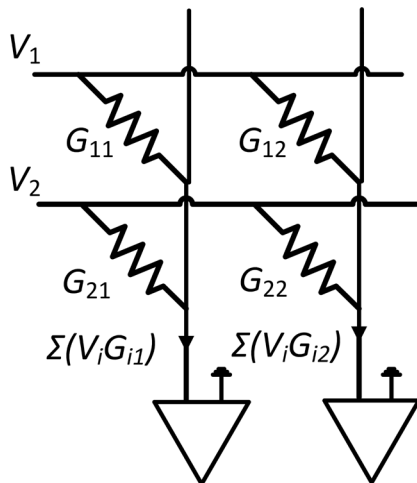
M. A. G. Elsheikh, H.-S. Lee

Sponsorship: MIT/MTL Samsung Semiconductor Research Fund

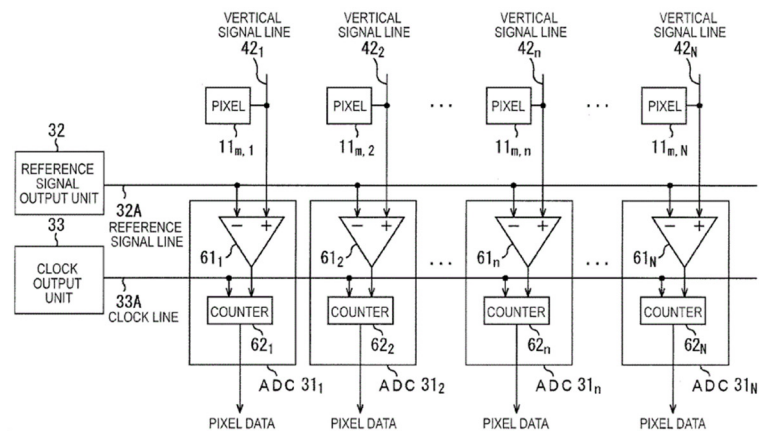
The meteoric rise of neural networks in recent years has been fueled by applications in several domains such as image recognition, self-driving cars, signal processing, and drug discovery. For more widespread deployment in portable applications, speed and power consumption must be improved. Employing specialized accelerator architectures offers improvements on both fronts. One accelerator topology, analog neural networks (ANNs), shown in Figure 1, perform matrix-vector-multiplications (MVMs) in the analog domain by encoding the inputs as the voltages and the weights as conductances. Summing up the currents in a common, virtual ground node is equivalent to performing the MVM process in one cycle, thereby potentially saving energy and time.

An analog-to-digital converter (ADC) architecture that is proposed for this application is the single slope ADC (SS-ADC), shown in Figure 2. The SS-ADC has become the standard architecture for complementary

metal-oxide semiconductor (CMOS) image sensors as it is suitable for a medium number of bits, it is highly reconfigurable, and the peripheral circuits can fit the column pitch of the sensor elements. The column-parallel SS-ADC consists of a comparator and a counter for each column and a central ramp generator. At the beginning of the quantization process, the ramp and the counter are reset. The ramp starts increasing as the counter starts incrementing, and each column comparator compares between its analog column voltage and the ramp voltage. When the ramp value exceeds the column value, the comparator trips, and the counter value is held. This value is the digital representation of the column signal. In this research several innovations can be introduced to the SS-ADC to tailor it for ANNs to improve them beyond the state of the art in terms of speed and power consumption.



▲ Figure 1: Analog neural network accelerator.



▲ Figure 2: The column parallel architecture SS-ADC.

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A Fully-integrated Energy-scalable Transformer Accelerator Supporting Adaptive Model Configuration and Word Elimination for Language Understanding on Edge Devices

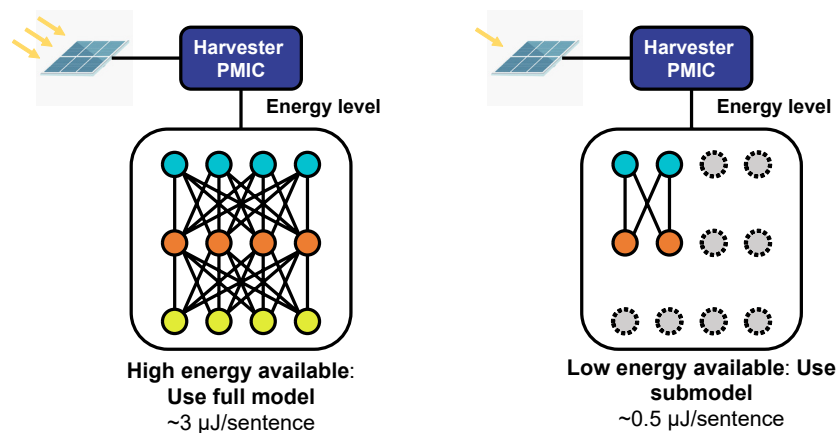
A. Ji, H. Wang, M. Wang, S. Han, A. P. Chandrakasan
Sponsorship: TSMC

Efficient natural language processing (NLP) on the edge is needed to interpret voice commands, which have become an increasingly common way to interact with devices around us. Attention-based transformer models have replaced recurrent neural networks as the predominant model for NLP applications due to parallel input processing and the attention mechanism being able to capture both short and long-range relations. However, existing mainstream models (e.g., BERT, GPT) are way too large for edge devices. For simple NLP tasks on the edge, tiny custom transformer models can achieve good accuracy while being much more suitable for constrained hardware.

There are two main challenges when deploying lightweight NLP models on edge devices. Firstly, hardware constraints can fluctuate based on battery level, latency requirements, availability of compute resources, and accuracy tolerance. Adapting to these conditions typically requires multiple models of different sizes. For instance, when the device is less constrained, we may use a large model while under

more constrained conditions, we may opt for a small model. But storing multiple models incurs a significant memory overhead. Secondly, sentences usually contain redundant words that contribute little to the overall understanding and may potentially be skipped during the majority of the processing. Conventional models spend an equal amount of time processing each word, leading to unnecessary computation.

Our work addresses these challenges with an energy-scalable transformer accelerator targeting small Internet of Things devices with two key features: 1) adaptive model configuration using a custom SuperTransformer model to generate models of various sizes while taking up only the memory footprint of a single full model; and 2) a comparator-based word elimination unit to progressively remove unimportant words from the sentence, reducing computation. We achieve 5.8× scalability in the network energy and latency. Word elimination can reduce network energy by 16% with some accuracy loss.



▲ Figure 1: Adaptive model configuration based on energy level of energy harvester using a single SuperTransformer model.

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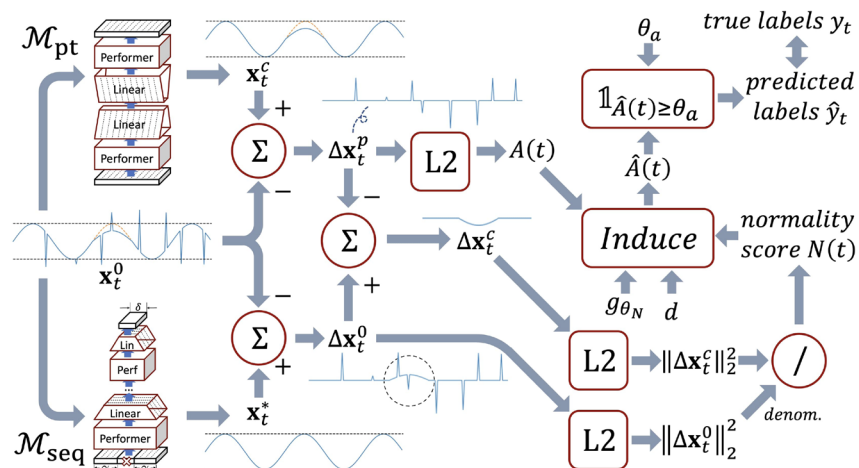
Unsupervised Time Series Anomaly Detection via Point/Sequential Reconstruction

C.-Y. Lai, F.-K. Sun, Z. Gao, J. H. Lang, D. S. Boning
Sponsorship: Turntide Technologies

Fortune Global 500 manufacturing and industrial firms lose around 3.3 million hours of production time due to machine failure, resulting in an economic impact of \$864 billion of their annual revenue. By identifying anomalies in time series data for manufacturing and operations, one can reduce downtime and prevent financial setbacks. However, time series anomaly detection is challenging due to the complexity and variety of patterns that can occur. One major difficulty arises from modeling time-dependent relationships to find contextual anomalies while maintaining detection accuracy for point anomalies.

In this work, we propose a novel framework--normality score conditioned time series anomaly detection by point/sequential reconstruction (NPSR)--for unsupervised time series anomaly detection that utilizes point-based and sequence-based reconstruction models. The general scheme is shown in Figure 1. The point-based model attempts

to quantify point anomalies, and the sequence-based model attempts to quantify both point and contextual anomalies. Under the formulation that the observed time point is a two-stage deviated value from a nominal time point, we introduce a normality score calculated from the ratio of a combined value of the reconstruction errors. We derive an induced anomaly score by further integrating the normality score and anomaly score, and then theoretically prove the superiority of the induced anomaly score over the original anomaly score under certain conditions. Extensive studies conducted on several public datasets show that the proposed framework outperforms most state-of-the-art baselines for time series anomaly detection. It also possesses the potential to decrease labor needs for fault monitoring and correspondingly accelerate decision making and can contribute to artificial intelligence (AI) sustainability by preventing energy waste or system failure.



▲ Figure 1: General scheme for NPSR.

FURTHER READING

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Lego-like Reconfigurable Sensor Computing System

G. Lee, C. Choi, H. Kim, J.-H. Kang, M.-K. Song, H. Leon, J. Kim

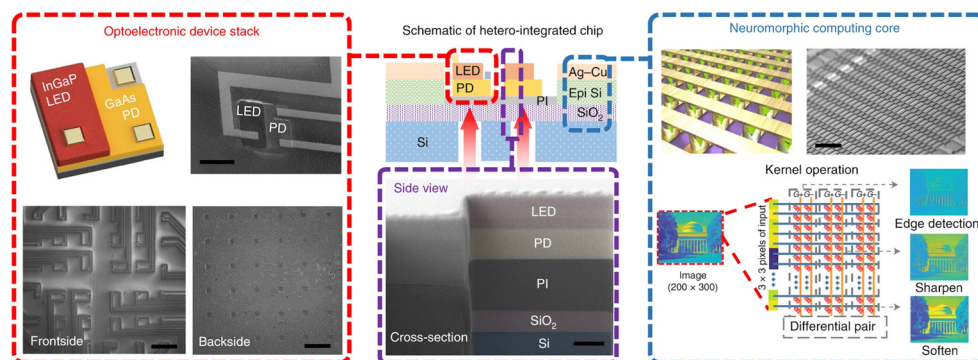
Sponsorship: Ministry of Trade, Industry, and Energy, Korea Institute of Science and Technology, Samsung Global Research Outreach Program

The emergence of artificial intelligence applications has transformed computer design, leading to a quest for hardware architecture that can process large volumes of data with high power, area, and time efficiency. To improve data communication bandwidth among sensors, memory, and processors, three-dimensional (3D) heterogeneous integration combined with advanced packaging technologies is a promising solution. However, these systems have limitations such as a lack of hardware reconfigurability and reliance on conventional von Neumann architecture.

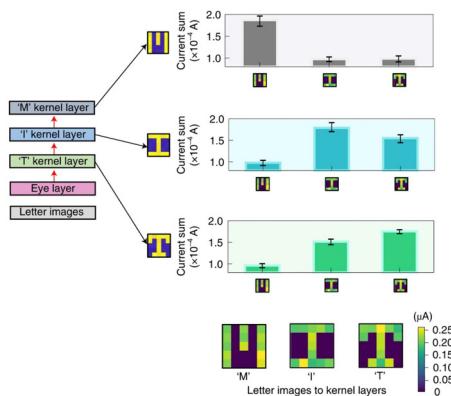
In this project, we address these issues by introducing stackable heater-integrated chips that employ optoelectronic device arrays for inter-chip communication and neuromorphic cores built with memristor crossbar arrays for parallel data processing

(Figure 1). With these stackable and replaceable chips, we created a system that can directly classify information from a light-based image source. First, we showed that three different preprogrammed neuromorphic core layers can be stacked and share the light inputs, illustrating the robustness of light-signal-based communication (Figure 2). Further, we showed that an additional noise reduction layer inserted after the sensor layer successfully improves the letter recognition performance in a noisy environment (Figure 3).

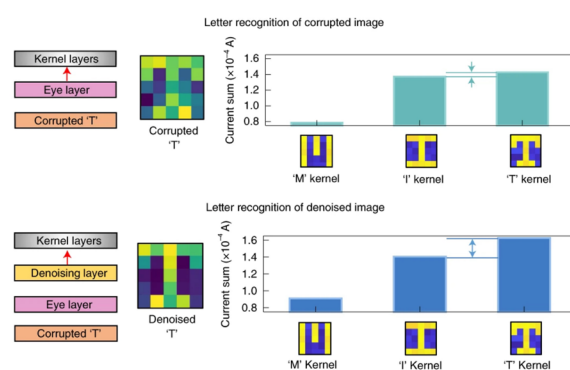
This project provides a reconfigurable 3D hetero-integrated platform that enables vertical stacking of various functional layers. This could provide an energy-efficient data communication and processing solution to sensor computing or edge computing applications.



◀ Figure 1: Stackable hetero-integrated neuromorphic chips.



▲ Figure 2: Robust kernel operation of stackable heater-integrated neuromorphic chips.



▲ Figure 3: Noise reduction using additional layer.

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LEGO: Spatial Accelerator Generation and Optimization for Tensor Applications

Y. Lin, Z. Zhang, S. Han
Sponsorship: SRC

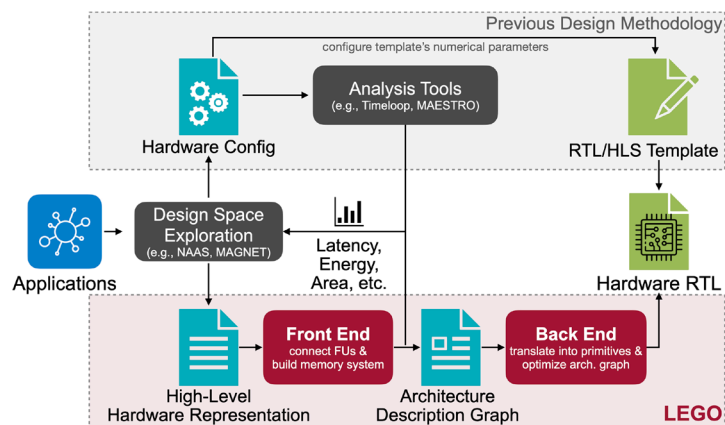
The proliferation of tensor applications, such as deep neural networks, has led to an unprecedented demand for efficient and high-performing solutions. Particularly, modern foundation models and generative artificial intelligence (AI) applications require multiple input modalities (both vision and language), which increases the demand for flexible accelerator architecture. Existing frameworks suffer from the trade-off between design flexibility and productivity of register transfer language (RTL) generation: either limited to very few hand-written templates or unable to automatically generate the RTL.

To address this challenge, we propose the LEGO framework, which automatically generates and optimizes spatial architecture design in the front end and outputs synthesizable RTL code in the back end without RTL templates. LEGO front end finds all possible interconnections between function

units and determines the memory system shape by solving the integer linear equations and establishes the connections by a minimum-spanning-tree-based algorithm and a breadth-first-search-based heuristic algorithm for merging different spatial dataflow designs.

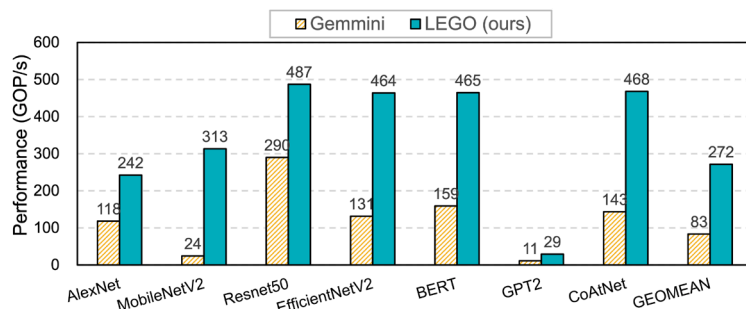
LEGO back end then translates the hardware in a primitive-level graph to perform lower-level optimizations and applies a set of linear-programming algorithms to optimally insert pipeline registers and reduce the overhead of unused logic when switching spatial dataflows.

Our evaluation demonstrates that LEGO can achieve $3.3\times$ speedup and $2.1\times$ energy efficiency compared to previous work by Gemini and can generate one architecture for diverse modern foundation models in generative AI applications.



◀ Figure 1: Instead of configuring the sizing parameters in the hardware template, LEGO directly generates spatial architecture design and outputs RTL code from high-level hardware description.

▶ Figure 2: Performance comparison of Gemini and LEGO. LEGO achieved an average $3.3\times$ speedup over Gemini. Both Gemini and LEGO are bounded by memory bandwidth on GPT2. LEGO performs much better on MobileNetV2 due to its efficient support of depthwise convolution by dataflow switching.



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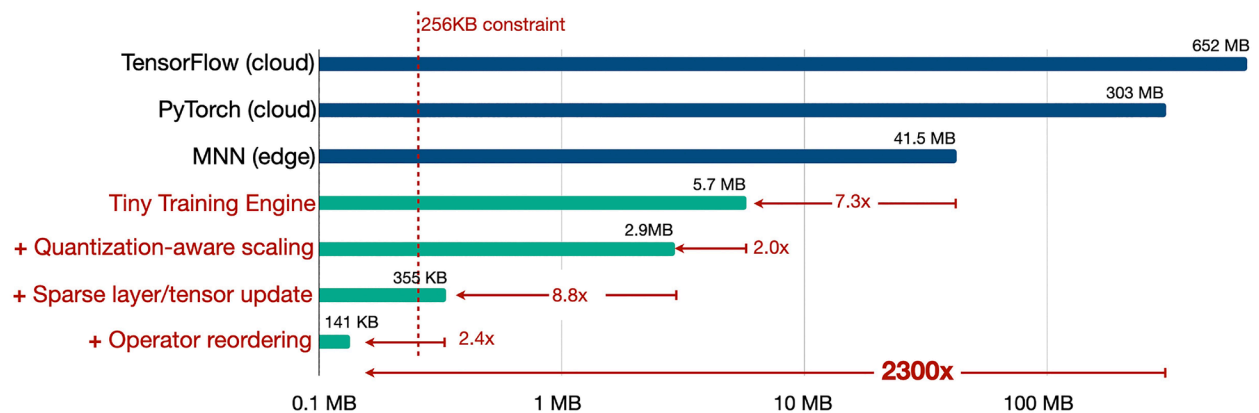
On-device Training Under 256KB Memory

J. Lin, L. Zhu, W. M. Chen, W. C. Wang, C. Gan, S. Han

Sponsorship: NSF, MIT-IBM Watson AI Lab, MIT AI Hardware Program, Amazon, Intel, Qualcomm, Ford, Google

On-device training enables the model to adapt to new data collected from the sensors by fine-tuning a pre-trained model. Users can benefit from customized artificial intelligence (AI) models without having to transfer the data to the cloud, protecting privacy. However, the training memory consumption is prohibitive for Internet of Things (IoT) devices that have tiny memory resources. We propose an algorithm-system co-design framework to make on-device training possible with only 256KB of memory. On-device training faces two unique challenges: (1) the quantized graphs of neural networks are hard to optimize due to low bit-precision and the lack of normalization, and (2) the limited hardware resource does not allow full back-propagation. To cope with the optimization difficulty, we propose quantization-aware scaling to calibrate the gradient scales

and stabilize 8-bit quantized training. To reduce the memory footprint, we propose sparse update to skip the gradient computation of less important layers and sub-tensors. The algorithm innovation is implemented by a lightweight training system, Tiny Training Engine, which prunes the backward computation graph to support sparse updates and offload the runtime auto-differentiation to compile time. Our framework is the first solution to enable tiny on-device training of convolutional neural networks under 256KB static random-access memory (SRAM) and 1MB Flash without auxiliary memory, using less than 1/1000 of the memory of PyTorch and TensorFlow while matching the accuracy on tinyML application VWW. Our study enables IoT devices not only to perform inference but also to continuously adapt to new data for on-device lifelong learning.



▲ Figure 1: Algorithm and system co-design reduces the training memory from 303MB (PyTorch) to 141KB with the same transfer learning accuracy, leading to 2300× reduction.

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Efficient Camera-radar Fusion for 3D Perception

Z. Liu, H. Tang, K. Shao, X. Chen, S. Han

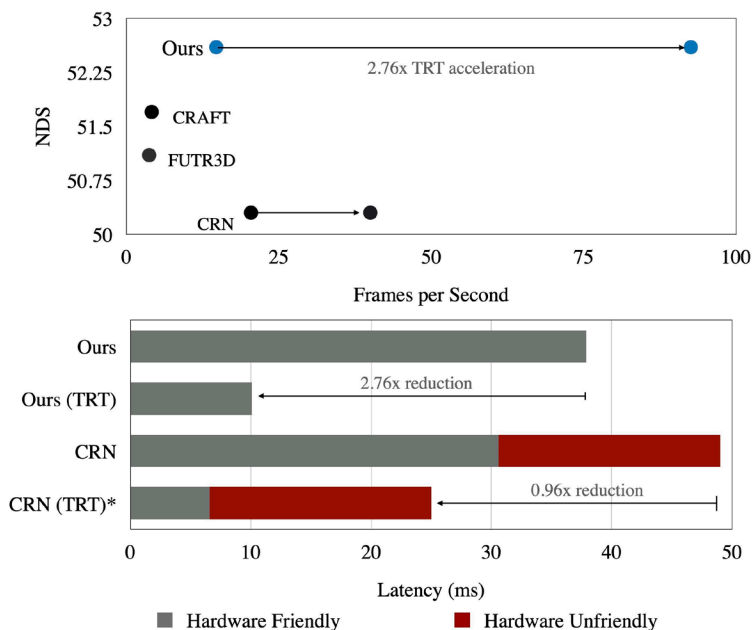
Sponsors: National Science Foundation, Hyundai Motor, Qualcomm, NVIDIA, Apple

The development of three-dimensional (3D) perception systems is crucial to the widespread adoption of autonomous driving. However, many studies tend to overlook practical considerations, resulting in relatively little focus on the efficient and sensible deployment of 3D perception models in the real world. A successful practical deployment requires consideration of several factors simultaneously, such as accuracy, speed, cost, and deployability. Given the high cost of light detection and ranging (LiDAR) sensors compared to cameras or radars, we propose an efficient camera-radar fusion approach for 3D perception.

Various studies have explored the question of how to fuse information from different modalities (see Figure 1). In our approach, we propose performing the fusion in bird's eye view (BEV) space, as it retains semantic and spatial information from each modality. We apply a modality-specific encoder to each input,

followed by the BEV projection and a two-dimensional (2D) decoder. To further improve the model, we designed a novel view transformer module that is responsible for transforming image features from the camera view to 3D space. By fusing radar points onto the image plane, our model is capable of more accurate depth estimation, leading to better spatial alignment and improved performance. Additionally, we modify previous architectures by ensuring that all operations in our model are capable of hardware acceleration.

Our architecture design results in a camera-radar fusion model that improves on the previous state-of-the-art single-frame models. Our model achieves 52.6% NDS on the nuScenes detection dataset. Moreover, our model can leverage TensorRT acceleration to achieve a much greater speedup than competing methods (see Figure 2). Ultimately, our model achieves real-time latencies on NVIDIA Jetson AGX Orin.



◀ Figure 1: Visualization of radar points projected onto corresponding image. A principal challenge of utilizing radar data is its sparsity, as plainly seen here. However, radar returns also carry semantically useful information, such as radar cross section and radial velocity, which are helpful for 3D object detection models.

◀ Figure 2: Comparison between our models and previous camera radar fusion methods. Due to our design, our model can better leverage hardware acceleration to achieve stronger accuracy at faster speeds than CRN, the currently leading approach.

FURTHER READING

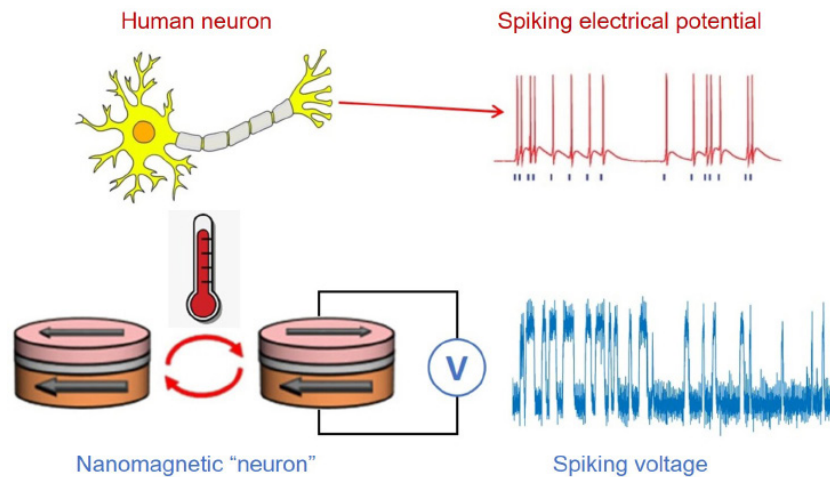
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Neuromorphic Computing with Probabilistic Nanomagnets

B. C. McGoldrick, M. A. Baldo, L. Liu
Sponsorship: EECS Mathworks Fellowship

The human brain is capable of performing complex tasks such as object recognition and inference, all while operating at low power. In contrast, performing the same tasks on digital computers requires significant energy, time, and hardware. While the brain exhibits random, noisy behavior, digital computers are designed oppositely to be deterministic and low-noise. By emulating the brain's probabilistic nature in hardware, we can potentially achieve superior speed and energy-efficiency on solving the aforementioned problems. We

develop a probabilistic bit (p-bit) based on a nanomagnetic device that produces a random bipolar voltage signal driven by ambient thermal noise. We can control the p-bit's probability and fluctuation rate by applying magnetic fields or charge currents. Finally, we elucidate a plan to integrate our tunable p-bits with traditional CMOS circuits to realize a probabilistic inference system with potentially greater speed and energy efficiency than existing approaches.



▲ Figure 1: Nanomagnetic “neuron” that converts ambient thermal fluctuations at room temperature to a random, fluctuating bipolar voltage signal. This behavior can be likened to the random spiking behavior of a neuron in the human brain.

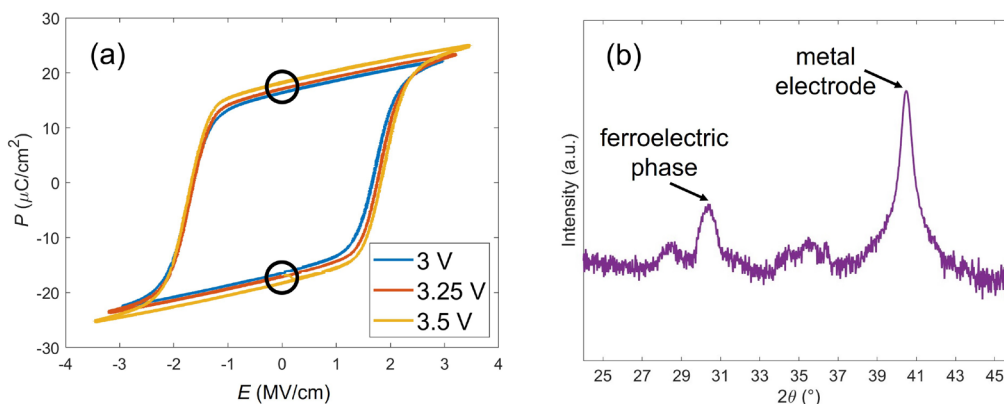
CMOS-Compatible Ferroelectric Materials and Structures

E. Rafie Borujeny, Y. Shao, T. Kim, J. A. del Alamo
Sponsorship: MIT Quest for Intelligence, SRC

Ferroelectrics are a class of materials that exhibit a nonlinear relationship between the externally applied electric field (E) and the electric polarization (P) formed inside them. In addition, they show a spontaneous non-zero polarization even when no external E is applied (Figure 1a). Moreover, the value of P in ferroelectric materials depends not only on the value of E but also on its history (for example, note in Figure 1 that at $E=0$, P can have two values depending on whether we reach $E=0$ from $E>0$ or from $E<0$). Having a spontaneous and history-dependent polarization means that ferroelectric materials can be incorporated into electronic devices to act as non-volatile memory elements.

Our research focuses on high-quality complementary metal-oxide semiconductor- (CMOS) compatible ferroelectrics that can be incorporated into nanometer-scale electronic devices. We specifically focus on developing ferroelectric structures based on

hafnium zirconium oxide (HZO) thin (~ 10 nm) films fabricated at low temperature (at or below 400°C). We investigate how process variations influence the composition, structure and electrical behavior of these films. We also investigate how the presence of other materials in contact with these ferroelectrics, as it occurs in real-world electronic devices, influences their performance. As a result of these investigations, we have successfully developed high-quality HZO films that contain the desired ferroelectric crystalline phase responsible for the ferroelectric properties (Figure 1b) and show clear and symmetric polarization-voltage characteristics even when the fabrication process temperature is limited to 400°C (Figure 1a). These investigations pave the way for the incorporation of ferroelectric materials into standard CMOS technology to enhance the functionality and performance of future electronics.



▲ Figure 1: (a) Relationship between P and applied E in a ferroelectric HZO film annealed at 400°C -- note the hollow circles that show two values of P at $E=0$; (b) X-ray diffraction pattern of the corresponding film depicting the presence of the desired orthorhombic ferroelectric structure inside the film.

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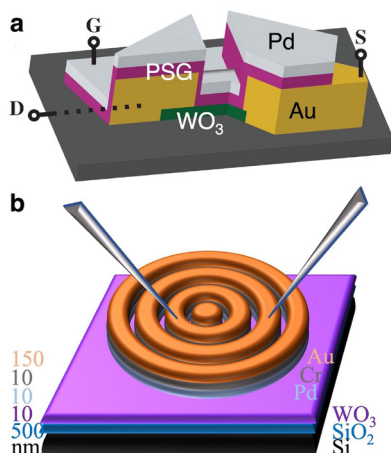
Circular TLM Characteristics of WO₃ for Protonic Programmable Resistors

D. Shen, J. A. del Alamo
Sponsorship: MIT-IBM Watson AI Lab

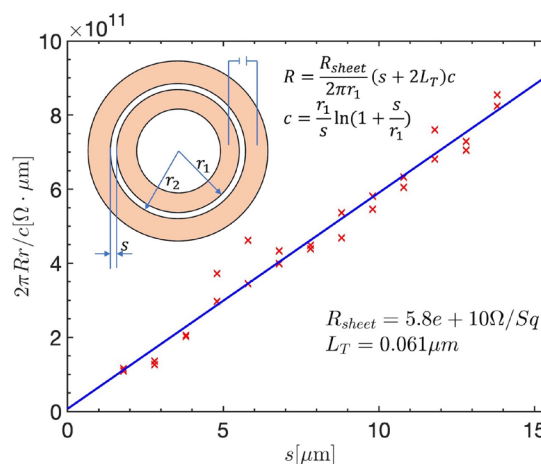
Analog computing offers a potential solution for overcoming computational bottlenecks in traditional digital systems utilized for deep learning. The fundamental concept of analog deep learning accelerators involves processing information locally by leveraging the physical properties of devices, rather than conventional Boolean arithmetic—specifically, using Ohm's and Kirchhoff's laws for matrix inner product calculations and threshold-based updating for the outer product. Among various physical principles, electrochemical ion-intercalation makes possible a three-terminal device with a channel resistance that is modulated by ionic exchange between the channel and a gate reservoir via an electrolyte. This study focuses on such ionic programmable resistors featuring WO₃ as the channel and protons as the ions, aiming to provide information processing with increased energy savings, efficiency, non-volatility, and low latency. Our group's previous work, with a device structure shown in Figure 1a, has demonstrated silicon-compatible nanoscale devices that are 1,000x smaller than biological neurons, en-

abling channel conductance modulation of an over 20x range with nanosecond operation at room temperature.

To further examine the properties of WO₃ as the channel material and efficiently understand the impact of different fabrication process conditions, we have developed a straightforward and effective test structure, depicted in Figure 1b. The test structure employs the conventional circular transfer length method (TLM) to measure sheet resistance and contact resistance via linear fitting of resistance data collected from a series of devices, as shown in Figure 2. By obtaining resistance information before, during, or after protonation, we gleaned valuable WO₃ characteristics—such as a 104x conductance modulation range, low proton diffusion coefficient, and high resistance recovery ability under heating. Additionally, we will compare different protonation methods such as metal diffusion method with Pd and hydrogen spillover method with HCl. These insights help us optimize the fabrication process for improved programmable resistors.



▲ Figure 1: WO₃ protonic device structures: (a) Three-dimensional illustration of the device studied in our previous work, WO₃ as channel, nano-porous phosphosilicate glass (PSG) as the electrolyte, and Pd as hydrogen reservoir and controlling gate. (b) Circular TLM structure for rapid test, Pd absorbing hydrogen and shuttling protons.



▲ Figure 2: Typical circular TLM fitting demonstration. The inset shows the parameters of concentric metal rings and the near-linear relation between cross-ring resistance and gap-spacing. Main figure shows results for WO₃ deposited with 90W RF sputtering and 400°C annealing, with r₁ = 100 μm and s ranging from 1.8 μm to 13.8 μm.

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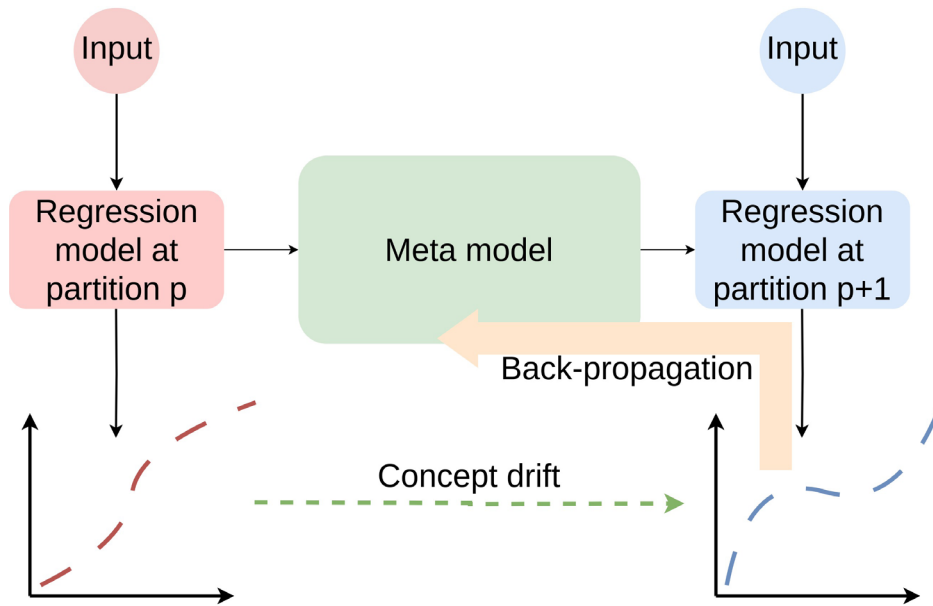
Training Meta Neural Networks for Concept Drift Adaptation in Time Series

F.-K. Sun, D. S. Boning
Sponsorship: Lam Research

Time series analysis and modeling play crucial roles in various applications such as forecasting and anomaly detection. However, one common challenge is the occurrence of concept drift, where the dynamics of the underlying system change over time due to factors like wear, tear, and environmental variations. Dealing with concept drift typically involves retraining the model whenever new data points are observed, but this process can be time-consuming and computationally intensive.

To better understand the impact of concept drift, we start by synthesizing a multivariate linear dataset with linear drift and training a regression model using it. We divide the dataset into 10 sets, training the regression model up to the p -th set and evaluating its performance on the subsequent $(p+1)$ -th set. As expected, we observe a degradation in the model's performance over time.

To address this issue, we propose a solution in the form of a "meta model" designed to learn and predict the drift dynamics of the regression models. The underlying assumption is that the drift dynamics are predictable. The "meta model" takes the p -th regression model as input and predicts the $(p+1)$ -th regression model. Notably, we have also developed a technique enabling end-to-end training of the meta model. Consequently, even if the regression model is trained on data only up to the p -th set, we can utilize the meta model to predict the $(p+1)$ -th model and evaluate it on the corresponding $(p+1)$ -th set of data. This approach is valuable in real-world scenarios where we want to assess new batches of data but possess only an "outdated" model. Our experimental results demonstrate that the meta model effectively learns the drift dynamics, resulting in a performance degradation reduction ranging from 2x to 10x compared to not adapting to the drift.



▲ Figure 1: The algorithm flow of training the meta model. Notably, the gradient back-propagation is directly propagated from the output to the meta model, enabling an end-to-end training approach.

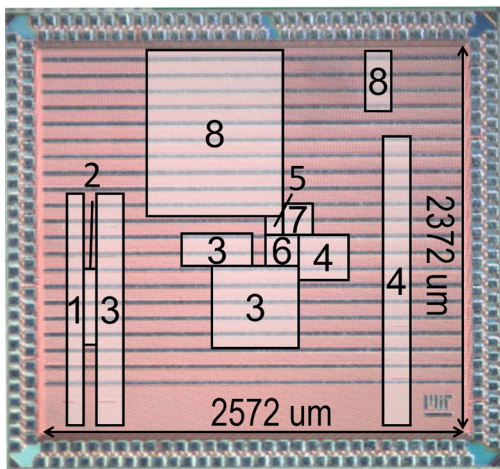
Algorithm and Hardware Co-design for Efficient Video Understanding on the Edge

M. Wang, Y. Lin, Z. Zhang, J. Lin, S. Han, A. P. Chandrakasan
Sponsorship: Qualcomm Incorporated, TSMC University Shuttle Plan

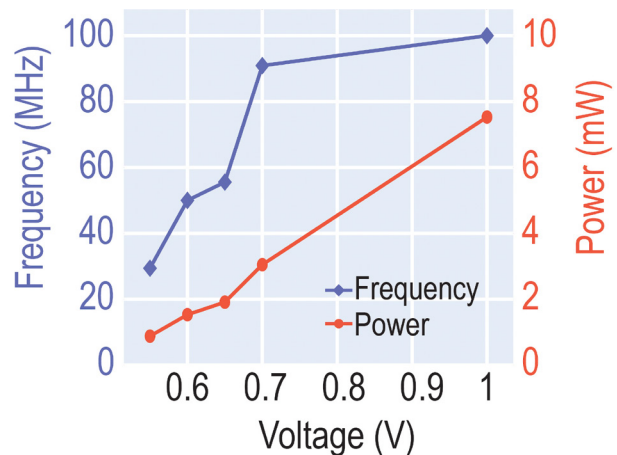
With the rise of various applications including augmented reality/virtual reality, autonomous driving, object tracking for unmanned aerial vehicles, etc., there is an increasing need for accurate and energy-efficient video understanding on the edge. Although many deep learning chips are designed for images, little work has been done for videos. Video understanding on the edge has three major challenges. First, video understanding requires temporal modeling. For example, it identifies the difference between opening and closing a box, which is distinguishable only with temporal information considered. Second, many applications are delay-critical, such as self-driving cars and artificial intelligence drones. Third, high energy efficiency is important for edge devices with a tight power budget. Due to temporal continuity, consecutive frames might share a lot of common information, providing the potential to improve processing efficiency. However, an image-based processing system cannot utilize that since each frame is processed individually.

In this project, we co-design algorithms and hardware for energy-efficient video processing for

delay-critical applications. We propose a real-time DiffFrame convolution achieving 2.2x dynamic random-access memory (DRAM) access reduction compared to conventional convolution at single-frame latency, design a sorter-free architecture for efficient utilization of temporal similarities between video frames, enable temporal modeling capability achieving high accuracy on video understanding applications, and optimize data buffering to remove DRAM traffic overhead for temporal modeling and reduce 55%-79% input activation DRAM traffic in depth-wise convolution layers. The chip consumes 40uJ/frame with 38 frames/second at 0.6V in 28nm TSMC 28-nm complementary metal-oxide-semiconductor (CMOS) process. Figure 1 shows the chip photograph; Figure 2 presents the frequency and power measurement results. Our demonstration of ferroelectricity in stacking-engineered TMD bilayers consolidates the feasibility of engineering 2D ferroelectric semiconductors and opens up a broad way of engineering various functional heterostructures out of non-ferroelectrics.



▲ Figure 1: Die micrograph (1: 16kB weight buffer; 2: 8x8 multiplier-and-accumulator array; 3: 32kB input activation buffer; 4: 44kB output activation and RefFrame unit; 5: DiffFrame generator; 6: DiffFrame pruning; 7: ConvMap buffer; 8: convolution map generator & coordinate buffer).



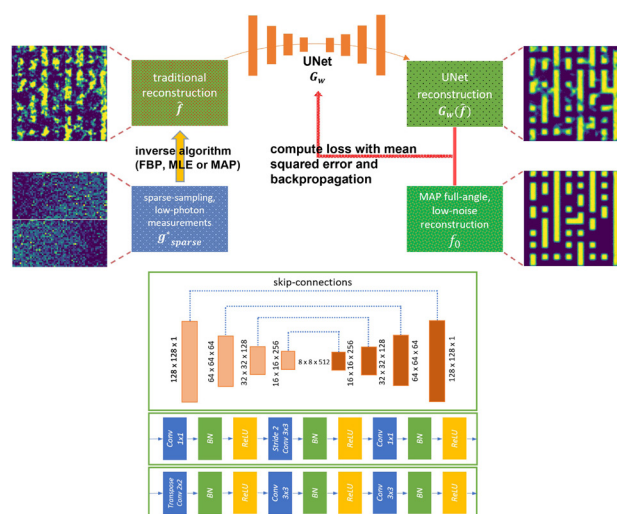
▲ Figure 2: Frequency and power measurements.

Noise Resilience Deep Reconstruction for X-ray Tomography

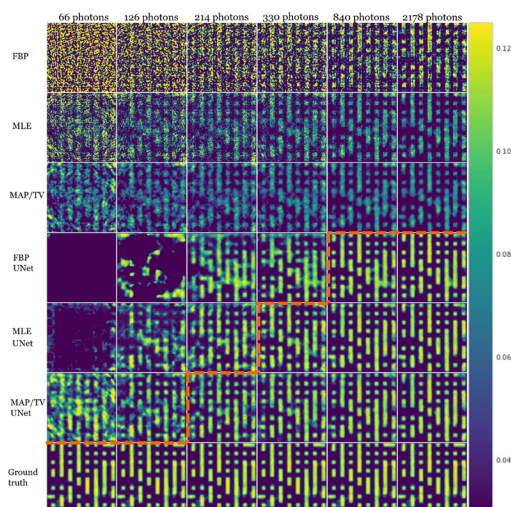
Z. Guo, Z. Liu, Q. Zhang, G. Barbastathis
Sponsorship: Singapore's National Research Foundation

X-ray tomography is a non-destructive imaging technique that visualizes the interior features of solid objects, with applications in biomedical imaging, materials science, manufacturing inspection, and other disciplines. Under limited-angle and low-photon sampling, a regularization prior is required to retrieve a high-fidelity reconstruction. Recently, deep learning has been used in X-ray tomography. The prior learned from training data replaces the general-purpose priors in iterative algorithms, achieving high-quality reconstructions with a neural network. Previous studies typically assume the noise statistics of testing data is acquired a priori from training data, leaving the network susceptible to a change in the noise characteristics under practical imaging conditions. In this work, we pro-

pose a noise-resilient deep-reconstruction algorithm for X-ray tomography. Our approach improves the noise resilience of the learned prior by using noise-resilient maximum a posteriori (MAP) reconstructions as the input to the neural network. Unlike previous efforts, we focus on the generalization of the deep learning algorithms to test data with different noise levels than the training data, which is critical in practical applications. Without training samples from different photon statistics, the MAP+UNet approach can produce acceptable reconstruction down to 50 photons per ray in simulations and 214 per ray in experiments, whereas the filtered back projection (FBP)+UNet approach requires around 10x more photons per ray in simulations and 2.5x more in experiments.



▲ Figure 1: A conceptual diagram for the learning-based algorithms.



▲ Figure 2: Selected 2D reconstruction for algorithms using experimental data. Each row represents a reconstruction algorithm. Each column represents an intensity of the photon rays. Dotted orange line is the boundary between acceptable and unacceptable performance as determined by the MST metric.

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MEMS, Thermal, Fluidic Devices, and Robotics

Multi-langmuir Probe Sensor Made via Rapid Prototyping for CubeSat and Laboratory Plasma Diagnostics	80
3D-printed Compact Peristaltic Vacuum Pumps	81
Extruded Quadrupole Mass Filters for CubeSats.....	82
3D-printed, Internally Fed Electrospray Thrusters for CubeSat Platforms.....	83
Laser-assisted Failure Recovery for Dielectric Elastomer Actuators in Aerial Robots	84
3D-printed Glass-ceramic Reflectron for Compact Mass Spectrometry	85
Silicon MEMS DACS and Finite Chord Slender Body Translating in a Vacuum.....	86

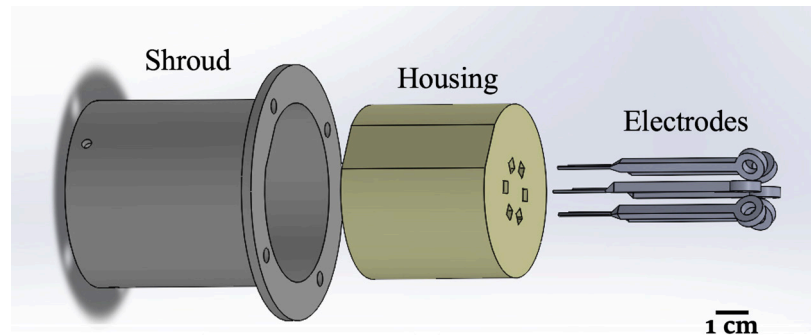
Multi-langmuir Probe Sensor Made via Rapid Prototyping for CubeSat and Laboratory Plasma Diagnostics

Z. Bigelow, L. F. Velásquez-García
Sponsorship: MIT Portugal

Langmuir probes (LPs) are widely considered to be the most versatile in-situ plasma sensors due to the simplicity of their design, small cross section, low maintenance requirements, and compatibility with a very broad range of plasma conditions. When operated with compact, low-power electronics, LPs can be installed onboard CubeSats to characterize the thermosphere—a portion of the ionosphere closely related to global warming. LPs operate by using one electrode to collect current while sweeping a bias voltage to measure plasma parameters. They can operate individually or in groups for improved accuracy, with double and triple LPs offering various benefits over single LPs.

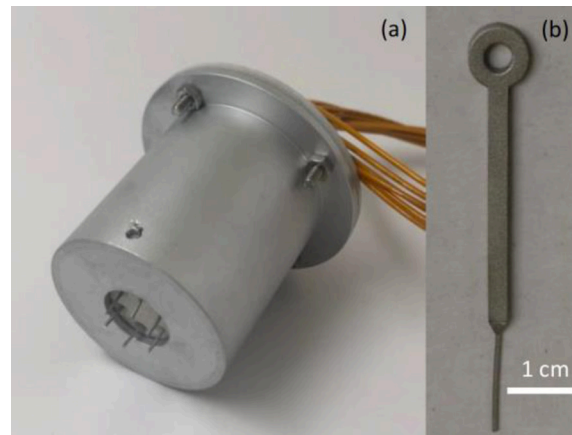
We report the design, fabrication, and characterization of the first fully additively manufactured, multi-LP sensor for CubeSat

ionospheric plasma diagnostics. The probes are configured on three different, independent sensing systems (i.e., single, dual, and triple LPs) that generate rich plasma data, including corroborated and real-time measurements. Plasma parameters from time-averaged probe configurations showed excellent agreement. The sensors are made via additive manufacturing (Figure 1): the housing is printed via vat polymerization in vitrolite, a glass-ceramic material (Figure 2a), and the electrodes are three-dimensional (3D)-printed via binder material jetting in stainless steel (Figure 2b). In this way, this device is compatible with in-space manufacturing and will allow, for the first time, the development of better and cheaper CubeSat sensors.



◀ Figure 1: Exploded schematic of the 3D-printed, multi-LP head.

▶ Figure 2: a) Fully assembled, 3D-printed LP head; the shroud has a 13.5-mm diameter hole that surrounds the LP array. b) Close-up of 3D-printed stainless-steel electrode.



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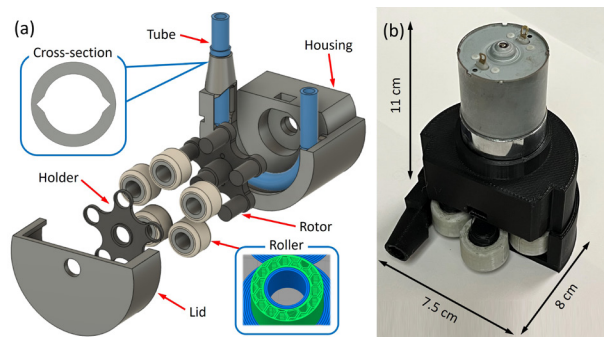
3D-printed Compact Peristaltic Vacuum Pumps

H. Lee, J. Cañada, L. F. Velásquez-García
Sponsorship: Empiriko Corporation, "la Caixa" Foundation

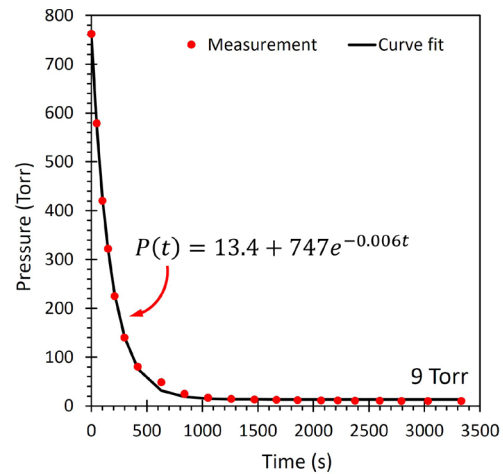
Peristaltic pumps are displacement pumps that transport fluids along a tube by compressing the tube into pockets and pushing the pockets along the pumping direction. Peristaltic pumps are one of the preferred means to transport liquids that need to stay inert or that are chemically reactive. However, due to the large forces required to fully seal the actuation tube and the high actuation speeds needed to overcome leakage, peristaltic pumps are rarely used in applications that require the transportation of gases (e.g., generation of vacuum). This work focuses on using material extrusion three-dimensional (3D)-printing, which allows the creation of multi-material parts with custom, complex geometries, to overcome the shortcomings of peristaltic pumps and enable their use to create and maintain dry vacuum in compact systems.

The proposed pump implements a novel actuator design with a notched cross section that enables the

full seal of the tube while requiring less than half the compression force of the typically used circular cross sections. This feature enables the creation and maintenance of dry vacuum, even at low actuation speeds. The device is fabricated through material extrusion using two materials: the rigid parts are printed in polylactic acid (PLA), and the compliant parts (e.g., actuator tube, exterior of compression rollers) are made in FiberFlex 40D (Figure 1). Experimental characterization of the 3D-printed peristaltic pump prototypes demonstrates that the devices can attain base pressures as low as 9 Torr (Figure 2), i.e., an order of magnitude lower than those achieved by state-of-the-art, single-stage, miniaturized diaphragm vacuum pumps. Our technology is of particular interest for in-situ, low-waste manufacturing of analytical hardware in areas with limited access to standard manufacturing techniques, including in-space manufacturing.



▲ Figure 1: Exploded view (a) and picture (b) of the 3D-printed peristaltic vacuum pump*



▲ Figure 2: Experimentally determined pressure versus time characteristic for a 3D-printed peristaltic vacuum pump.

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Extruded Quadrupole Mass Filters for CubeSats

A. Diaz, L. F. Velásquez-García
Sponsorship: MIT Portugal

Mass spectrometry is the gold standard for quantitative chemical analysis. Mass spectrometers employ mass filters that generate electromagnetic fields to sort out, in vacuum, by mass-to-charge ratio, the ionized constituents of a sample. However, mainstream mass spectrometers are large, heavy, and power hungry, restricting their ability to be deployed into CubeSats. Mass spectrometer hardware miniaturization has been attained at the expense of great loss in performance. Via additive manufacturing, it is possible to create complex objects monolithically and more precisely. Also, additive manufacturing is compatible with in-space manufacturing. One of the most versatile mass filters is the quadrupole mass filter, which uses a combination

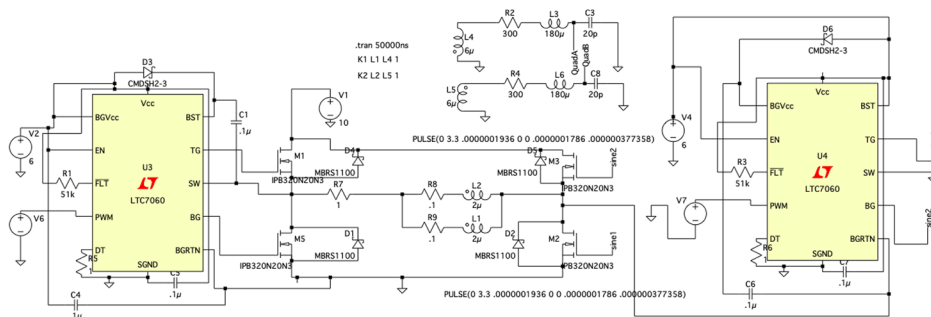
of alternating and direct current (ac and dc) voltages to contain charges species of a given specific charge. There are reports of 3D-printed quadrupoles, but they are not monolithically made.

In this project we are exploring the feasibility of implementing monolithically 3D-printed, compact quadrupole mass filters. The devices were made via multi-material extrusion (Figure 1). We are also developing compact electronics to drive the quadrupoles that are compatible with the size, weight, and power constraints of CubeSats. Current work focuses on characterizing and optimizing the technology.



◀ Figure 1: A monolithically 3D-printed quadrupole mass filter.

▼ Figure 2: Low-power electronics to drive the 3D-printed QMF developed in this study.



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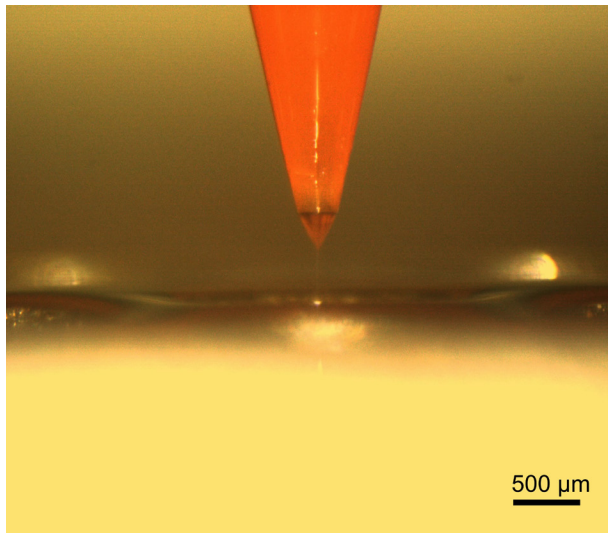
3D-printed, Internally Fed Electro spray Thrusters for CubeSat Platforms

H. Kim, L. F. Velásquez-García
Sponsorship: MIT Portugal

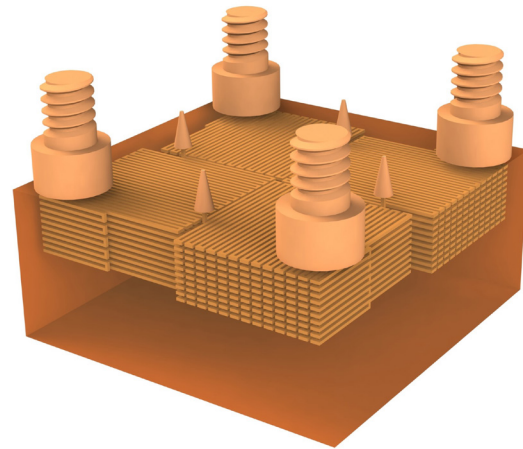
An electro spray thruster offers several benefits as a propulsion system for small satellites including a lower power requirement when miniaturized and a broad range of thrust and specific impulse. However, multiplexed electro spray thrusters have traditionally been manufactured via microfabrication in a cleanroom, which is expensive, time-consuming, and not compatible with in-space manufacturing. Advances in three-dimensional (3D) printing technology make it possible to create microstructures at a much lower cost than microfabrication. However, internally fed electro spray thrusters have only been fabricated in a cleanroom so far, primarily due to their high hydraulic resistance requirement for the uniform operation of emitters. The uniform operation of emitters is essential for the high efficiency of the thruster and correct control of the thrust it generates. The precision of 3D printing the channels is therefore important; a high hydraulic resis-

tance channel is also beneficial for mitigating the effect of uncertainties result from Taylor cones on each emitter. This study approaches this problem in two ways to 3D print the internally fed electro spray thruster. The first approach optimizes the channel design, considering 3D printing resolution and electro spray physics. The second approach modifies liquid resin for 3D printing to expand the lower limit on the internal channel size.

The characterization of a single-emitter device showed stable emission for multiple flow rates, with current and flow rate following the well-known scaling law of electro spray in cone-jet mode. The thrust and specific impulse estimates showed that the device performance is comparable to state-of-the-art cleanroom microfabricated, internally fed electro spray thrusters. The current focus is on multiplexing the emitters.



▲ Figure 1: A photo of a Taylor cone on the emitter.



▲ Figure 2: The optimized channel design for 4 emitters to minimize possible non-uniformity of flow between emitters. The channel width, height, and length are 370 μm , 350 μm , and 2 m, respectively.

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Laser-assisted Failure Recovery for Dielectric Elastomer Actuators in Aerial Robots

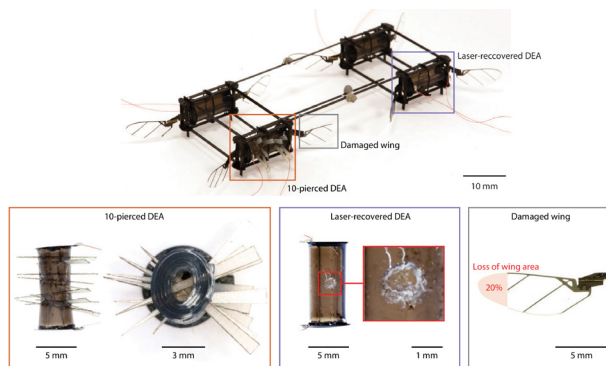
S. Kim, K. Chen

Sponsorship: RLE, MIT, Mathworks Engineering Fellowship, NSF

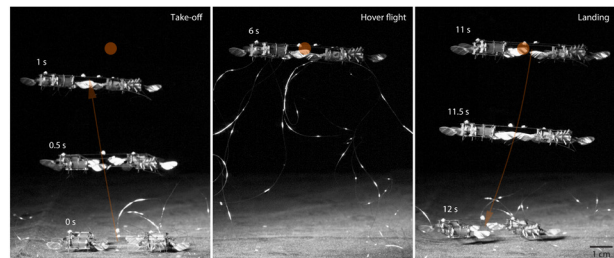
To survive in nature, insects exhibit remarkable resilience to flight muscle and wing damage caused by predator attacks and general wear. Motivated by applications such as exploration of cluttered and constrained environments, researchers developed micro-aerial-vehicles (MAVs) that can endure in-flight collisions by implementing impact-resilient mechanisms or designing flight controllers to compensate for unexpected damage. However, unlike natural flight muscles, rigid flight actuators cannot tolerate punctures or incision damage, which limits MAVs' robustness when they perform high-risk missions. Dielectric elastomer actuators (DEAs) are soft transducers that have enabled robots to move with similar agility to those using rigid actuators. However, they are prone to local defects that can cause global device failure, limiting their performance, lifetime, and scalability.

In this work, we proposed the design, fabrication, and repair methods that led to soft artificial flight muscles capable of enduring severe damage (Figure 1). We first developed a DEA that can endure more than 100 punctures while maintaining high bandwidth

(>400 Hz) and power density (>700 W/kg)—sufficient for supporting energetically expensive locomotion such as flight. When the DEA suffered severe dielectric breakdowns that caused device failure, we demonstrated a laser-assisted repair method for isolating the critical defects and recovering performance. To illustrate the effectiveness of our methods, we constructed an insect-scale flapping-wing robot using damaged DEAs. After enduring severe piercing damage, unrepairable breakdowns, and a 20% loss of wing area, the robot demonstrated a twelve-second feedback-controlled flight (Figure 2) with a maximum position error of 3.56 cm (0.7 body length). For the first time, an aerial robot endured critical actuator damage and demonstrated hovering flights of similar position and attitude accuracy. This result not only represents a challenging biomimetic capability that is absent in existing robots, but also highlights the unique advantages of applying soft artificial muscles in place of traditional rigid actuators.



▲ Figure 1: The aerial robot consisted of four modules that could maintain controlled flight capability despite enduring severe damage. The robot modules were pierced by ten fiber glass needles, laser-recovered after experiencing permanent breakdown, and lost 20% area near the wing tip.



▲ Figure 2: A twelve-second hovering flight performed by the severely damaged robot shown in Figure 1. One DEA was pierced by ten needles, the other DEA suffered an unrepairable breakdown, and one robot wing lost 20% of its area.

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3D-printed Glass-ceramic Reflectron for Compact Mass Spectrometry

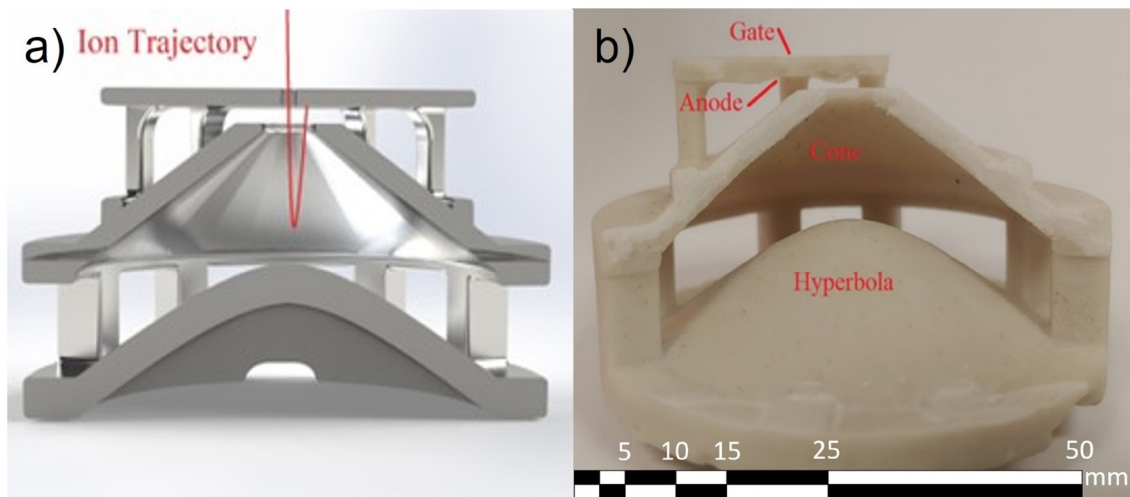
N. Lubinsky, L. F. Velásquez-García
Sponsorship: Empiriko

Accurate measurement of blood plasma constituents is essential for conducting drug assays and monitoring biomarkers. The traditional gold standard to attain these is by employing a triple quadrupole—an expensive, bulky, and power-hungry instrument. Our research group aims to harness advanced additive manufacturing, micro-, and nanotechnology to demonstrate mass spectrometry hardware that is inexpensive and capable.

One design we are currently exploring is a self-contained reflectron mass spectrometer. This device filters ions by mass-to-charge ratio by measuring the time-of-flight (TOF) of ions as they are reflected by the internal electromagnetic fields of the device. The geometry of the mass filter is a hyperbola surrounded by a cone, creating a potential distribution that is quadratic with distance (Figure 1). This way, the ions

exhibit a repelling force independent of the initial energy of the ion. Therefore, we expect a TOF solely dependent on the specific mass-per-charge of the ions.

To filter ions, the reflectron requires the use of an entrance gate electrode with an aperture for ions. Once the potential drops to 0 V on the gate, ions flow into the reflectron, ultimately reflecting towards the entrance, to a nearby particle detector. The time from the delay of the gate switching off to the time we register the MCP pulses constitutes the TOF of an individual ion, which depends on the specific mass-to-charge ratio of the ion. In our approach, the electrodes are three-dimensionally (3D)-printed monolithically in glass-ceramic via vat photopolymerization. Post-print, we selectively plate them, forming conductive surfaces. Current research efforts focus on optimizing the 3D-printed hardware and characterizing it in vacuum.



▲ Figure 1: Monolithic reflectron cross section of simulations of particle trajectories (a) and post-print result (b). A hyperbolic electrode is surrounded by a grounded cone, 3D printed in glass-ceramic via vat photopolymerization, and coated in nickel (not shown). Adapted from *IVNC 2023 Conference Proceedings*.

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Silicon MEMS DACS and Finite Chord Slender Body Translating in a Vacuum

J. Protz

Sponsorship: Protz Lab Group; microEngine, LLC; Asteria Propulsion LLC

Micro-electromechanical systems (MEMS) rockets have been researched at MIT for two decades. Previously, the researcher has explored micro rockets with steam injectors, micro jet engines, and a replacement for model rocket igniters and primer caps made as a sq. mm-sized MEMS chip that would combine a computer, sensors, and a micro-rocket motor. Recently, the researcher has looked at using the latter to make a divert and attitude control system (DACS) for a bullet or for the final stage of a miniature launch vehicle. As envisioned, blind holes would be drilled into the base of a bullet; into each would be stacked a battery, a packaged MEMS primer cap chip, solid propellant, and a clay nozzle. The battery would power the chip, the chip's plume would ignite the grain, the burning grain would exhaust through the nozzle, the bullet would be released from a rifled barrel or spinning rocket and spin, and the thrust would create a torque that causes precession. By control of the timing and sequence of the firings of the grains, the bullet could be steered in mid-flight. The advantage of the chip would be its low cost.

The effort is at an early stage and focuses on identifying technologies to join as a system. If successful, it could enable hobby rocket-sized launch vehicles or find use in such Olympic sports as biathlons. Other recent work by the investigator

has focused on the modeling of finite-chord slender bodies translating at high speed in a high vacuum. The investigator conjectures that the mass density everywhere in the universe is positive definite; the mass density of the vacuum approaches zero but never reaches it; and objects transiting the vacuum have boundary films, near wakes, wake shear zones, etc. The researcher further conjectures that Pendry's theoretical result for the drag caused by the Casimir effect, etc., two plates separated by a small vacuum gap translate relative to each other, can be extended to compute the drag on a lone translating slender body by noting that the boundary film undergoes acceleration. By the Unruh effect, this finding suggests that the far vacuum ("free stream") appears to the boundary film to be a thermal bath, and this causes the boundary film to appear to be a vacuum gap that separates two plates that are translating relative to each other. The "lumped parameter" approach used can also be applied to the analogous problem in fluid dynamics. The project is at an early stage, and mathematical modeling is in progress. A next step after the modeling could be to design a nano-EMS (NEMS) device capable of measuring the vacuum drag experimentally. If this project is successful, it will advance the engineering of vehicles for high-speed space flight.

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Nanoscience, Nanotechnology, Nanomaterials

Acoustically Active Surfaces Based on Piezoelectric Microstructures.....	88
Morphological Change of Hydrogen Gas Doped Metal Oxide Nanoparticles under Charge Flow.....	89
Using Point Defects to Control Giant Opto-mechanical Effects in Wide-band-gap Semiconductors.....	90
Atomic-scale Mechanisms of MoS ₂ Oxidation for Kinetic Control of MoS ₂ /MoO ₃ Interfaces.....	91
Chemical Vapor Deposition Synthesis of Multilayer Hexagonal Boron Nitride.....	92
Weighing the DNA Content of Adeno-associated Virus Vectors with Zeptogram Precision using Nanomechanical Resonators.....	93
Modelling Interfacial Competition on Drug Crystal Surfaces Using Molecular Dynamics Simulations.....	94
Discovery of a Family of Magic-angle Twisted Graphene Superconductors.....	95
Predicting Coherent Nanocrystal Orientation in Nanocrystal Superlattices by Minimizing Ligand Packing Frustration.....	96
Van Der Waals Integration Beyond the Limits of Van Der Waals Forces.....	97
Nonplanar Nanofabrication via Interface Engineering.....	98
Role of Local Gyrotropic Force in Distortion-limited High-speed Dynamics of Antiferromagnetic Skyrmion.....	99
Metal-graphene Interface in Evaporative-deposition of Various Metals on Graphene.....	100
Interfacial Ferroelectricity in Rhombohedral-stacked Bilayer Transition Metal Dichalcogenides.....	101
Electrical Switching of a Bistable Moiré Superconductor.....	102
Spectroscopy Signatures of Electron Correlations in a Trilayer Graphene/hBN Moiré Superlattice.....	103
Nanofabrication of Metasurface Structures for Holography, Using Laser Ablation-based Implosion Fabrication.....	104
Contact Printed Nanoparticles as Building Blocks for Active Nanodevices.....	105

Acoustically Active Surfaces Based on Piezoelectric Microstructures

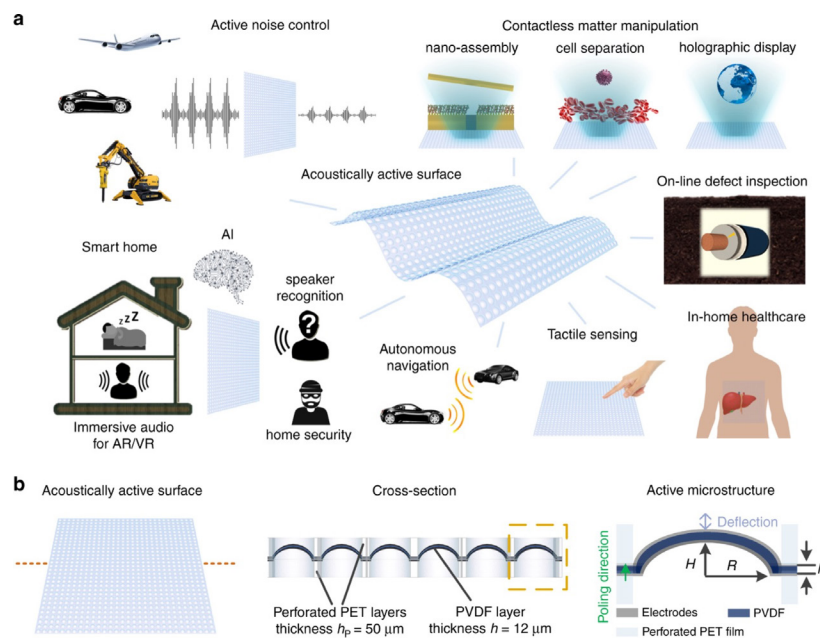
T. Dang, J. Han, J. Lang, V. Bulović
Sponsorship: Ford Motor Company, Lendlease Group

Acoustic transducers have attracted significant attention due to their ubiquitous application in modern-day technologies, such as active noise control, human-machine interfaces, ultrasonic imaging, and tactile sensing (Figure 1a). The industrial and consumer demand for using sound as a sensing and actuation medium has encouraged the development of cost-effective, scalable, and high-performance loudspeakers. Commercial speakers typically generate sound based on electrostatic or piezoelectric effects; among these, piezoelectric loudspeakers have stood out due to their simple structures and low power consumption.

In this project, we develop a flexible thin-film acoustic transducer based on an ensemble of free-standing microstructures using a piezoelectric polyvinylidene fluoride (PVDF) sheet. The

microstructures follow the shape of a dome fabricated through a vacuum-induced self-aligned micro-embossing process (Figure 1b). These PVDF dome arrays are sandwiched between two layers of perforated polyethylene terephthalate (PET) sheets, which serve as both the embossing mold and a protection layer to ensure the free vibration of the piezoelectric microstructures.

The performance of the speakers is subsequently measured, and they demonstrate excellent sound generation and sensing capabilities as well as high sensitivity and large bandwidths. Our ongoing work focuses on scaling up the current speakers and integrating them into various sound-generating applications.



▲ Figure 1: Concept and structure of acoustically active surfaces. (a) Application prospects of acoustic surfaces. (b) Schematic showing the cross section of an acoustic surface and a magnified picture of an active microstructure within the array.

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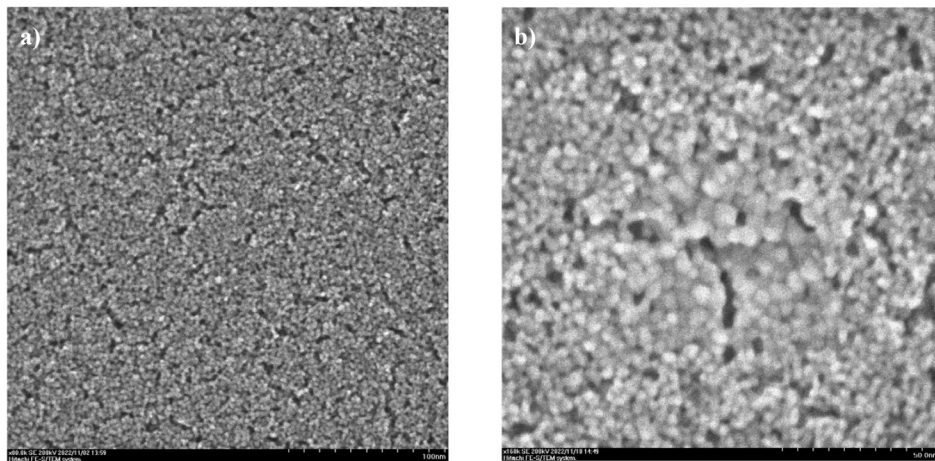
Morphological Change of Hydrogen Gas Doped Metal Oxide Nanoparticles under Charge Flow

J. Geng, M. Saravanapavanantham, A. Penn, V. Bulović
Sponsorship: Samsung

Quantum dot light-emitting diodes (QD-LEDs) emit color-pure, easily tunable, bright light and are thus a promising new technology for lighting and display applications. However, before market viability, they must be made more efficient and durable. Zinc magnesium oxide (ZnMgO) nanoparticles serve as an excellent electron transport layer in indium phosphide QD-LEDs. It has been observed that operating QD-LEDs under hydrogen gas flow causes performance improvement over a short timescale.

To investigate this effect, we simultaneously flowed hydrogen gas over a drop-cast layer of ZnMgO nanoparticles and imaged the layer in an in-situ transmission electron microscope (TEM). Figure 1 shows images of the nanoparticles before and during

hydrogen gas flow. We observed that the nanoparticles coarsen over a few minutes once doped with hydrogen and irradiated with the electron beam, which simulates the passage of charge through the device. The resulting doped and irradiated spots are comprised of larger, fewer dots and significant cracks. This effect only occurs in areas of dense nanoparticle population, where particles may merge. These observations allow us to hypothesize that the larger dots allow for better charge transport through the layer due to fewer necessary grain boundary crossings. These results provide a physical explanation for improved QD-LED performance under hydrogen and may inform further development of the InP QD-LED.



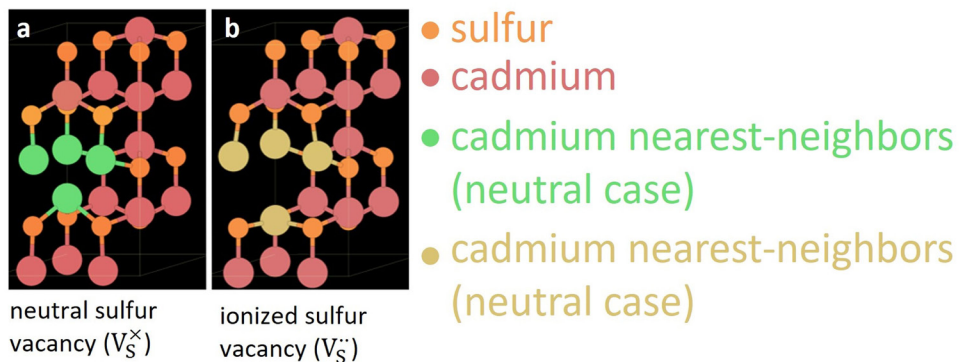
▲ Figure 1: TEM images of ZnMgO nanoparticle layer a) before and b) during hydrogen gas flow.

Using Point Defects to Control Giant Opto-mechanical Effects in Wide-band-gap Semiconductors

J. Dong, Y. Li, Y. Zhou, A. Schwartzman, H. Xu, B. Azhar, J. Bennett, J. Li, R. Jaramillo
Sponsorship: Office of Naval Research (Grant No. N00014-17-1-2661)

Semiconductor point defects that create deep charge traps are often to be avoided because they speed up bad things (e.g., non-radiative recombination) and slow down good things (e.g., photodetector response). Nevertheless, deep traps often feature large charge-lattice coupling phenomena that are fundamentally interesting and could be put to good use. We found experimentally that deep traps in II-VI semiconductors CdS, ZnS, and ZnO are correlated with giant opto-mechanical effects, such as changes in hardness and elastic modulus greater than 50% under relatively mild illumination

(e.g., blue light at 1.5 mW/cm²) during nanoindentation, and that these giant effects can be tuned by materials processing. Giant photoplasticity has been reported and understood conceptually for decades, but the giant photoelastic effect that we observe has not been understood. Using density functional theory, we find that giant photoelasticity can arise from changes in lattice configuration resulting from defect ionization (i.e., DX center phenomena). This places photoelasticity on a firm theoretical footing and paves the way for parametric design of devices using the effect.



▲ Figure 1: Illustrations of changed atomic positions around sulfur vacancy in CdS, as vacancy changes from neutral (a) to doubly ionized state (b). Illustrations project atomic positions computed using density functional theory. Colors highlight changed positions of four Cd atoms nearest vacancy.

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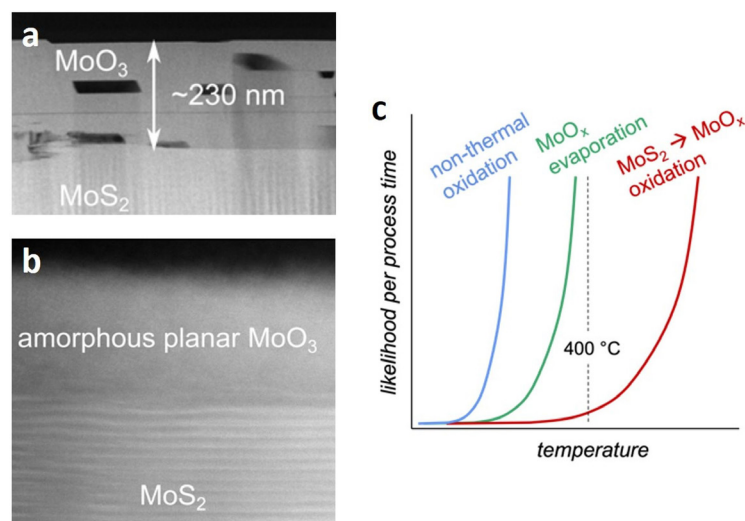
Atomic-scale Mechanisms of MoS₂ Oxidation for Kinetic Control of MoS₂/MoO₃ Interfaces

K. Reidy, W. Mortelmans, S. S. Jo, A. N. Penn, B. Wang, A. C. Foucher, F. M. Ross, R. Jaramillo
Sponsorship: Semiconductor Research Corporation, Office of Naval Research (Grant No. N00014-17-1-2661)

Like most semiconductors, the surfaces of transition metal dichalcogenides (TMDs) are prone to oxidation. TMDs are now on development roadmaps for continued transistor scaling, which increases the importance of controlling TMD oxidation and understanding the electrical properties of interfaces between TMDs and their oxides. A lesson learned from Si microelectronics is that, if at all possible, we should make use of semiconductor native oxides. Particularly for semiconducting TMDs for which the native oxides may be useful dielectrics (or even ferroelectrics), there is an opportunity to better understand the processing-property relationships that control dielectric response, leakage, and interface quality. For TMDs for which the native oxides have easily varied conductivity, there is an opportunity to develop resistive switching functionality, or to develop native oxide electrodes.

Here, we investigate the atomic scale oxidation

mechanisms of the most widely studied TMD, MoS₂. We find that thermal oxidation results in α -phase crystalline MoO₃ with sharp interfaces, voids, and a textured alignment with the underlying MoS₂. Experiments with remote substrates prove that thermal oxidation proceeds via vapor-phase mass transport and redeposition, due to rapid evaporation of the oxide—a challenge to forming thin, conformal planar oxide films. We accelerate the kinetics of oxidation relative to the kinetics of mass transport using a non-thermal oxygen plasma to form a smooth and conformal oxide. The resulting amorphous MoO₃ films can be grown several nanometers thick, and we calibrate the oxidation rate for varying processing conditions. Our results provide quantitative guidance for managing both the atomic scale structure and thin film morphology of oxides in the design and processing of TMD devices.



▲ Figure 1: Kinetics of thermal vs. non-thermal oxidation. (a) Transmission electron micrograph (TEM) of a crystalline, non-uniform MoO₃ layer formed by thermal oxidation of MoS₂. (b) TEM of an amorphous, uniform MoO₃ layer formed by plasma oxidation of MoS₂. (c) Schematic of rates of relevant processes: thermal oxidation, evaporation, and non-thermal oxidation.

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Chemical Vapor Deposition Synthesis of Multilayer Hexagonal Boron Nitride

H. Liu, Z. Luo, J. Kong

Sponsorship: EECS Faculty Research Innovation Fellowship

Hexagonal boron nitride (hBN) has attracted tremendous research interest due to its wide band gap of up to ~6 eV, remarkable chemical and physical stability, atomic surface flatness, etc. As such, hBN serves as a promising candidate as quantum emitters, insulators, or support for the next generation of electronic and photonic devices. Recent reports on the wafer-scale synthesis of hBN are limited to monolayer or few layers, which is due to the self-limited growth regime for the growth substrates with low nitrogen solubility. However, monolayer or few-layer hBN is limited in its performance, some of the problems include unstable optical emission, non-satisfied mechanical strength, inability to screen out substrate effects, etc. In this work, we propose to utilize single crystalline metal alloys as

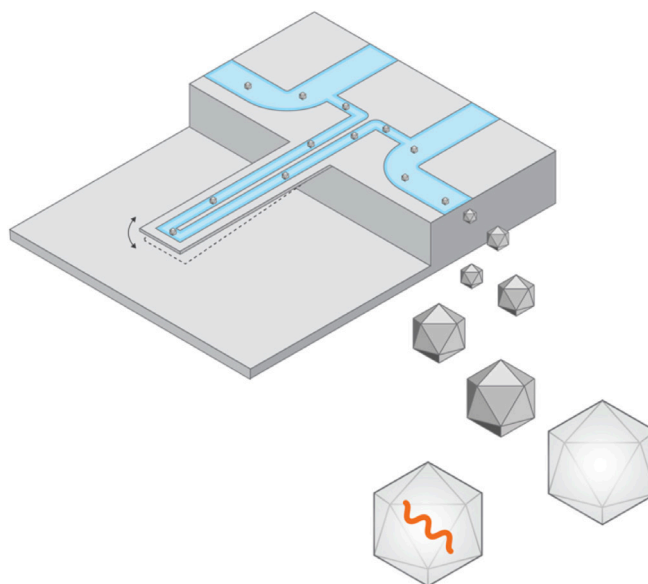
the growth substrate to synthesize multilayer hBN by chemical vapor deposition. The uniformity of both substrates and the as-synthesized hBN films will be characterized by optical contrast and Raman spectroscopy mapping. The crystallinity of the hBN films will be characterized by XRD and the full width at half maximum of Raman peaks corresponding to hBN. Atomic force microscopy will be used to measure the hBN thicknesses and electron microscopy will be conducted to reveal the microstructure of hBN films. The success of this work will help to improve the next generation of 2D materials-based electronic devices, finally leading to a world with a higher information transport rate with less energy consumption compared to the current Si-based devices.

Weighing the DNA Content of Adeno-associated Virus Vectors with Zeptogram Precision using Nanomechanical Resonators

G. Katsikis, I. E. Hwang, W. Wang, V. S. Bhat, N. L. McIntosh, O. A. Karim, B. J. Blus, S. Sha, V. Agache, J. M. Wolfrum, S. L. Springs, A. J. Sinskey, P. W. Barone, R. D. Braatz, S. R. Manalis
Sponsorship: U.S. Food and Drug Administration

Quantifying the composition of viral vectors used in vaccine development and gene therapy is critical for assessing their functionality. Adeno-associated virus (AAV) vectors, which are the most widely used viral vectors for in vivo gene therapy, are typically characterized using polymerase chain reaction (PCR), enzyme-linked immunosorbent assay (ELISA), and analytical ultracentrifugation, which require laborious protocols or hours of turnaround time. Emerging methods such as charge-detection mass spectroscopy, static light scattering, and mass photometry offer turnaround times

of minutes for measuring AAV mass using optical or charge properties of AAV. Here, we demonstrate an orthogonal method where suspended nanomechanical resonators (SNR) are used to directly measure both AAV mass and aggregation from a few microliters of sample within minutes. We achieve a precision near 10 zeptograms, which corresponds to 1% of the genome holding capacity of the AAV capsid. Our results show the potential of our method for providing real-time quality control of viral vectors during biomanufacturing.



▲ Figure 1: Concept of measuring mass of AAVs in solution showing a schematic of a hollow cantilever of length 17.5 μm . Inside the cantilever, we flowed solutions of AAVs with different DNA content or genetic constructs (denoted by orange).

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- G. Katsikis, I. E. Hwang, W. Wang, V. S. Bhat, N. L. McIntosh, O. A. Karim, B. J. Blus, S. Sha, V. Agache, J. M. Wolfrum, S. L. Springs, A. J. Sinskey, P. W. Barone, R. D. Braatz, and S. R. Manalis, "Weighing the DNA Content of Adeno-Associated Virus Vectors with Zeptogram Precision Using Nanomechanical Resonators," *Nano Letters*, vol. 22, no. 4, pp. 1511–1517, Feb. 2022.

Modelling Interfacial Competition on Drug Crystal Surfaces Using Molecular Dynamics Simulations

D. Nguyen, L. Attia, D. Gokhale, P. S. Doyle
Sponsorship: MIT UROP Office

Oral administration is often preferred among all drug administration routes due to its simplicity, low cost, and convenience. However, nearly 90% of drug candidates in the pharmaceutical development pipeline have high hydrophobicity, which significantly hinders their dissolvability in the gastrointestinal (GI) tract and limits bioavailability. Our lab has developed a suite of 'bottom-up' methods to template drug nanocrystals by embedding APIs in polymeric matrices as an approach to reduce drug aggregate sizes for improved bioavailability. However, recent experimental results have motivated the need for a mechanistic understanding of the influence of excipient-drug interactions during processing.

In this work, we present the use of molecular dynamics (MD) simulations to advance understanding of how molecular interactions between excipients and drug control the self-assembled nanostructure on drug crystal surfaces. MD is used to explore the compositional effects of surfactant and polymer excipients interacting on the surface of a model hydrophobic API (fenofibrate). The role of surfactant in screening polymer-drug interactions is elucidated as an important mechanism for designing 'bottom-up' small molecule formulation processing schemes. Based on the results of this work, various combinations of drugs, surfactants and polymer matrices can be tested computationally and experimentally, leading to the next generation of oral drug delivery forms.

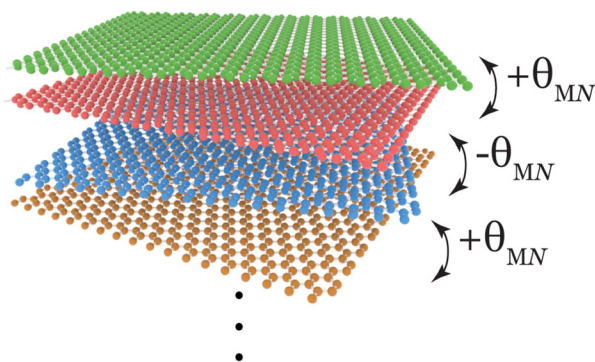
Discovery of a Family of Magic-angle Twisted Graphene Superconductors

J. M. Park, Y. Cao, L. Xia, S. Sun, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero
Sponsorship: Department of Energy, NSF

When materials are thinned down to an atomic limit, properties vastly different from their three-dimensional counterparts appear. Further, these two-dimensional (2D) materials can be stacked to create a new type of platform called van der Waals heterostructures, which exhibit novel phases not present in the constituent layers. More recently, another degree of freedom that controls the relative twist angle between the adjacent layers has been explored, giving rise to the field of moiré systems. In particular, when two layers of graphene were stacked with a relative twist angle of 1.1 degrees, unexpected insulator and superconductor were observed. After the discovery of such magic-angle twisted bilayer graphene (MATBG) system, various kinds of moiré systems were investigated, and novel interaction-driven phenomena including correlated insulators, quantum anomalous Hall effect, ferromagnetism, and generalized Wigner crystal were found.

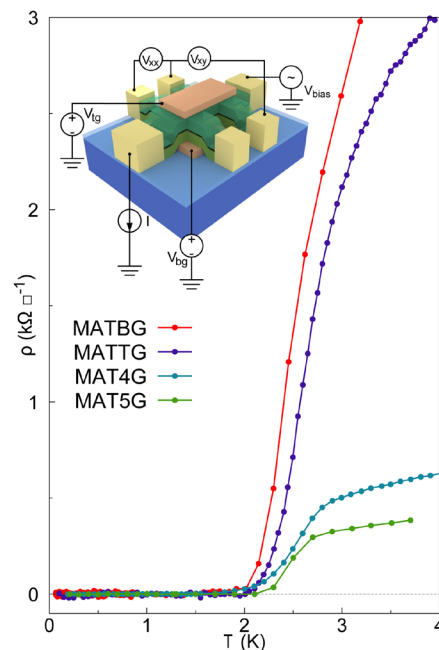
Despite the numerous correlated phases observed

in moiré systems, signatures of robust and reproducible superconductivity have been rare and only found in MATBG and more recently in MAT trilayer graphene. In this study, we report the experimental realization of superconducting MAT four-layer and five-layer graphene, therefore establishing alternating twist magic-angle multilayer graphene as a robust family of moiré superconductors. This finding suggests that the flat bands present in all members play a crucial role in forming the superconductivity. Our measurements in parallel magnetic fields, particularly the investigation of Pauli limit violation and spontaneous rotational symmetry breaking, reveal a clear distinction between the $N=2$ and $N>2$ -layer structures, consistent with the difference between their orbital responses to magnetic fields. Our results expand the emergent family of moiré superconductors, providing novel insight into the design of unconventional superconducting materials platforms.



▲ Figure 1: Magic-angle twisted multilayer graphene, where the adjacent layers are twisted in an alternating direction.

► Figure 2: Zero resistivity shows robust superconductivity in the magic-angle twisted multilayer graphene family.



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Predicting Coherent Nanocrystal Orientation in Nanocrystal Superlattices by Minimizing Ligand Packing Frustration

E. K. Price, W. A. Tisdale

Sponsorship: DoE Office of Science, Basic Energy Sciences, NSF Graduate Research Fellowships Program (GRFP)

Semiconducting, colloidal nanocrystals (NCs) have size-tunable optical and electronic properties and show promise for next-generation sensing, photovoltaic, and computing devices. For integration into optoelectronic devices, NCs are assembled into ordered superlattices (SLs). Since the SL structure can influence charge and thermal transport in these devices, robust engineering control over SL formation is needed. A number of factors influence the self-assembly of colloidal NCs, including the well-studied impacts of nanocrystal size and shape. In recent years, the importance of both bound and unbound organic ligands on self-assembly outcomes has been highlighted; the ligand length, ligand coverage, bound and unbound ligand fractions, and ligand interactions can all influence the resulting NC SL structure. In this work, we consider how the classic influence of nanocrystal shape can impact ligand packing frustration and influence the coherent orientation of non-spherical NCs in NC

SLs. Through the application of the freely jointed chain model to estimate conformational entropy, we find that minimizing the packing frustration of the ligand layer may explain experimental observations of NC alignment in NC SLs. We validate our model by comparing to published X-ray scattering data showing the kinetics of lead sulfide (PbS) superlattice formation. These data show that as solvent is evaporated, the SL exhibits a Bain-like distortion, contracting from an fcc to bcc configuration, and the coherent NC tilt relative to the substrate changes from 9.7° to 0° . The thermodynamic understanding of coherent NC orientation in NC SLs explored in this work may inform the synthesis of high-quality films with minimal disorder for integration into optoelectronic devices and enable the experimental realization of predicted theoretical properties such as band-like transport in NC SLs.

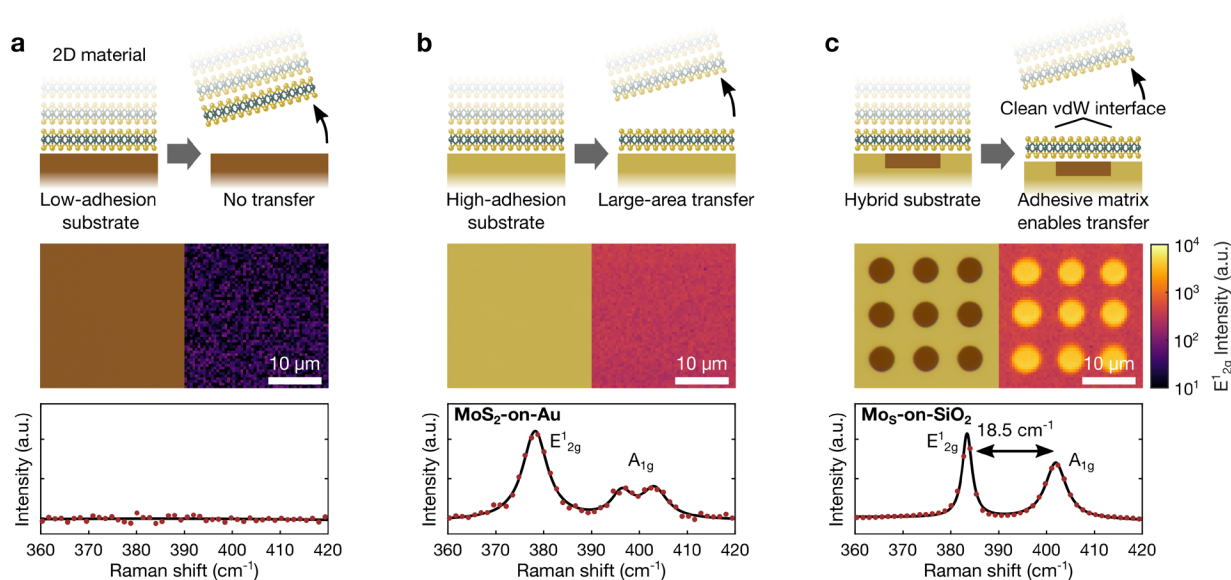
Van Der Waals Integration Beyond the Limits of Van Der Waals Forces

P. F. Satterthwaite, W. Zhu, P. Jastrzebska-Perfect, M. Tang, H. Gao, H. Kitadai, A.-Y. Lu, Q. Tan, J. Kong, X. Ling, F. Niroui
Sponsorship: NSF Center for Energy Efficient Electronics Science (E3S) (ECCS-093951), NSF EAGER (2135846), NSF Graduate Research Fellowship Program (1745302)

Fabrication of pristine van der Waals (vdW) interfaces between two-dimensional (2D) and other materials is essential for emerging optical and electronic devices. The weak vdW forces at the interface of interest cannot, however, be readily tuned to enable direct integration of arbitrary materials. Conventionally, this is addressed by transferring the 2D material using sacrificial layers, solvents and high-temperatures, introducing damage and contaminants. Conventional device integration further requires post-transfer fabrication steps which can lead to device performance being constrained by the processing artifacts rather than the intrinsic materials properties.

Here, we introduce a novel fabrication platform, adhesive matrix transfer, which enables direct 2D material-to-device integration in a single, dry step.

This is achieved by decoupling the forces enabling transfer from the forces at the interface of interest. For example, 2D semiconductors such as MoS_2 cannot be directly transferred to dielectrics such as SiO_2 , low adhesion but important substrates for device integration (Fig. 1a). In contrast, direct transfer of monolayer MoS_2 to gold can be achieved (Fig. 1b), but MoS_2 -on-gold is of limited technological value. By using gold as an adhesive matrix surrounding SiO_2 , MoS_2 -on- SiO_2 can be directly fabricated with no exposure to solvents or polymers (Fig. 1c). Using this transfer, we further demonstrate clean, direct fabrication of MoS_2 transistors demonstrating the ability of our platform to enable direct 2D material-to-device integration.



▲ Figure 1: Adhesive matrix transfer. (a) Direct transfer of MoS_2 to SiO_2 is not possible due to weak adhesive interactions. (b) MoS_2 can, however, be directly transferred to gold. (c) Using gold as an adhesive matrix, MoS_2 -on- SiO_2 can be directly fabricated. Top row shows schematic illustration of experiments. Middle row shows optical micrographs, and Raman intensity mapping. Bottom row shows characteristic Raman spectra.

Nonplanar Nanofabrication via Interface Engineering

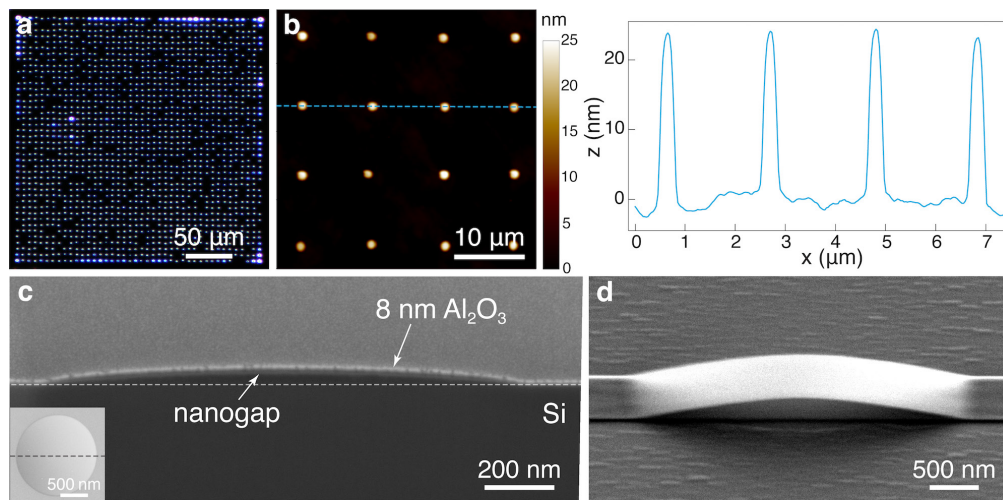
S. O. Spector, P. F. Satterthwaite, F. Niroui

Sponsorship: NSF Graduate Research Fellowship, Samsung Electronics Fellowship

Nonplanar nanostructures, composed of suspended ultrathin films and nanogaps, are foundational for next-generation miniaturized nanoelectromechanical devices, photonic elements, and metamaterials. However, resolution constraints and instabilities due to nanoscale forces limit their fabrication through conventional top-down techniques.

This work reports a new approach for scalable fabrication of suspended, ultrathin nanostructures with controlled nanoscale gaps, without the use

of a sacrificial layer. We engineer surface adhesive forces through a patterned molecular monolayer to enable controlled delamination of an oxide thin film in predetermined locations. By extending standard, wafer-scale, and conventionally compatible planar fabrication techniques, we form nonplanar structures with thicknesses < 10 nm and nanogaps reaching < 10 nm. Using this approach, we demonstrate ultrathin mechanical resonators in the megahertz range with applications in ultrasensitive sensors.



▲ Figure 1: (a) Darkfield image of an array of dome-shaped Al₂O₃ nanostructures. (b) Atomic force microscopy (AFM) and line scan of a nanostructure array. (c) Cross-sectional scanning electron microscopy (SEM) of a fabricated 8 nm-thin suspended membrane. (d) SEM of a doubly clamped, 8 nm-thin mechanical resonator.

Role of Local Gyrotropic Force in Distortion-limited High-speed Dynamics of Antiferromagnetic Skyrmion

E. A. Tremsina, G. S. D. Beach

Sponsorship: NSF GRFP, DARPA TEE Program, SMART, one of seven centers of nCORE, a Semiconductor Research Corporation program, sponsored by NIST

Magnetic solitons, quasiparticles formed by a local twist in the magnetization, are great candidates for use in novel spintronic devices. The key question for their use in practical applications, however, is the maximum speed of propagation through magnetic media. For one-dimensional solitons (domain walls), the high-speed dynamics are well understood and are limited in antiferromagnetic materials by relativistic-like effects, namely velocity saturation towards a speed akin to the speed of light, and Lorentz-like width contraction. Two-dimensional solitons (skyrmions) instead exhibit elliptical distortions followed by a full breakdown at a critical limiting velocity, and the exact nature of this

process is yet to be understood. Here, the unique capabilities of a fully atomistic model are used to perform an extensive and systematic study of soliton dynamics. As a result, a physical explanation for skyrmion deformations, which are attributed to the local imbalance of the gyrotropic forces, is derived using numerical simulation data. It is shown also that the inherent skyrmion structure impedes their ability to even reach the velocity regime where relativistic effects could begin to occur. These results expand the understanding of the fundamental properties of magnetic skyrmions, in particular, their dynamical stability at high speeds, as well as their potential use for spintronic applications.

Metal-graphene Interface in Evaporative-deposition of Various Metals on Graphene

Z. Wang, H. Wang, J. Zhu, T. Pieszkow, X. Zheng, S. A. Vitale, Y. Han, J. Kong

Sponsorship: MIT DMSE and EECS, Rice University Materials Science and NanoEngineering, MIT Lincoln Laboratory

Graphene, the first member in the two-dimensional (2D) materials family, has unique electrical, optical, and mechanical properties, which opens vast opportunities for applications. The metal-graphene interface is crucial for many research studies and applications but has not been understood thoroughly due to the difficulty in characterizing it. Here we observed that when 8-15 nanometers of metal is deposited onto chemical vapor

deposition- (CVD) grown graphene, certain types of metal exhibit a change in optical contrast compared to the area without graphene underneath, but for others no such change is noticeable. In this work we carried out various investigations to understand the reasons behind the phenomena and explored their potential applications.

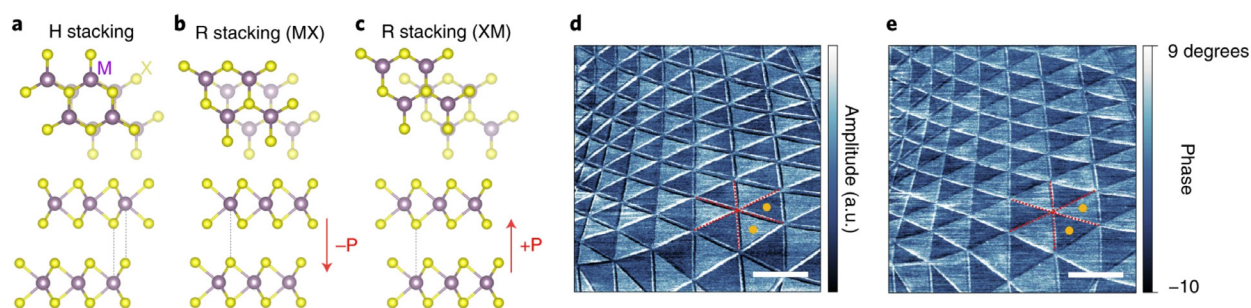
Interfacial Ferroelectricity in Rhombohedral-stacked Bilayer Transition Metal Dichalcogenides

X. Wang, K. Yasuda, Y. Zhang, S. Liu, K. Watanabe, T. Taniguchi, J. Hone, L. Fu, P. Jarillo-Herrero
Sponsorship: DoE, ARO, Gordon and Betty Moore Foundations, NSF

Two-dimensional (2D) ferroelectrics have great potential for dense and low-consumption nonvolatile memory applications. However, there are rare experimental reports due to the demand of layered polar bulk material. Van der Waals (vdW) materials enable the fabrication of heterostructures by stacking one layer of crystal on top of another at a controlled angle. These heterostructures combine characteristics of the individual building blocks but can also exhibit physical properties absent in the parent compounds through interlayer interactions and therefore can greatly expand the design space of 2D ferroelectrics.

Here we report on a new family of nanometer-thick, 2D ferroelectric semiconductors, in which the individual constituents are well-studied non-ferroelectric monolayer transition metal dichalcogenides (TMDs), namely WSe_2 , MoSe_2 , WS_2 , and MoS_2 . Specifically, we cut a monolayer TMD into two pieces and stack one half on top of the other

in parallel. This forms the rhombohedral-stacking (R-stacking) configuration different from the natural 2H phase. We demonstrate that robust out-of-plane ferroelectricity exists in such R-stacked bilayer TMDs, and the polarization can be flipped via in-plane sliding motion between the two monolayers. We visualize the ferroelectric domains as well as electric-field-induced domain wall motion with piezoelectric force microscopy. Furthermore, we probe the polarization switching of the bilayer via an adjacent graphene layer in a ferroelectric field transistor geometry and quantify the ferroelectric built-in interlayer potential, which is in good agreement with first-principles calculations. Our demonstration of ferroelectricity in stacking-engineered TMD bilayers consolidates the feasibility of engineering 2D ferroelectric semiconductors and opens up a broad way of engineering various functional heterostructures out of non-ferroelectrics.



▲ Figure 1: (a) H-stacked bilayer TMD. M, metal atom (W or Mo). X, chalcogen atom (S or Se), (b) MX and (c) XM stacking forms of R-stacked bilayer TMD, (d) amplitude and (e) phase images of vertical piezoelectric force microscopy (PFM) on twisted MoSe_2 . Scale bars, 200 nm.

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Electrical Switching of a Bistable Moiré Superconductor

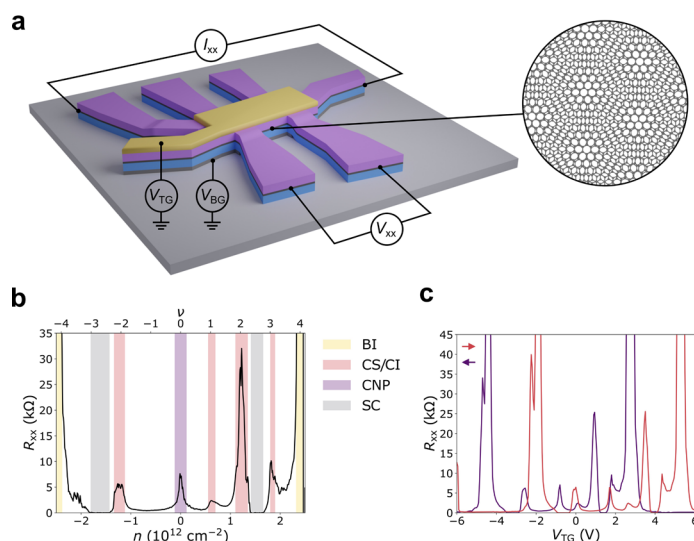
D. R. Klein, L.-Q. Xia, D. MacNeill, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero

Sponsorship: Air Force Office of Scientific Research, Army Research Office, Gordon and Betty Moore Foundation, NSF

Electrical control of superconductivity is critical for nanoscale superconducting circuits including cryogenic memory elements, superconducting field-effect transistors (FETs) and gate-tunable qubits. Superconducting FETs operate through continuous tuning of carrier density, but no bistable superconducting FET, which could serve as a new type of cryogenic memory element, has been reported.

Recently, experimentally realized magic-angle twisted bilayer graphene (MATBG) emerged as a highly-tunable platform for studying strongly correlated phenomena, including superconductivity, correlated insulators, orbital magnetism and anomalous Hall effect, and strange metal behavior. Separately, Bernal-stacked bilayer graphene aligned to its insulating hexagonal boron nitride gate dielectrics has been reported to manifest gate hysteresis and bistability. Here we report the observation of this

same hysteresis in MATBG with aligned boron nitride layers. This bistable behavior coexists alongside the strongly correlated electron system of MATBG without disrupting its correlated insulator or superconducting states (see Figure 1). This all-van der Waals platform enables configurable switching between different electronic states of this rich system. To illustrate this new approach, we demonstrate reproducible bistable switching between the superconducting, metallic, and correlated insulator states of MATBG using gate voltage or electric displacement field. The combination of these results with other configurable MATBG superconducting devices, including Josephson junctions and superconducting quantum interference devices, will enable an additional control knob over the electronic states and pave the way for a new generation of switchable moiré graphene superconducting electronics.



▲ Figure 1: a. Schematic of the MATBG device. b. Measured longitudinal resistance R_{xx} . The band insulators (BI), correlated semimetals/insulators (CS/CI), charge neutrality point (CNP) and superconductivity (SC) regions are highlighted. c. Hysteresis of R_{xx} versus applied top gate voltage V_{TG} depending on gate sweep direction.

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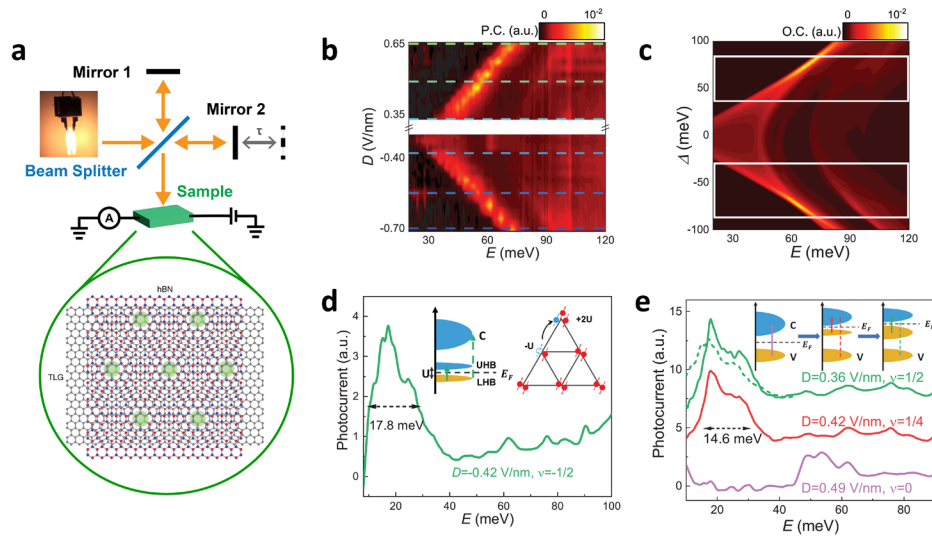
Spectroscopy Signatures of Electron Correlations in a Trilayer Graphene/hBN Moiré Superlattice

J. Yang, G. Chen, T. Han, Q. Zhang, Y.-H. Zhang, L. Jiang, B. Lyu, H. Li, K. Watanabe, T. Taniguchi, Z. Shi, T. Senthil, Y. Zhang, F. Wang, L. Ju

Sponsorship: Center for Integrated Quantum Materials, NSF Grant No. DMR1231319

Two-dimensional (2D) materials, since their discovery in 2005, have attracted great interest among scientists. Specifically, the idea of creating a moiré superlattice by stacking 2D materials vertically allows people to combine the properties of various 2D materials and to manipulate the electrons via electrostatic gating, making it a great platform to study exotic physics phenomena. Among them, rhombohedral- (ABC) stacked trilayer graphene/hexagonal boron nitride moiré superlattice (ABC-TLG/hBN) has been found to be a promising system since it has large tunability and is free of twisting angle disorders. People have observed correlated insulator, superconductivity, and topological state in transport studies. In contrast, the spectroscopic study of ABC-TLG/hBN is still absent, mainly due to the size-mismatch between device dimension (typically $\sim 10 \mu\text{m}$) and wavelength (30-100 μm), which makes the signal-to-noise ratio very small. In this work, we report spectroscopy measurements of dual-gated ABC-

TLG/hBN using a special Fourier-transform infrared (FTIR) photocurrent spectroscopy method. We observe a strong optical transition between moiré minibands that narrow continuously as we increase the band-gap via electrostatic gating, indicating a reduction of the single-particle bandwidth. At half-filling of the valence flat band, a broad absorption peak emerges at ~ 18 milli-electron volts, representing the direct optical excitation across an emerging Mott gap. Similar photocurrent spectra are obtained in two other emerging correlated insulating states at quarter- and half-filling of the first conduction band at finite magnetic field. Our work is the very first spectroscopic study of an ABC-TLG/hBN system and provides key parameters of the Hubbard model to understand electron correlation. Further, this technique can be applied to many other graphene-based moiré systems that also lack spectroscopic studies and provides more insights into many exotic physics phenomena.



▲ Figure 1: (a) Illustration of FTIR photocurrent spectroscopy and ABC-TLG/hBN superlattice. (b) Experimental results and (c) calculations of charge-neutral point photocurrent spectra at different displacement fields, where the narrowing of inter-band transition peaks indicates suppressing of bandwidth W . (d) First direct measurement of on-site interaction U via photocurrent spectra at half-filling. (e) Spectra at correlation gaps at quarter- and half-filling at finite magnetic field.

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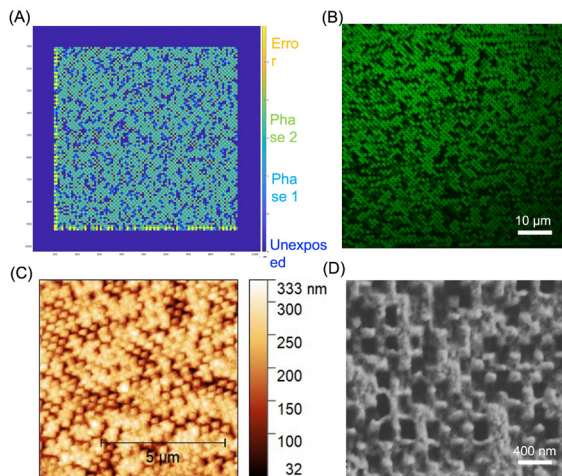
Nanofabrication of Metasurface Structures for Holography, Using Laser Ablation-based Implosion Fabrication

G. Yang, Q. Yang, T. Nambara, Y. Kunai, Y. Salamin, M. Soljačić, P. T. C. So, E. S. Boyden
Sponsorship: Fujikura Corp.

Nanofabrication techniques have advanced the development of precise optical components for various fields, including imaging, sensing, and communication. We present a laser ablation-based implosion fabrication technique for constructing metasurface structures with nanoscale precision for holography and diffractive optical element (DOE) applications. Our process utilizes a two-photon laser to activate photosensitizers, breaking polymer chains to create topological nanostructures and metasurfaces with varying height gradients. We designed a phase mask metasurface transmitting light with varying thicknesses, generating phase changes with three quantization levels. The implosion fabrication method built intricate, free-form three-dimensional (3D) architectures with nanometer precision. We obtained multiple layers of diffractive structures with varying refractive indices (RI) by adjusting the thickness of patterned structures. Comparing the designed mask and fluorescent image of the patterned region (Figure 1a, b) showed high correlation in vox-

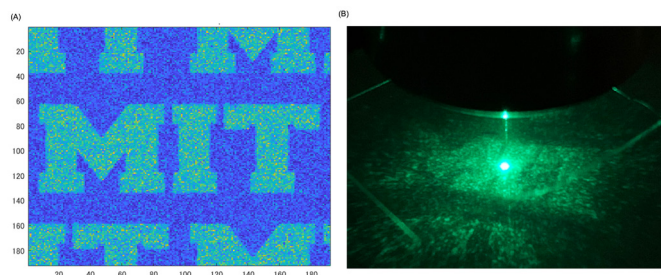
el unit distribution and precision. Scanning electron microscopy and atomic force microscopy (AFM) confirmed successful construction of metasurface structures with varying height gradients (Figure 1c, d), each unit with a feature size of 200-250 nm and height gradient difference of 100 nm.

Using coherent light, the metasurface generated a far-field diffraction pattern reconstructing the MIT logo with high contrast, resolution, and minimal aberrations (Figure 2). The fabricated metasurface structures can produce far-field diffraction hologram effects when illuminated with a monochromatic light source. Our innovative laser ablation-based implosion fabrication technique has the potential to create personalized DOEs with nanoscale 3D structural accuracy and full-color 3D visual effects. This breakthrough holds tremendous promise for revolutionizing the field of holography and creating opportunities in the development of advanced optical devices.



◀ Figure 1: A) The designed mask of different levels; B) Fluorescent image of a plane of the patterned layer; C) AFM image and D) AFM image of the metasurface.

▼ Figure 2: A) The simulated image of reconstructed MIT logo; B) The far-field diffraction effect, displayed as the MIT logo.



FURTHER READING

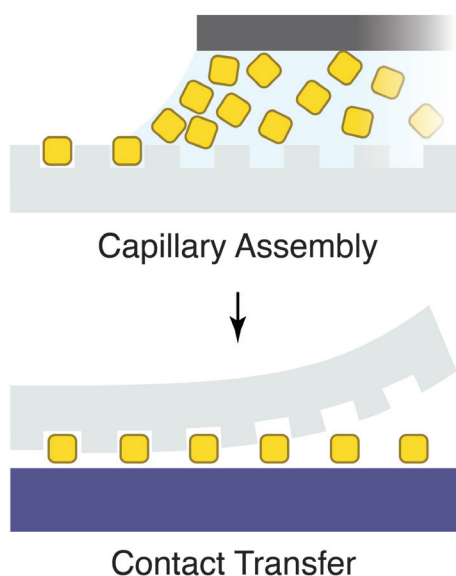
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Contact Printed Nanoparticles as Building Blocks for Active Nanodevices

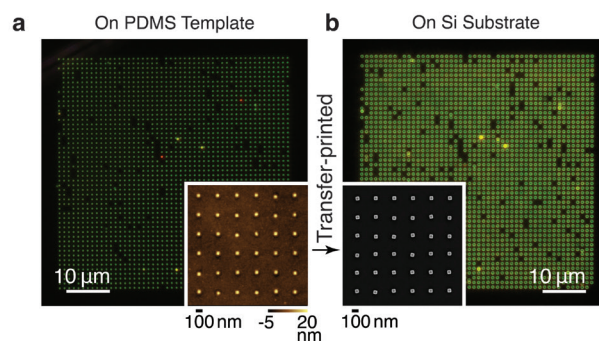
W. Zhu, P. F. Satterthwaite, P. Jastrzebska-Perfect, R. Brenes, F. Niroui
Sponsorship: NSF Award CMMI-2135846

Nanoparticles, efficiently formed through bottom-up synthesis with diverse composition, structure, and functionalities, exhibit unique properties compared to their top-down fabricated counterparts. Leveraging these properties requires deterministic patterning of nanoparticles with the desired spatial order. Here, we present a versatile, scalable, and pristine approach for deterministic integration of nanoparticles into active structures and devices with single-particle resolution. Our approach, named nanoparticle contact printing, first spatially assembles nanoparticles into a topographical template, and then prints them onto diverse surfaces and interfaces. By engineering interfacial interactions, our approach promotes high-yield nanoparticle transfer without requiring solvents,

surface treatments, or sacrificial layers as is conventionally needed. With our approach, surfaces remain pristine and are accessible for integration into functional structures. We demonstrate this through a particle-on-mirror plasmonic cavity model system, where >2000 gold nanocubes are deterministically patterned onto template-stripped gold with sub-50 nm positional accuracy and minimized inter-structural variability. We further highlight the integration opportunities offered by our technique by fabricating arrays of emitter-coupled nanocavities. In addition, we use this platform to demonstrate mechanically active molecular junctions with sub-nm tunability as building blocks of miniaturized nanoelectromechanical sensors and actuators.



▲ Figure 1: Schematic overview of nanoparticle contact printing: nanoparticles are assembled onto topographical template through capillary assembly, followed by contact transfer onto receiving substrate.



▲ Figure 2: (a) Dark-field image of assembled 50 x 50 array of individual gold nanocubes, with AFM image inset highlighting assembled nanocubes. (b) Dark-field image of nanocube array after contact transfer onto Si substrate, with SEM image inset showing transferred nanocubes.

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Quantum Science and Engineering

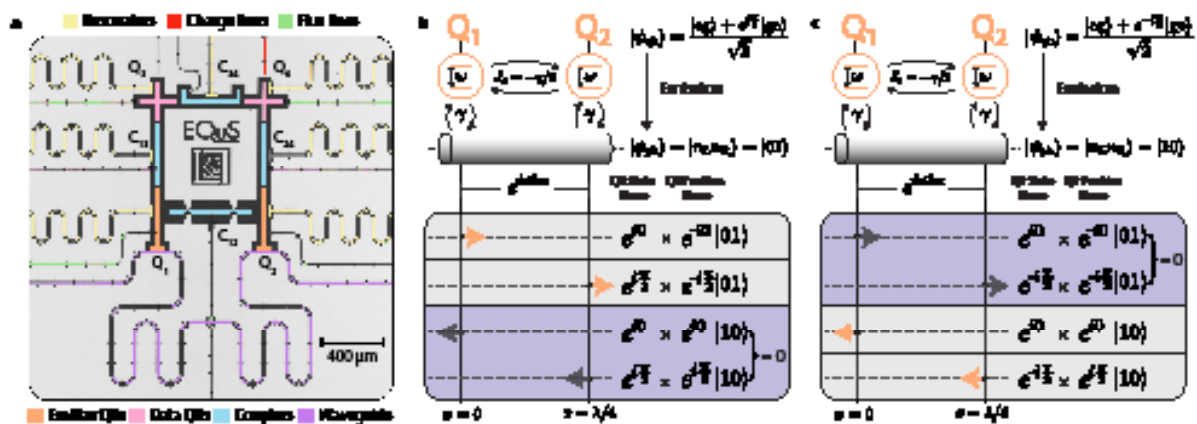
Emitting and Absorbing a Directional Microwave Photon with Waveguide Quantum Electrodynamics.....	107
Integrated Photonics for Advanced Cooling of Trapped-ion Quantum Systems	108
Frequency Multiplexing of Cryogenic Sensors for the Ricochet Experiment.....	109
QOC: Quantum On-chip Training with Parameter Shift and Gradient Pruning.....	110

Emitting and Absorbing a Directional Microwave Photon with Waveguide Quantum Electrodynamics

A. Almanakly, B. Yankelevich, B. Kannan, A. Di Paolo, A. Greene, B. M. Niedzielski, K. Serniak, M. E. Schwartz, J. L. Yoder, J. I.-J. Wang, T. P. Orlando, S. Gustavsson, J. A. Grover, W. D. Oliver
 Sponsorship: Amazon Web Services Center for Quantum Computing, DoD, USARO, DoE Office of Science - National Quantum Information Science

Routing quantum information between non-local computational nodes is a foundation for extensible networks of quantum processors. Propagating photons are efficient carriers of quantum information. In this work, we develop a quantum interconnect composed of an emitter, receiver, and propagation channel. We demonstrate high-fidelity directional microwave photon emission with quantum interference using an ar-

tificial molecule comprising two superconducting qubits strongly coupled to a bidirectional waveguide. By emitting time-symmetric photons from one module, we operate another identical module tiled along the waveguide as an absorber of photons, developing an interconnect capable of hosting remote entanglement for extensible quantum networks.



▲ Figure 1: a) A false-colored optical micrograph of the device. b) Schematic outlining the quantum interference effect that enables the emission of a rightward-propagating photon in the waveguide. c) Same as b) but for a leftward-propagating photon.

Integrated Photonics for Advanced Cooling of Trapped-ion Quantum Systems

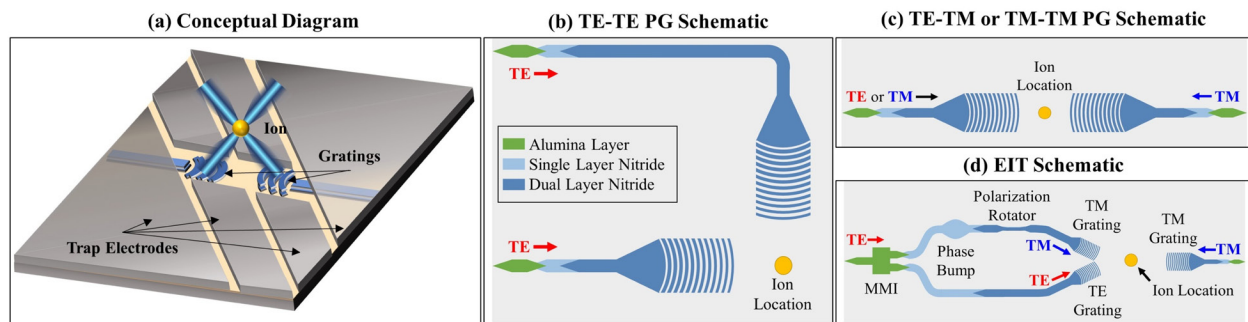
A. Hattori*, S. Corsetti*, T. Sneh, M. Notaros, R. Swint, P. T. Callahan, C. D. Bruzewicz, F. Knollmann, R. McConnell, J. Chiaverini, J. Notaros

Sponsorship: NSF Quantum Leap Challenge Institute Hybrid Quantum Architectures and Networks, NSF Quantum Leap Challenge Institute Quantum Systems through Entangled Science and Engineering, MIT Center for Quantum Engineering, NSF Graduate Research Fellowship, MIT Cronin Fellowship, MIT Locher Fellowship

Trapped-ion systems are a promising modality for quantum information processing due to their long coherence times and strong ion-ion interactions, which enable high-fidelity two-qubit gates. However, most current implementations are comprised of complex free-space optical systems, whose large size and susceptibility to vibration and drift can limit fidelity and addressability of ion arrays, hindering scaling. Integrated-photonics-based solutions offer a potential avenue to address many of these challenges.

Motional state cooling is a key optical function

in trapped-ion systems. However, to date, integrated-photonics-based demonstrations have been limited to Doppler and resolved-sideband cooling. In this work, we develop integrated-photonics-based system architectures and design key transverse-electric (TE) and transverse-magnetic (TM) integrated devices for two advanced cooling schemes, polarization gradient (PG) and electromagnetically-induced-transparency (EIT) (Figure 1). These systems improve cooling performance for trapped ions, enabling scalable quantum systems.



▲ Figure 1: (a) Conceptual diagram of the integrated PG-cooling system. Simplified schematics showing the proposed integrated-photonics-based architectures for (b) TE-TE PG cooling, (c) TE-TM or TM-TM PG cooling, and (d) EIT cooling (not to scale).

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Frequency Multiplexing of Cryogenic Sensors for the Ricochet Experiment

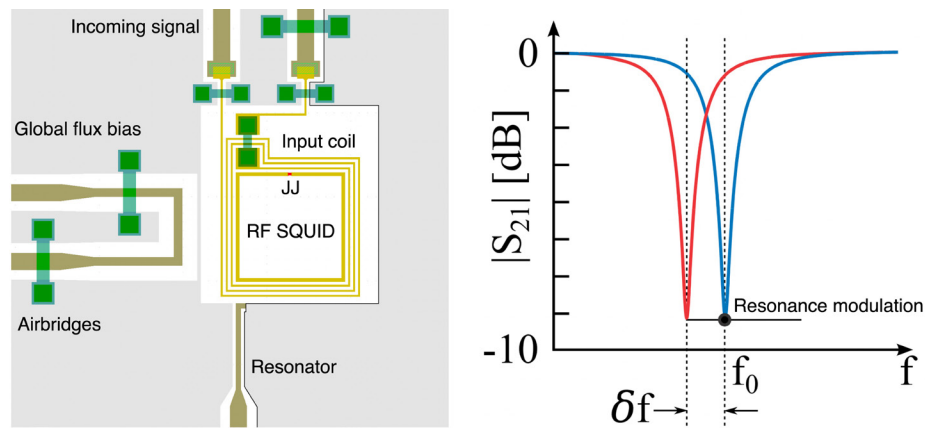
W. Van De Pontseele, J. Yang, P. Harrington, S. Weber, S. Henderson, W. D. Oliver, J. Formaggio
Sponsorship: DOE QuantISED Award DE-SC0020181, Heising-Simons Foundation

Readout of weak microwave signals over a wide bandwidth is increasingly important for fundamental science. The high frequency allows multiplexing detectors and reduces low-frequency noise for experiments such as Ricochet.

Ricochet aims to measure coherent neutrino scattering to search for new physics. It consists of superconducting crystals that function as bolometers and are read out using transition-edge sensors.

We designed and characterised devices

for frequency multiplexing in 6 and 18-channel configurations with Lincoln Laboratory. The signals inductively couple into RF SQUIDS that modulate the resonant frequency of aluminium resonators. These high-Q resonators connect to a common RF feedline, reducing cabling and heat loads. The low-frequency signals are recovered using SLAC Microresonator Radio Frequency (SMuRF) electronics for read out of frequency-division-multiplexed cryogenic sensors.



▲ Figure 1: (left) Schematic of a single RF SQUID of the 18-resonator chip. The scale of the inner SQUID loop is 60x60 micron. Fabricated at Lincoln Laboratories using Al-AIOx-Al trilayer process. (right) Effect of an incoming current on the resonant frequency.

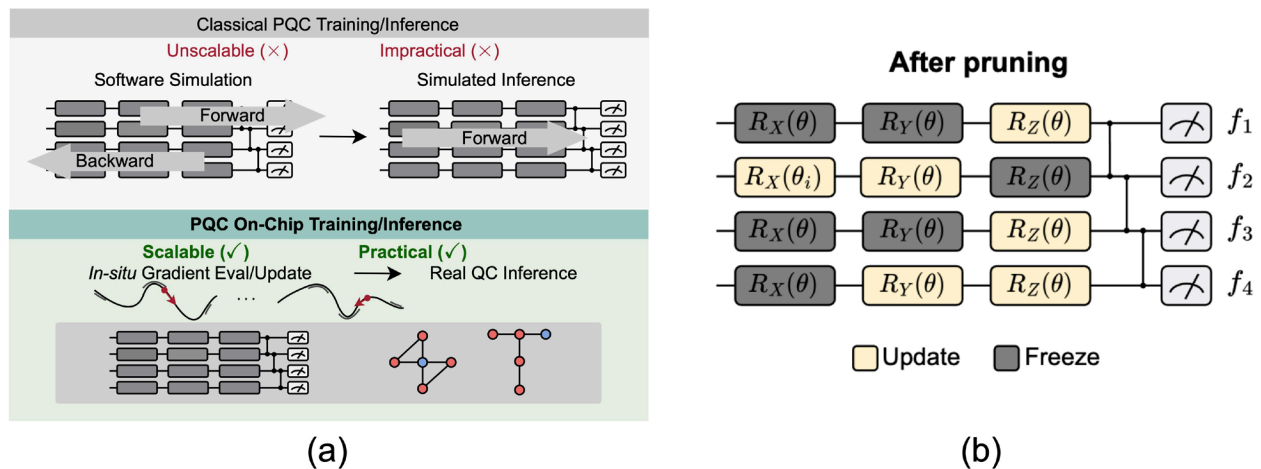
QOC: Quantum On-chip Training with Parameter Shift and Gradient Pruning

H. Wang, Z. Li, J. Gu, Y. Ding, D. Z. Pan, S. Han

Sponsorship: MIT-IBM Watson AI Lab, NSF CAREER Award, Qualcomm Innovation Fellowship

Parameterized quantum circuits (PQC) are drawing increasing research interest thanks to their potential to achieve quantum advantages on near-term noisy intermediate scale quantum (NISQ) hardware. In order to achieve scalable PQC learning, the training process needs to be offloaded to real quantum machines instead of using exponential-cost classical simulators. One common approach to obtain PQC gradients is parameter shift, whose cost scales linearly with the number of qubits. We present QOC, the first experimental demonstration of practical on-chip PQC training with parameter shift. Nevertheless, we find that due to the significant quantum errors (noises) on real machines, gradients obtained from naive parameter shift have low fidelity and thus degrade the training accuracy. To this end, we further propose probabilistic gradient pruning

to first identify gradients with potentially large errors and then remove them. Specifically, small gradients have larger relative errors than large ones, thus having a higher probability to be pruned. We perform extensive experiments with the quantum neural network (QNN) benchmarks on 5 classification tasks using 5 real quantum machines. The results demonstrate that our on-chip training achieves over 90% and 60% accuracy for 2-class and 4-class image classification tasks, respectively. The probabilistic gradient pruning brings up to 7% PQC accuracy improvements over no pruning. Overall, we successfully obtain similar on-chip training accuracy compared with noise-free simulation but have much better training scalability. The QOC code is available in the TorchQuantum library.



▲ Figure 1: (a) In QOC, PQC training and inference are both performed on real quantum machines, making the whole pipeline scalable and practical. (b) Gradients are probabilistically pruned with a ratio in the pruning window to mitigate noises and stabilize training.

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Semiconductor Manufacturing and Supply Chain

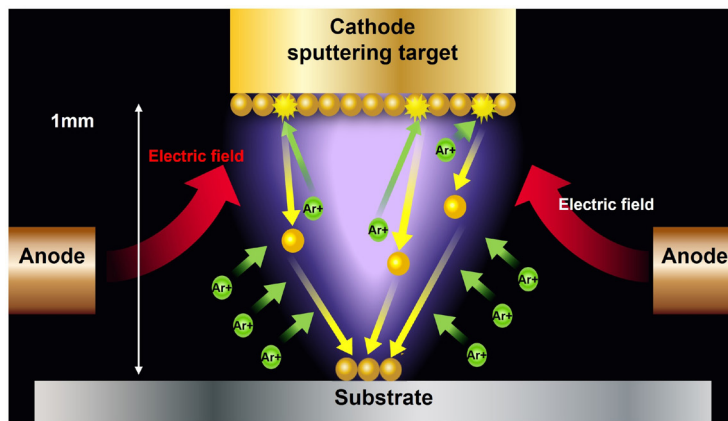
Plasma Microsputtered Materials for Agile Manufacturing of Electronics and Microsystems	112
One-class Anomaly Detection Using Kernel Density Estimation Methods for Semiconductor Fabrication Processes.....	113
Diffractive-optical Microlenses for Maskless Photolithography.....	114
Sub-micron Defect-free and Freestanding Microporous Poly(Arylene Ether) Thin Films for Membrane-based Gas Separations	115

Plasma Microsputtered Materials for Agile Manufacturing of Electronics and Microsystems

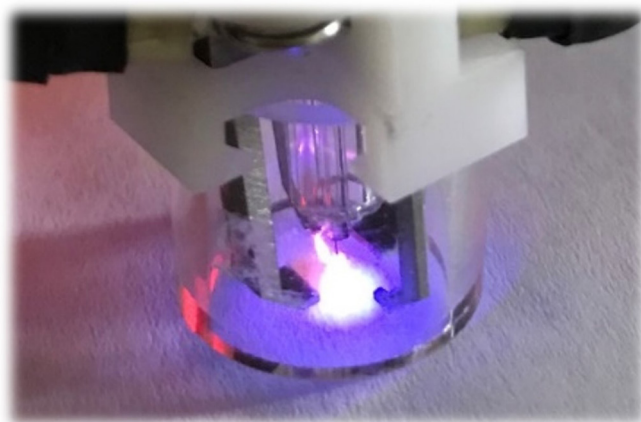
N. Lubinsky, L. Parameswaran, R. Mathews, L. M. Racz, L. F. Velásquez-García
Sponsorship: Kansas City National Security Campus

Agile manufacturing of electronics and microsystems could benefit from and be enabled by additive manufacturing technology capable of depositing high-quality thin films in non-planar, temperature-sensitive surfaces. Our approach utilizes a direct current (DC) microplasma generated at ambient temperature and pressure, obviating the need of a vacuum. Using a three-dimensional stage that rasters the microsputterer head across space, freeform planar structures made of high-quality materials can be deposited on non-planar surfaces. Moreover, using a multi-material sputtering head can monolithically fabricate objects that attain complex functionalities.

The basic functionality of the DC microsputterer is shown in Figure 1, where 4 electrodes help guide ions to a narrowly defined region while argon gas flow sustains the plasma. Additionally, the laminar gas flow works to further constrain the sputtered material into thin trace films, as ions collide and interact with the fluidic forces at work, collectively driving “ionic drag” that acts as a net focusing effect. This can be seen in the synthesized, additively manufactured sputter head in action shown in Figure 2. Current efforts focus on synthesizing the next generation of microsputtering write heads and conducting simulations to improve deposition yield and explore new modes of operation.



◀ Figure 1: Conceptual schematic of microsputtering head using gold wire as feedstock. The combination of electric fields and laminar gas flow helps project and focus the sputtered material onto printing surface. Adapted from Kansas City National Security Printed Electronics Consortium Proceedings.



◀ Figure 2: Picture of microplasma printer head generating gold trace on paper substrate. Adapted from Kansas City National Security Printed Electronics Consortium Proceedings.

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One-class Anomaly Detection Using Kernel Density Estimation Methods for Semiconductor Fabrication Processes

R. Owens, F.-K. Sun, C. Lang, B. Lawler, D. S. Boning
Sponsorship: Analog Devices, Inc.

In semiconductor fabrication processes, undetected faults can be extremely costly. Machine learning has allowed for advances in fault detection and classification, but there are still difficulties in applying these techniques to the monitoring of fabrication processes. Concept drift, infrequency of faults, and differences between processes, tools, and recipes all present challenges distinct to the semiconductor industry.

In this work, we present a one-class time series anomaly detection method that uses univariate sensor data to detect faults in semiconductor fabrication processes. The proposed method uses kernel density estimation (KDE) to create probability distributions for nominal process runs. Incoming sensor data can then be compared to these trained distributions to determine the likelihood that the new signal is nominal or anomalous. Critically, the use of a first-in, first-

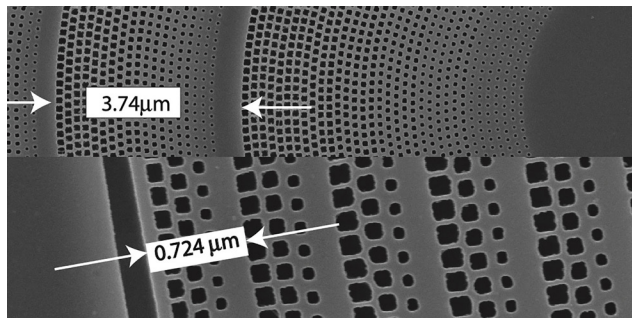
out queue for creating the probability distributions allows for the model to adapt to new conditions, thus overcoming the challenge of concept drift. The KDE method can be combined with techniques for transfer learning, which enables startup of the anomaly detector with as little as 25 previous process runs. This allows for model information to be transferred between similar tools or recipes, even ones that are used infrequently. We also consider the use of dynamic time warping to improve the accuracy of the sensor probability distributions. The proposed KDE methods are tested on historical data from plasma etch and ion implantation processes, outperforming benchmark methods including traditional statistical process control (SPC), one-class support vector machine (OC-SVM), and variational auto-encoder (VAE) based detectors.

Diffraction-optical Microlenses for Maskless Photolithography

H. I. Smith, M. Mondol, F. Zhang, T. Savas, M. Walsh
Sponsorship: LumArray, Inc.

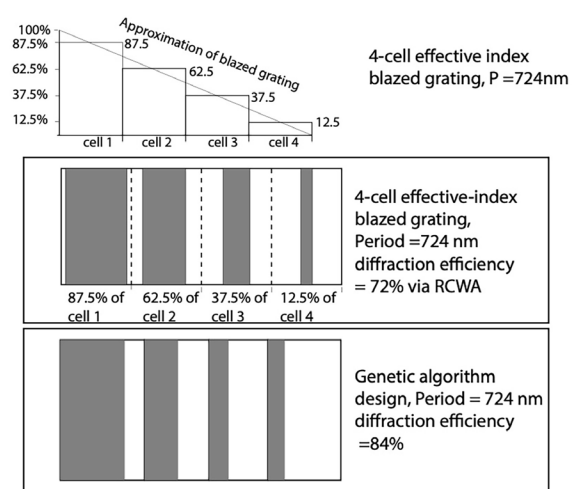
Maskless lithography plays an important role in nanostructures research by avoiding the delay and cost of mask manufacture. Maskless photolithography, using an array of diffraction-optical microlenses, offers the additional advantages of full-wafer areas and long-range spatial-phase coherence, a feature that is essential in photonic and other advanced applications. To improve the focal efficiency and resolution beyond that of the binary pi-phase zone plates currently employed and to exceed the depth-of-focus characteristic of classical lenses, diffraction-optical microlenses (also called metalenses) each 135 microns in diameter and operating at 405 nm wavelength are investigated theoretically and experimentally. A microlens is first divided into Fresnel zones, across which the effective index-of-refraction is modulated by forming appropriate pillars or holes such that beams diffracted from the zones interfere constructively at the focal spot, located 100 microns in front of the microlens plane.

The diffraction efficiency of each zone is evaluated using rigorous coupled-wave analysis (RCWA). A genetic algorithm is then used to determine if higher efficiency can be achieved by repositioning of the pillars or their widths. MEEP software is used to predict focal efficiency of the complete microlens. Scanning-electron-beam lithography was used to fabricate effective-index-modulated metalenses in CSAR-62 e-beam resist. Focal efficiencies up to 54% were achieved, a significant increase over zone plates. However, problems with stability and dimensional control favor reactive-ion etching over direct exposure. In a dielectric of 1.9 index, the maximum height-to-width ratio is about 10-to-1. Theoretical models and experimental results indicate that extreme precision in fabrication, on the order of 10 nm, well below the 213 nm wavelength within the dielectric, is needed to achieve theoretical expectations.



► Figure 2: (upper and middle) Schematics of linearly varying refractive index by effective-index modulation across 4 sub-wavelength cells. (lower) Genetic algorithm maximizes diffraction efficiency by adjusting widths and locations of pillars specified by effective-index model, illustrating necessity of precision control of dimensions and lateral position to achieve maximum efficiency and lowest background.

◄ Figure 1: Scanning-electron micrograph of hole-based effective-index modulation: (upper) central zone (9 micron radius) and next zone (3.74 micron width). (lower) outer 5 zones. Dielectric was electron beam resist (CSAR-62) with refractive index of 1.59. Maximum focal efficiency of 54% was measured.



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Sub-micron Defect-free and Freestanding Microporous Poly(Arylene Ether) Thin Films for Membrane-based Gas Separations

J. Y. Yeo, G. Sheng, F. M. Benedetti, D. Syar, T. M. Swager, Z. P. Smith
Sponsorship: ENI, Office of Naval Research – Young Investigator Program (ONR-YIP)

Membrane-based gas separations are viewed as a critical component to accessing low-energy feedstocks and decarbonizing the chemical industry. However, it is exceedingly challenging to synthesize membrane materials that are high performing, scalable, and processable especially at the nanometer scale. It requires the polymer to have a high molecular weight while still being soluble in organic solvents. As a class of materials, microporous organic polymers (MOPs) have been attracting significant attention for membrane-based gas separations due to their high gas permeability as compared to current commercial polymers. For this project, we present the rational design and synthesis of a new class of linear microporous poly(arylene ether)s (PAEs) via Pd-catalyzed C-O polymerization reactions. The scaffold of these new microporous polymers consists of rigid three-dimensional triptycene and highly stereocontorted spirobifluorene, which endow these

polymers with large internal free volume as well as high porosity with angstrom-sized pores. Unlike classic polymers of intrinsic microporosity (PIMs), this robust methodology for the synthesis of poly(arylene ether)s allows for the facile incorporation of functionalities and branched linkers for control of permeation and mechanical properties. This allowed for the fabrication of a submicron defect-free film with permeance-selectivity property sets that are comparable to high-performance ultrathin polymer membranes reported in the literature. The structural tunability, high physical stability, and ease-of-processing suggest that this new platform of microporous polymers provide generalizable design strategies to address outstanding separation challenges for gas separation membranes.

Research Centers

Center for Integrated Circuits and Systems 117

MIT/MTL Center for Graphene Devices and 2-D Systems..... 118

The MIT Medical Electronic Device Realization Center 119

Center for Integrated Circuits and Systems

Associate Professor Ruonan Han, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Eight faculty members participate in the CICS: Director Ruonan Han, Hae-Seung (Harry) Lee, Anantha Chandrakasan, Song Han, David Perreault, Negar Reiskarimian, Charles Sodini, and Vivienne Sze.

CICS investigates circuits and systems for a wide range of applications, including artificial intelligence, wireless/wireline communication, sensing, security, biomedicine, power conversion, quantum information, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of

holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. The meeting also serves as a valuable networking event for both participants and students. Closer technical interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

MIT/MTL Center for Graphene Devices and 2-D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) brings together MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional (2-D) materials.

Two-dimensional materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of. At the same time that they have extremely rich electronic and chemical properties. MIT has been leading research on the science and engineering of 2-D materials for more than 40 years. Since 2011, the MIT/MTL Center for Graphene Devices and 2-D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced

technologies and strategies that enable 2-D materials, devices, and systems to provide discriminating or breakthrough capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials to optoelectronics, RF communications, and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools, and analysis for the creation of a vision for the future of new systems enabled by 2-D materials.

Some of the many benefits of the Center's membership include complimentary attendance to meetings, industry focus days, and live webcasting of seminars related to the main research directions of the Center. Our industrial members also gain access to a resume book that connects students with potential employers, as well as access to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices, and systems.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Co-Director
Brian Anthony, Co-Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will, in turn, transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personalized medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personalized medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication, and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, Medical Electronic Devices.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacturing devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure, and cerebral blood flow velocity. MEDRC has 4 sponsoring companies, 8 faculty members, 12 active projects, and approximately 15 students. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT's Institute for Medical Engineering and Science (IMES) that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

Faculty Profiles

Akintunde I. (Tayo) Akinwande	121
Dimitri A. Antoniadis.....	122
Marc A. Baldo	123
Duane S. Boning.....	124
Edward S. Boyden	125
Vladimir Bulović	126
Anantha P. Chandrakasan.....	127
Yufeng (Kevin) Chen	128
Riccardo Comin.....	129
Jesús A. del Alamo.....	130
Luca Daniel.....	131
Dirk R. Englund.....	132
Jongyoon Han	133
Ruonan Han.....	134
Song Han.....	135
Juejun (JJ) Hu	136
Qing Hu	137
Rafael Jaramillo	138
Pablo Jarillo-Herrero.....	139
Long Ju.....	140
Jeehwan Kim.....	141
Jing Kong.....	142
Jeffrey H. Lang.....	143
Hae-Seung Lee.....	144
Luqiao Liu.....	145
Scott R. Manalis.....	146
Farnaz Niroui	147
Jelena Notaros	148
William D. Oliver.....	149
Tomás Palacios	150
David Perreault	151
Carlos M. Portela.....	152
Negar Reiskarimian.....	153
Charles G. Sodini	154
Vivienne Sze.....	155
Carl V. Thompson	156
Luis Fernando Velásquez-García	157

Akintunde I. (Tayo) Akinwande

Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

Empty space electronics. Nano vacuum channel transistors. Chip scale electron, ion, neutron and x-ray sources for imaging and sensing. Micro and nano structures for charged particle beams.

Rm. 39-553 | 617-258-7974 | akinwand@mit.edu

GRADUATE STUDENTS

Nedeljko Karaulac, EECS
Álvaro Sahagún, EECS
Youngjin Shin, EECS

UNDERGRADUATE STUDENT

Alyssa Keirn, EECS

SUPPORT STAFF

Maria Markulis, Administrative Assistant

SELECTED PUBLICATIONS

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Dimitri A. Antoniadis

Ray and Maria Stata Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

Research is in the field of nanoscale solid-state electronic devices and the application of new materials systems and new structures to transistors for deeply scaled electronics.

Rm. 39-427a | 617-253-4693 | daa@mit.edu

GRADUATE STUDENTS

Taekyong Kim, EECS

SUPPORT STAFF

Elizabeth Green, Sr. Administrative Assistant

SELECTED PUBLICATIONS

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Marc A. Baldo

Director, Research Laboratory of Electronics
Dugald C. Jackson Professor
Department of Electrical Engineering & Computer Science

Spin and Excitonic Electronics Group: organic & molecular electronics, LEDs and solar cells, spintronics.

13-3053 | 617-452-1532 | baldo@mit.edu

POSTDOCTORAL ASSOCIATES

Kangmin Lee, EECS

GRADUATE STUDENTS

Dooyong Koh, EECS

Aaron Li, Chemistry

Brooke McGoldrick, EECS

Oliver Morgan Nix, Chemistry

Collin Fisher Perkinson, Chemistry

Jaekang Song, EECS

Jan Tjepelt, EECS

Narumi Wong, Chemical Engineering, Mathworks
fellow

SUPPORT STAFF

Catherine Bourgeois, Program Manager

SELECTED PUBLICATIONS

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Duane S. Boning

Clarence J. LeBel Professor of Electrical Engineering
Professor of Electrical Engineering & Computer Science,
Department of Electrical Engineering & Computer Science

Design for manufacturability of processes, devices, and circuits. Understanding and reduction of variation in semiconductor, photonics and MEMS manufacturing, emphasizing statistical, machine learning, and physical modeling of spatial and operating variation in circuits, devices, and CMP, electroplating, spin coating, etch, and embossing processes.

Rm. 39-415a | 617-253-0931 | boning@mtl.mit.edu

COLLABORATORS

Emmanuel Bender, MTL Research Affiliate
Jinwoo Park, MTL Visiting Scientist

GRADUATE STUDENTS

Christian Allinson, EECS and Sloan
Uttara Chakraborty, EECS
Farri Gaba, EECS and TPP
Zhengqi Gao, EECS
Andrew Lai, EECS
Rachel Owens, EECS
Colin Poler, EECS and Sloan
Fan-Keng Sun, EECS
Andrew Tindall, EECS and Sloan
Peter Tran, EECS
Zhengxing Zhang, EECS

SUPPORT STAFF

Jami L. Mitchell, Administrative Assistant

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Edward S. Boyden

Y. Eva Tan Professor in Neurotechnology at MIT

Co-Director, Center for Neurobiological Engineering, K Lisa Yang Center for Bionics, Departments of Brain and Cognitive Sciences, Media Arts and Sciences, Biological Engineering, McGovern Institute and HHMI

Developing, and applying, tools that enable the mapping of the molecules and wiring of the brain, the recording and control of its neural dynamics, and the repair of its dysfunction.

Rm. 46-2171C | 617-324-3085 | edboyden@mit.edu

RESEARCH SCIENTISTS AND STAFF

Adam Amsterdam, McGovern
Bobae An, McGovern
Giovanni Talei Franzesi, McGovern
Debarati Ghosh, McGovern Konstantinos Kagias, McGovern
Youngmi Lee, McGovern
Kylie Leung, McGovern
Demian Park, McGovern
Brett Pryor, McGovern
Sara Tavana, McGovern
Doug Weston, McGovern
Aimei Yang, McGovern
Eunah Yu, McGovern
Chi Zhang, McGovern
Jian-Ping Zhao, McGovern

Anubhav Sinha, HST
Michael Skuhersky, BCS
Corban Swain, BE
Shiwei Wang, Chemistry
Zeguan Wang, MAS
Lige (Caroline) Zhang, MAS
Ruihan Zhang, MAS

SUPPORT STAFF

Ally Bassile-McCarthy, Administrative Assistant
Macey Lavoie, Administrative Assistant
Lisa Lieberman, Senior Administrative Assistant
Fira Zainal, Financial Assistant

POSTDOCTORAL ASSOCIATES

Shahar Bracha, McGovern
Alexi Georges Choueiri, McGovern
Nava Shmoel David, McGovern
Jinyoung Kang, McGovern
Yangning Lu, McGovern
Yong Qian, McGovern
Sapna Sinha, McGovern
Panagiotis (Panos) Symvoulidis, McGovern
Hao Wang, McGovern
Guang Xu, McGovern
Gaojie Yang, McGovern
Quansan Yang, McGovern

SELECTED PUBLICATIONS

C. Linghu, B. An, M. Shpokayte, O. T. Celiker, N. Shmoel, R. Zhang, C. Zhang, D. Park, W. M. Park, S. Ramirez, and E. S. Boyden, "Recording of Cellular Physiological Histories Along Optically Readable Self-Assembling Protein Chains," *Nat Biotechnol.* doi: 10.1038/s41587-022-01586-7. Jan. 2. 2023. Online ahead of print.

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GRADUATE STUDENTS

Nick Barry, MAS
Jeffrey Brown, EECS
Amauche Emenari, BCS
Kettner Griswold, MAS
Nathan Han, EECS
Jordan Harrod, HST
Helena Hu, BE
Brennan Jackson, HST
Daniel Leible, BCS
Yixi Liu, EECS
Victoria Long, EECS
Camille Mitchell, BCS
Mitchell Murdock, BCS
Cipriano Romero, EECS
Catherine Marin Della Santina, BE
Margaret Elizabeth Schroeder, BCS
Jiuhan Shi, BCS
Tay Won Shin, MAS

Vladimir Bulović

MIT.nano Director

Fariborz Maseeh (1990) Professor of Emerging Technology
Department of Electrical Engineering and Computer Science

Physical properties of nanostructured materials and composite structures and their use in development of electronic, excitonic, optical, and nano-mechanical devices. Applications of nanostructures in large-scale technologies.

Rm. 13-3138 | 617-253-7012 | bulovic@mit.edu

RESEARCH SCIENTISTS

Jeremiah Mwaura, RLE

Annie Wang, RLE

POSTDOCTORAL ASSOCIATES

Benjia Dak Dou, RLE

Jun Guan, RLE

Jinchi Han, RLE

Richard Swartwout, RLE

GRADUATE STUDENTS

Roberto Brenes, EECS, NSF Fellow

Tori Dang, EECS

Jamie Geng, EECS

Tamar Kadosh, DMSE

Madeliene Laitz, EECS, NSF Fellow

Brendan Motes, MEng

Mayuran Saravanapavanantham, EECS, NSF Fellow

Shreyas Srinivasan, Chemistry

Ella Wassweiler, EECS, NSF Fellow

Ruiqi Zhang, EECS

Karen Yang, EECS, McWhorter Fellow

J. Shi, D. Yoo, F. Vidal-Codina, C. W. Baik, K. S. Cho, N. C. Nguyen, H. Utzat, J. Han, A. M. Lindenberg, V. Bulović, M. G. Bawendi, J. Peraire, S.-H. Oh, and K. A. Nelson, "A Room-temperature Polarization-sensitive CMOS Terahertz Camera Based on Quantum-dot-enhanced Terahertz-to-visible Photon Upconversion," *Nature Nanotechnology*, 17, 1288–1293 (2022).

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SUPPORT STAFF

Samantha Farrell, Sr. Administrative Assistant

Jay Sandlin, Research Support Associate

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Anantha P. Chandrakasan

Dean of Engineering, Vannevar Bush Professor of
Electrical Engineering & Computer Science
Department of Electrical Engineering and Computer Science

Design of digital integrated circuits and systems. Energy efficient implementation of signal processing, communication and medical systems. Circuit design with emerging technologies.

Rm. 38-107 | 617-258-7619 | anantha@mit.edu

POSTDOCTORAL ASSOCIATE

Donghyeon Han, RLE

Yeseul Jeon, RLE

GRADUATE STUDENTS

Aya Amer, EECS Maitreyi Ashok, EECS

Ruicong Chen, EECS (co-supervised with H. Lee)

Adam Gierlach, EECS (co-supervised with G. Traverso)

Alex Ji, EECS

Mingran Jia, EECS (co-supervised with R. Han)

Dimple Kochar, EECS

Eunseok Lee, EECS (co-supervised with R. Han)

Kyungmi Lee, EECS

Mohith Harish Manohara, EECS

Saurav Maji, EECS

Rishabh Mittal, EECS (co-supervised with H-S. Lee)

Patricia Jastrzebska-Perfect (co-supervised with G. Traverso)

Zoey Song, EECS

Saebyeok Shin, EECS

Miaorong Wang, EECS

Jongchan Woo, EECS (co-supervised with Rabia T. Yazicigil)

So-Yoon Yang, EECS (co-supervised with G. Traverso)

Deniz Yildirim, EECS

VISITING SCHOLARS

Rabia Tugce Yazicigil, Boston University

SUPPORT STAFF

Katey Provost, Program/Project Coordinator

SELECTED PUBLICATIONS

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Yufeng (Kevin) Chen

D. Reid (1941) and Barbara J. Weedon Career Development
Assistant Professor
Department of Electrical Engineering & Computer Science

Biomimetic robotics, insect-scale robotics, unsteady aerodynamics, soft artificial muscles, electroactive polymer actuators

Rm. 10-140H | 617-253-7351 | yufengc@mit.edu

POSTDOCTORAL ASSOCIATE

Steven Ceron (co-advised), EECS

GRADUATE STUDENTS

Suhan Kim, EECS

Zhijian Ren, EECS

Yi-Hsuan Hsiao, EECS

Quang Phuc N. Kieu (co-advised), EECS

SUPPORT STAFF

Catherine Bourgeois, Administrative Assistant

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Riccardo Comin

Associate Professor
Department of Physics

Quantum solids, electronic systems with strong interactions, superconductors, topological insulators. Single crystal synthesis of bulk and ultrathin materials. Heterostructure and device fabrication. Investigation of electronic symmetry breaking phenomena using advanced photon probes, including Angle-resolved Photoemission, Resonant X-ray scattering and imaging, Raman scattering.

Rm. 13-2153 | 617-253-7834 | rcomin@mit.edu

POSTDOCTORAL ASSOCIATES

Luca Nessi, Physics
Dongjin Oh, Physics
Joshua Sanchez, NSF MPS-Ascend Fellow
Yi Tseng, Physics

GRADUATE STUDENTS

Ahmet Kemal Demir, Physics
Min Gu Kang, Physics, Samsung Fellow
Jiaruo Li, Physics
Connor Occhialini, Physics
Qian Song, DMSE

UNDERGRADUATE STUDENT

Nicholas Gonzalez-Yepe, Chemistry

SUPPORT STAFF

Gerry Miller, Administrative Assistant

SELECTED PUBLICATIONS

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†co-authors

Jesús A. del Alamo

Donner Professor
Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

Nanometer-scale III-V compound semiconductor transistors for future digital, power, RF, microwave and millimeter wave applications. Reliability of compound semiconductor transistors. Diamond transistors. Ionic and ferroelectric non-volatile programmable AI synapses.

Rm. 38-246 | 617-253-4764 | alamo@mit.edu

POSTDOCTORAL ASSOCIATES

Elham Rafie Borujeny, EECS
Murat Onen, EECS

GRADUATE STUDENTS

Taekyong Kim, EECS
Aviram Massuda, EECS
Yanjie Shao, EECS
Dingyu Shen, EECS

SUPPORT STAFF

Elizabeth Kubicki, Administrative Assistant

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Luca Daniel

Professor

Department of Electrical Engineering & Computer Science

Development of numerical techniques: parameterized model order reduction, uncertainty quantification, inverse problems and robust optimization for high dimension parameter spaces. Current applications: magnetic resonance imaging; electrical power distribution networks; robustness & stability of deep neural networks.

Rm. 36-849 | 617-253-2631 | luca@mit.edu

RESEARCH SCIENTIST

Praneeth Namburi, IMES (co-mentor Brian Anthony)

GRADUATE STUDENTS

Adina Bechhofer, EECS (co-advisors Donnie Keathley, Karl Berggren)

Mercer Borris, EECS and LGO

Jackie Chen, EECS and LGO

Matteo Furlan, Politecnico di Milano (co-advisors Vladimir Bulovic, Jeff Lang)

Zhengqi Gao, EECS (co-advisor Duane Boning)

Lauren Heintz, EECS and LGO

Ching-Yun (Irene) Ko, EECS

Martin Ma, Harvard

Andrew Mighty, EECS and LGO

Jeet Mohapatra, EECS (co-advisor Tommi Jaakkola)

Jose E. C. Serralles, EECS

Wang Zhang, MechE

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UNDERGRADUATE STUDENTS

Angelos Assos, EECS

Anthony Baez, EECS

Leif Clark, EECS (co-advisor Jeff Lang)

Pawan Goyal, EECS SuperUROP

Zachary Gromko, EECS (Cadence co-supervisor Shirin Farrahi)

Thomas Ngo, EECS

William Nolan, EECS (co-advisor Jeff Lang)

Ishan Pakuwal, EECS

SUPPORT STAFF

Chadwick Collins, Administrative Assistant

SELECTED PUBLICATIONS

C.-Y. Ko, P.-Y. Chen, J. Mohapatra, P. Das, and L. Daniel, "SynBench: Task-Agnostic Benchmarking of Pretrained Representations using Synthetic Data," in *NeurIPS 2022 Workshop on Synthetic Data for Empowering ML Research*, Dec. 2022, New Orleans, USA.

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Dirk R. Englund

Associate Professor

Department of Electrical Engineering & Computer Science

Quantum Communications, Quantum Computing, and Quantum Sensing:
Devices and systems.

Rm. 36-525 | 617-324-7014 | englund@mit.edu

RESEARCH SCIENTISTS

Ryan Hamerly, RLE
Avinash Kumar, RLE
Matthew E. Trusheim, ISN
Franco Wong, RLE

ENGINEERS

Charles Hsu, RLE
Adyant Kamdar, Software Engineer
Anders Khaykin, RLE

POSTDOCTORAL ASSOCIATES

Jawaher Almutlaq, RLE
Ethan Arnault, RLE
Ian Berkman
Hyeonrak Choi, RLE
Mohamed ElKabbash, RLE
Lingling Fan, RLE
Qiusi Gu, RLE
Artur Hermans
Yong Hu, RLE
Bevin Huang, RLE
Chao Li, RLE
Chao Luan, RLE
Mahdi Mazaheri
Adrian Menssen, RLE
Camille Papon, RLE
Valeria Saggio, RLE
Kfir Sulimany
Sivan Trajtenberg-Mills, RLE
Sri Krishna Vadlamani, RLE
Bo-Han Wu

GRADUATE STUDENTS

Dowon Baek, EECS
Saamil Bandyopadhyay, RLE
Liane Bernstein, EECS
Cole Brabec, EECS
Kevin Chen, EECS
Ian Christen, EECS
Marc Davis, EECS
Ronald Davis
Yuqin (Sophia) Duan, EECS
Yin Min Goh, EECS
Isaac B. Harris, EECS
Hugo Larocque, EECS
Linsen Li
Thomas Propson, EECS
Hamza Raniwala, EECS
Hanfeng Wang, EECS

Reggie Wilcox

UNDERGRADUATE STUDENTS

Anthony L. Acevedo, EECS
Vaishnavi L. Addala, EECS
Annabel O. Adeyeri, EECS
Berkin Binbas, Physics
Eric Q. Bui, EECS
Kevin Z. Cheng, Physics
Torque Dandachi
Gage O. Lankford, Physics
Kenneth A. Muhammad, EECS
Jason T. Necaise
Quynh T. Nguyen
Lydia J. Patterson, EECS
Janet Y. Qian, EECS
Pedro Sales Rodriguez
Hank P. Stennes, EECS
Max J. Tao, Physics
Hasan Zeki Yildiz, EECS
Mikaeel M. Yunus

SUPPORT STAFF

Janice Balzer, Administrative Assistant

SELECTED PUBLICATIONS

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Jongyoon Han

Professor of Electrical Engineering & Biological Engineering
Department of Electrical Engineering & Computer Science
Department of Biological Engineering

BioMEMS, cell and molecular sorting, novel nanofluidic phenomena, biomolecule separation and pre-concentration, seawater desalination and water purification, bioprocessing, stem cells, engineering for cell therapy

Rm. 36-841 | 617-253-2290 | jjhan@mit.edu

RESEARCH SCIENTISTS

Kerwin Keck, SMART Centre, Singapore
Junghyo Yoon, RLE

RESEARCH ENGINEERS

Chin Ren Goh, SMART Centre, Singapore
Nicholas Ng, SMART Centre, Singapore
Kaiyun Quek, SMART Centre, Singapore
Nicholas Tan, SMART Centre, Singapore

POSTDOCTORAL ASSOCIATE

Kiesar Bhat, SMART Centre, Singapore
Mingyang Cui, RLE
Do Hyun Kim, RLE
Yaoping Liu, SMART Centre, Singapore
Daniel Roxby, SMART Centre, Singapore
Yanmeng Yang, SMART Centre, Singapore

GRADUATE STUDENTS

Alexander Bevacqua, BE
Hans Gaensbauer, EECS
Yejin Park, EECS
Zhumei Sun, ME
Jerome Tan, Singapore SMART Centre / NTU,
Singapore
Eric Wynne, EECS

SUPPORT STAFF

Arlene Wint, Administrative Assistant

SELECTED PUBLICATIONS

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Ruonan Han

Director of Center for Integrated Circuits and Systems
Associate Professor of Electrical Engineering & Computer Science
Officer of the Electrical Engineering & Computer Science
Undergraduate Laboratory
Department of Electrical Engineering & Computer Science

Integrated circuits and systems operating from RF to THz frequencies for sensing and communication applications. Electromagnetism, Chip-scale wave-matter interactions for miniature spectroscopy and frequency metrology.
Rm. 39-527A | 617-324-5281 | ruonan@mit.edu

GRADUATE STUDENTS

Cole Brabec (Co-supervised with Dirk Englund), EECS
Xibi Chen, EECS
Mingran Jia (Co-supervised with Anantha Chandrakasan), EECS
Eunseok Lee (Co-supervised with Anantha Chandrakasan), EECS
Jinchen Wang, EECS

SUPPORT STAFF

Kathleen Brody, Administrative Assistant
Elizabeth Kubicki, Administrative Assistant

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Song Han

Associate Professor

Department of Electrical Engineering & Computer Science

Machine learning, artificial intelligence, model compression, hardware acceleration

Rm. 38-344 | 617-253-0086 | songhan@mit.edu

POSTDOCTORAL ASSOCIATES

Wei-Ming Chen, EECS

Wei-Chen Wang, EECS

GRADUATE STUDENTS

Han Cai, EECS

Qiyao (Catherine) Liang, EECS

Ji Lin, EECS

Yujun Lin, EECS

Zhijian Liu, EECS

Haotian Tang, EECS

Hanrui Wang, EECS

Guangxuan Xiao, EECS

Zhekai Zhang, EECS

Ligeng Zhu, EECS

UNDERGRADUATE STUDENTS

Emelie Eldracher, EECS

Kevin Shao, EECS

SUPPORT STAFF

Jami L. Mitchell, Administrative Assistant

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Juejun (JJ) Hu

John F. Elliott Professor of Materials Science & Engineering
Department of Materials Science & Engineering

Integrated photonics, silicon photonics, optical metasurfaces

Rm. 13-4054 | 302-766-3083 | hujejun@mit.edu

RESEARCH SCIENTISTS

Tian Gu, MRL
Zhaoyi Li, DMSE

POSTDOCTORAL ASSOCIATES

Diana Mojahed, DMSE
Louis Martin, DMSE
Brian Sia, DMSE
Hanyu Zheng, DMSE

GRADUATE STUDENTS

Cosmin Constantin-Popescu, DMSE
Tushar Karnik, DMSE
Brian Mills, DMSE
Maarten Peters, DMSE
Khoi Phuong Dao, DMSE
Luigi Ranno, DMSE
Fan Yang, DMSE

SUPPORT STAFF

Sarah Ciriello, Administrative Assistant

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Qing Hu

Professor

Department of Electrical Engineering & Computer Science

Physics and applications of millimeter-wave, terahertz, and infrared devices.

Rm. 36-465 | 617-253-1573 | qhu@mit.edu

COLLABORATORS

Jianrong Gao, Delft University

Kevin Lascola, Thorlabs

John L. Reno, Sandia National Lab.

Zbig Wasilewski, University of Waterloo

Gerard Wysocki, Princeton University

POSTDOCTORAL ASSOCIATES

Ali Khalatpour, RLE

GRADUATE STUDENTS

Andrew Paulsen, EECS

Tianyi Zeng, EECS

SUPPORT STAFF

Shayne Fernandes, Administrative Assistant

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Rafael Jaramillo

Thomas Lord Associate Professor
Department of Materials Science and Engineering

Developing compound semiconductors for application in photonics, microelectronics, communication, and energy conversion. Emphasis on chalcogenide thin film processing, including molecular beam epitaxy (MBE) and advanced characterization.

Rm. 13-5025 | 617-324-6871 | rjaramil@mit.edu

POSTDOCTORAL ASSOCIATES

Varun Kamboj, DMSE
Zhenjing Liu, MRL
Ida Sadeghi, MRL

GRADUATE STUDENTS

Tao Cai, DMSE
Jessica Dong, DMSE
Jiahao Dong, DMSE
Jack Van Sambeek, DMSE
Kevin Ye, DMSE

SELECTED PUBLICATIONS

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Pablo Jarillo-Herrero

Professor

Department of Physics

Quantum electronic transport and optoelectronics with low dimensional materials, such as graphene, transition metal dichalcogenides, and topological insulators. Nanofabrication of Van der Waals heterostructures. Mesoscopic physics and superconductivity.

Rm. 13-2017 | 617-253-3653 | pjarillo@mit.edu

POSTDOCTORAL ASSOCIATES

Luis Antonio Benitez-Moreno, Physics

Clement Collignon, Physics

Aviram Uri, Physics

Yonglong Xie, Physics

Kenji Yasuda, Physics

GRADUATE STUDENTS

Jeong Min Park, Physics

Skandaprasad Rao, Physics

Shuwen Sun, Physics

Xirui Wang, Physics

Xueqiao Wang, DMSE

Liqiao Xia, Physics

Zhiren Zheng, Physics

UNDERGRADUATE STUDENTS

Antti Eero Asikainen, Physics

Alex He, Economics

SUPPORT STAFF

Andrew Birkel, Lab Manager

Gerry Miller, Administrative Assistant

SELECTED PUBLICATIONS

Q. Ma*, S.-Y. Xu*, C.-K. Chan, C.-L. Zhang, G. Chang, Y. Lin, T. Palacios, H. Lin, S. Jia, P. A. Lee, P. Jarillo-Herrero, and N. Gedik, "Direct Optical Detection of Weyl Fermion Chirality in a Topological Semimetal," *Nature Physics*, [in press], 2017.

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* Equal Contribution

Long Ju

Assistant Professor of Physics
Department of Physics

Two-dimensional materials, optical spectroscopy, optoelectronics,
Rm. 13-2005 | 617-253-4828 | longju@mit.edu

POSTDOCTORAL ASSOCIATES

Zhengguang Lu, Physics
Fangzhou Xia, Physics and Mechanical Engineering

GRADUATE STUDENTS

Tonghang Han, Physics
Dasol Kim, Physics
Junseok Seo, Physics
Jixiang Yang, Physics

UNDERGRADUATE STUDENT

Yuxuan Yao, Physics

SUPPORT STAFF

Gerry Miller, Administrative Assistant

SELECTED PUBLICATIONS

T. Han, Z. Lu, G. Scuri, J. Sung, J. Wang, T. Han, K. Watanabe, T. Taniguchi, L. Fu, H. Park, and L. Ju, "Orbital Multiferroicity in Rhombohedral Pentalayer Graphene," *Nature*, in press (2023).

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Jeehwan Kim

Associate Professor of Mechanical Engineering
Associate Professor of Materials Science and Engineering
Principal Investigator of Research Laboratory of Electronics

Remote epitaxy, Two-dimensional materials, 2D material-based layer transfer, III-V / III-N electronics, Complex oxides-based applications, Heterogeneous integration, Flexible electronics, Electronic skin, Sensor fusion, Neuromorphic computing.

Rm. 37-276 | 617-324-1948 | jeehwan @ mit . edu

POSTDOCTORAL ASSOCIATE

Hyunseok Kim, MechE
Jae Hwan Kim, MechE
Jekyung Kim, MechE
Ki Seok Kim, RLE
Sangho Lee, MechE
Bo-In Park, RLE
Jiho Shin, RLE
Min-Kyu Song, MechE
Junmin Suh, RLE
Young Jin Yoo, RLE

GRADUATE STUDENTS

Ne Myo Han, MechE
Doyoon Lee, MechE
Giho Lee, MechE
Yunpeng Liu, MechE
Kuangye Lu, MechE
Xinyuan Zhang, DMSE

SUPPORT STAFF

John Mayo, Administrative Assistant

SELECTED PUBLICATIONS

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Jing Kong

Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

Synthesis, characterization and applications of low-dimensional materials, including carbon nanotube, graphene and other two dimensional materials.

Rm. 13-3065 | 617-324-4068 | jingkong@mit.edu

RESEARCH SCIENTISTS

Nannan Mao, RLE

Ji Hoon Park, RLE

POSTDOCTORAL ASSOCIATES

Zachariah B. Hennighausen, RLE

Jiangtao Wang, RLE

Peng Wu, RLE

Kenan Zhang, RLE

Tianyi Zhang, RLE

GRADUATE STUDENTS

Meng-Chi (Ed) Chen, EECS

Angyu Lu, EECS

Zhien Wang, DMSE

Xudong (Sheldon) Zheng, EECS

VISITING STUDENTS

Hongwei Liu, RLE

Shin-Yi Tang, RLE

SUPPORT STAFF

Arlene Wint, Administrative Assistant

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Jeffrey H. Lang

Vitesse Professor of Electrical Engineering
Department of Electrical Engineering & Computer Science

Analysis, design, and control of electro-mechanical systems with application to traditional rotating machinery and variable-speed drives, micro/nano-scale (MEMS/NEMS) sensors and actuators, flexible structures, and the dual use of actuators as force and motion sensors.

Rm. 10-176 | 617-253-4687 | lang@mit.edu

POSTDOCTORAL ASSOCIATES

Jinchi Han, RLE

GRADUATE STUDENTS

Henry Anderson, EECS

Tori Dang, EECS

Grace Tang, EECS

Emma Warzynek, EECS

John Zhang, MechE

UNDERGRADUATE STUDENTS

Makar Kuznetsov, EECS

William Nolan, EECS

SUPPORT STAFF

Donna Gale, Administrative Assistant

Arlene Wint, Administrative Assistant

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Hae-Seung Lee

ATSC Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Analog and Mixed-signal Integrated Circuits, with a Particular Emphasis in Data Conversion Circuits in scaled CMOS.

Rm. 39-521 | 617-253-5174 | hslee@mit.edu

POSTDOCTORAL ASSOCIATE

Anand Chandrasekhar, EECS

GRADUATE STUDENTS

Ruicong Chen, EECS

Mohamed Elsheikh, EECS

Rebecca Ho, EECS

Jaehwan Kim, EECS

Rishabh Mittal, EECS

SUPPORT STAFF

Elizabeth Kubicki, Administrative Assistant

PUBLICATIONS

A. Chandrasekhar, R. Padrós-Valls, R. Pallarès-Lopéz, E. Palanques-Tost, N. Houstis, T. M. Sundt, H.-S. Lee, C. G. Sodini, and A. D. Aguirre, "Tissue Perfusion Pressure Enables Continuous Hemodynamic Evaluation and Risk Prediction in the Intensive Care Unit," *Nature Medicine* 29, Aug. 2023, <https://doi.org/10.1038/s41591-023-02474-6>.

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Luqiao Liu

Associate Professor

Department of Electrical Engineering & Computer Science

Spintronics; spin based logic and memory device for digital and neuromorphic computing; nanoscale magnetic material for information storage and microwave application; fabrication technique of magnetic nanodevices; spin related phenomena in semiconductor, topological insulator; magnetic dynamics .

39-553a | 617-253-0019 | luqiao@mit.edu

GRADUATE STUDENTS

Josh Chou, Physics

Zhiping He, EECS

Justin Hou, EECS

Zhongqiang Hu, EECS

Dooyong Koh, EECS

Brooke C. McGoldrick, EECS

Qiuyuan Wang, EECS

SUPPORT STAFF

Maria Markulis, Administrative Assistant

SELECTED PUBLICATIONS

A. H. Comstock, C.-T. Chou, Z. Wang, T. Wang, R. Song, J. Sklenar, A. Amassian, W. Zhang, H. Lu, L. Liu, M. C. Beard, and D. Sun, "Hybrid Magnonics in Hybrid Perovskite Antiferromagnets," *Nature Comm.*, 14, 1834, (2023).

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Scott R. Manalis

David H. Koch Professor in Engineering
Departments of Biological and Mechanical Engineering

Development and application of novel single-cell measurement approaches with a primary focus on cancer research.

Rm. 76-261 | 617-253-5039 | srm@mit.edu

POSTDOCTORAL ASSOCIATES

Chuyi Chen, KI
Georgios (Yorgos) Katsikis, KI
Teemu Miettinen, KI
Yanqi Wu, KI
Jiaquan (Jason) Yu, KI
Ye Zhang, KI

B. Hamza, A. B. Miller, L. Meier, M. Stockslager, S. R. Ng, E. M. King, L. Lin, K. L. DeGouveia, N. Mulugeta, N. L. Calistri, H. Strouf, C. Bray, F. Rodriguez, W. A. Freed-Pastor, C. R. Chin, G. C. Jaramillo, M. L. Burger, R. A. Weinberg, A. K. Shalek, T. Jacks, and S. R. Manalis, "Measuring Kinetics and Metastatic Propensity of CTCs by Blood Exchange Between Mice," *Nature Communications* 12, 2021.

GRADUATE STUDENTS

Myra Dada, BE
Sarah Duquette, BE
Adam Langenbacher, CSB
Alex Miller, HST
Felicia Rodriguez, BE
Thomas Usherwood, HST
Weida (Richard) Wu, BE

G. Katsikis, J. F. Collis, S. M. Knudsen, V. Agache, J. E. Sader, and S. R. Manalis, "Inertial and Viscous Flywheel Sensing of Nanoparticles," *Nature Communications*, 12, 2021.

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UNDERGRADUATE STUDENTS

Annie Chen, Wellesley College
Sofia Flores, BE
Michelle Hsu, BE
Grace Smith, BE
Kayla Suarez, BE
Gianfranco Yee, BE
Amy Zhong, BE

L. Mu, J. H. Kang, S. Olcum, K. R. Payer, N. L. Calistri, R. J. Kimmerling, S. R. Manalis, and T. P. Miettinen, "Mass Measurements During Lymphocytic Leukemia Cell Polyploidization Decouple Cell Cycle and Cell Size-dependent Growth," *PNAS*, 117(27), 2020.

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RESEARCH STAFF

Lin Lin, KI

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SUPPORT STAFF

Mariann Murray, Administrative Assistant

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Farnaz Niroui

Emmanuel E. Landsman Career Development Chair
Assistant Professor
Department of Electrical Engineering & Computer Science

Nanofabrication technologies at the few-nanometer-scale and for the emerging nanomaterials. Surfaces, interfaces and forces at the nanoscale. Active nanoscale devices with applications in molecular electronics, nanoelectromechanical systems, reconfigurable nanosystems with embedded intelligence, and quantum technologies.

Rm. 13-3005B | 617-324-7415 | fniroui@mit.edu

GRADUATE STUDENTS

Maxwell Conte, DMSE
Teddy Hsieh, EECS, NSF Fellow
Peter Satterthwaite, EECS, NSF Fellow
Sarah Spector, EECS, NSF Fellow
Spencer (Weikun) Zhu, ChemE

UNDERGRADUATE STUDENTS

Shelly Ben-David, EECS
Alex Quach, EECS

SUPPORT STAFF

Catherine Bourgeois, Administrative Assistant

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Jelena Notaros

Robert J. Shillman (1974) Career Development
Assistant Professor
Department of Electrical Engineering & Computer Science

Silicon photonics platforms, devices, and systems for applications including displays, sensing, communications, quantum, and biology.

Rm. 26-343 | 617-253-3073 | notaros@mit.edu

GRADUATE STUDENTS

Sabrina Corsetti, EECS, MIT Locher Fellow and NSF Fellow

Daniel DeSantis, EECS, MIT Locher Fellow and NSF Fellow

Andres Garcia, EECS

Ashton Hattori, EECS, MIT Analog Devices Fellow, NDSEG Fellow, and NSF Fellow

Milica Notaros, EECS, MIT Jacobs Fellow and NSF Fellow

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UNDERGRADUATE STUDENTS

Carol Pan, EECS

Abigail Shull, EECS & Physics

Michael Torres, Mathematics

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SUPPORT STAFF

Dianne Lior, Administrative Assistant

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William D. Oliver

Henry Ellis Warren (1894) Professor of EECS & Physics
Director of Center for Quantum Engineering
Associate Director of Research Laboratory of Electronics

The materials growth, fabrication, design, measurement of superconducting qubits. The development of cryogenic packaging and control William electronics involving cryogenic CMOS and single-flux quantum digital logic.

Rm. 13-3050 | 617-258-6018 | william.oliver@mit.edu

RESEARCH SCIENTISTS

Jeff Grover, RLE and CQE
Simon Gustavsson, RLE and CQE
Kyle Serniak RLE, CQE, and Lincoln Lab
Joel I. J. Wang, RLE and CQE

POSTDOCTORAL ASSOCIATES

Réouven Assouly, RLE
Aranya Goswami, RLE
Patrick Harrington, RLE
Max Hays, RLE
Daniel Rodan Legrain, RLE
Ilan Rosen, RLE

GRADUATE STUDENTS

Aziza Almanakly, EECS, PD Soros Fellow
Junyoung An, EECS, KFAF Fellow
Lamia Ateshian, EECS
Will Banner, EECS
Shoumik Chowdhury, EECS, NSF Fellow
Qi (Andy) Ding, EECS
Shantanu Jha, EECS, NSF Fellow
Hanlim (Harry) Kang, EECS, KFAF Fellow
Junghyun Kim, EECS, KFAF Fellow
Chris McNally, EECS
Miguel Moreira, EECS
Sarah Muschinske, EECS, NASA Fellow
David Pahl, EECS
Lukas Pahl, EECS
David Rower, Physics, NSF Fellow
Beatriz Yankelevich, EECS, Hertz and NSF Fellow
Sameia Zaman, EECS, SLB Faculty for the Future Fellow

UNDERGRADUATE STUDENTS

Ashley Luo, EECS
Catherine Tang, EECS

VISITING STUDENTS

Kevin Kiener, Technical University of Munich
Elifnaz Onder, Yale University

SUPPORT STAFF

Margaret McCroby, Administrative Assistant
Chihiro Watanabe, Program Administrator

SELECTED PUBLICATIONS

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Tomás Palacios

Director, Microsystems Technology Laboratories
Professor, Department of Electrical Engineering & Computer Science

Design, fabrication, and characterization of novel electronic devices and systems based on wide bandgap semiconductors & two-dimensional (2-D) materials, polarization & bandgap engineering, transistors for high voltage, sub-mm wave power & digital applications, sensors and heterogeneous integration.

Rm. 39-567 | 617-324-2395 | tpalacios@mit.edu

GRADUATE STUDENTS

Jung-Han (Sharon) Hsia, EECS
Hae Won Lee, EECS
Kevin Limanta, EECS
Christian Lopez Angeles, EECS
Yiyue Luo, EECS
Elaine McVay, EECS
Gillian Micale, DMSE
John Niroula, EECS
Hridibrata Pal, EECS
Joshua Perozek, EECS
Pao-Chuan Shih, EECS
Qingyun Xie, EECS
Mantian Xue, EECS
Pradyot Yadav, EECS
Mengyang Yuan, EECS
Jiadi Zhu, EECS

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UNDERGRADUATE STUDENTS

Franck Belemkoabga, UROP
Matthew Cox, UROP
Denis Eruz, UROP
Adina Golden, UROP
Rolando Gonzalez, SuperUROP
James Greer, UROP
Alisa Hathaway, UROP
Neelambar Mondal, UROP
Nishat Fahmida Prottyasha, UROP

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VISITORS

Theresia Knobloch, TU Wien
Marisa Lopez-Vallejo, Professor, Universidad Politécnica de Madrid
David Morales, Universidad Politécnica de Madrid
Javier de Mena Pacheco, Universidad Politécnica de Madrid
Michal Prokop, Catalan Institute of Nanoscience and Nanotechnology
Anthony Taylor, Edwards Vacuum

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SUPPORT STAFF

Elizabeth Green, Sr. Administrative Assistant
Preetha Kingsview, Administrative Assistant

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David Perreault

Ford Professor of Engineering
Department of Electrical Engineering & Computer Science

Power electronics and energy conversion systems, high-efficiency radio-frequency power amplifiers and rf applications, Renewable energy systems, applications of power electronics in industrial, commercial, scientific, transportation, and biomedical systems

Rm. 10-172 | (617) 258-6038 | djperrea@mit.edu

POSTDOCTORAL ASSOCIATE

Xin Zan, RLE

GRADUATE STUDENTS

Julia Estrin, EECS
K Rafa Islam, EECS
Amanda Jackson, EECS
Mansi Joisher, EECS
Mohammad Qasim, EECS
Rachel Yang, EECS

UNDERGRADUATE STUDENTS

Sarah Coston, EECS

SUPPORT STAFF

David M. Otten, Principal Research Engineer
Donna Gale, Administrative Assistant

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Carlos M. Portela

d'Arbelloff Career Development Chair
Assistant Professor
Department of Mechanical Engineering

Mechanics of materials, emphasis on architected materials, nanomechanics, in situ mechanical testing, extreme dynamic conditions, acoustic metamaterials, precision additive manufacturing

Rm. 1-304 | 617-715-2680 | cportela@mit.edu

POSTDOCTORAL ASSOCIATES

Molly Carton, MechE, MIT Engineering Excellence Fellow
Yun Kai, MechE
James U. Surjadi, MechE

W. P. Moestopo, A. J. Mateos, R. M. Fuller, J. R. Greer, and C. M. Portela, "Pushing and Pulling on Ropes: Hierarchical Woven Materials," *Adv. Sci.* 7 (2020) 2001271. <https://doi.org/10.1002/advs.202001271>.

GRADUATE STUDENTS

Bastien Aymon, MechE
Thomas Butruille, MechE
Andrew Chen, MechE
Somayajulu Dhulipala, MechE
Micheal Espinal, MechE
Samuel Figueroa, MechE
Rachel Sun, MechE

SUPPORT STAFF

Janet Maslow, Administrative Assistant

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Negar Reiskarimian

X-Window Consortium Career Development Assistant Professor
Department of Electrical Engineering & Computer Science

Integrated circuits and systems and applied electromagnetics with a focus on analog, RF, millimeter-Wave (mm-Wave) and optical integrated circuits, metamaterials and systems for a variety of applications.

Rm. 39-427a | 617-253-0726 | negarr@mit.edu

GRADUATE STUDENTS

Soroush Araei, EECS
Shahabeddin Mohin, EECS
Sarina Sabouri, EECS, MIT Analog Devices Fellow
(co-supervised with A. Chandrakasan)
Melania St. Cyr, EECS, Draper Fellow
Haibo Yang, EECS, MIT Jacobs Fellow

UNDERGRADUATE STUDENTS

Deniz Erus, UROP

SUPPORT STAFF

Maria Markulis, Administrative Assistant

SELECTED PUBLICATIONS

S. Araei, S. Mohin, and N. Reiskarimian, "Realization of Low-Loss Fully-Passive Harmonic Rejection N-Path Filters," *IEEE International Microwave Symposium (IMS)*, Jun. 2023 [invited and to appear in *IEEE Microwave and Wireless Technology Letters (MWTL)*].

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Charles G. Sodini

LeBel Professor

Department of Electrical Engineering & Computer Science

Electronics and integrated circuit design and technology. Specifically, his research involves technology intensive integrated circuit and systems design, with application toward medical electronic devices for personal monitoring of clinically relevant physiological signals.

Rm. 39-527b | 617-253-4938 | sodini@mtl.mit.edu

COLLABORATORS

Sam Fuller, Analog Devices, Inc

Joohyun Seo, Analog Devices, Inc.

POSTDOCTORAL ASSOCIATE

Anand Chandrasekhar, MTL

SUPPORT STAFF

Kathleen Brody, Administrative Assistant

SELECTED PUBLICATIONS

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Vivienne Sze

Associate Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Joint design of signal processing algorithms, architectures, VLSI and systems for energy-efficient implementations. Applications include computer vision, machine learning, autonomous navigation, image processing and video coding.

Rm. 38-260 | 617-324-7352 | sze@mit.edu

GRADUATE STUDENTS

Tanner Andrulis, EECS (co-advised with Joel Emer)
Zih-Sing Fu, EECS (co-advised with Sertac Karaman)
Dasong Gao, EECS (co-advised with Sertac Karaman)
Keshav Gupta, EECS (co-advised with Sertac Karaman)
Jamie Koerner, EECS (co-advised with Thomas Heldt)
Peter Li, EECS (co-advised with Sertac Karaman)
Soumya Sudhakar, AeroAstro (co-advised with Sertac Karaman)
Yannan Nellie Wu, EECS (co-advised with Joel Emer)
Zi Yu Fisher Xue, EECS (co-advised with Joel Emer)

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UNDERGRADUATE STUDENTS

Xavier Bell, AeroAstro
Kaustubh Dighe, EECS
Andrew Feldman, EECS
Sebastian Garcia, EECS
Michael Gilbert, EECS
Kailas Kahler, EECS
John Posada, AeroAstro
Sean Alex Rice, EECS
Adrianna Wojtyna, EECS
Reng Zheng, EECS

SUPPORT STAFF

Janice L. Balzer, Administrative Assistant

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Carl V. Thompson

Director, Materials Research Laboratory
Stavros Salapatas Professor of Materials Science and Engineering
Department of Materials Science & Engineering

Processing and properties of materials for micro- and nano-systems.

Rm. 13-5069 | 617-253-7652 | cthomp@mit.edu

POSTDOCTORAL ASSOCIATES

Haemin Paik, DMSE
Hui Teng Tan, Singapore

GRADUATE STUDENTS

Ryan Benz, MechE
Uttara Chakraborty, EECS
Misong Ju, DMSE
Christopher Mallia, DMSE

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Luis Fernando Velásquez-García

Principal Research Scientist
Microsystems Technology Laboratories

Micro- and nano-enabled, multiplexed, scaled-down systems that exploit high electric field phenomena; microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS); powerMEMS; additively manufactured MEMS and NEMS. Actuators, cold cathodes, ionizers, microfluidics, microplasmas, CubeSat hardware, portable mass spectrometry, pumps, sensors, X-ray sources.

Rm. 39-415B | 617-253-0730 | lvelasq@mit.edu

POSTDOCTORAL ASSOCIATES

Han-Joo Lee, EECS
Nicholas Lubinsky, EECS

GRADUATE STUDENTS

Zoey Bigelow, EECS
Jorge Canada Perez-Sala, EECS
Alejandro Diaz, EECS
Colin Eckhoff, EECS
Alex Kashkin, MechE
Hyeonseok Kim, MechE
Isabelle Liu, EECS

SUPPORT STAFF

Jami L. Mitchell, Administrative Assistant

SELECTED PUBLICATIONS

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Theses Awarded

S.M.

- **Tanner Andrusis** (V. SZE)
Efficient, Accurate, and Flexible PIM Inference through Adaptable Low-Resolution Arithmetic
- **Adina Bechhofer** (L. DANIEL)
Geometrical Optimization of Planar Nano Vacuum Channel Transistors
- **Zoey Bigelow** (L. VELASQUEZ-GARCIA)
Solutions to the Generalized UAV Delivery Routing Problem for Last-Mile Delivery with Societal Constraints
- **Mercer Boris** (L. DANIEL)
AI in the Cath Lab: Implications of Clinical AI-Enabled Assistance for Intravascular Ultrasound Procedures
- **Taylor Facen** (L. DANIEL)
How Enhanced Data Availability Affects Multi-Channel Marketing Attribution
- **Lauren Heintz** (L. DANIEL)
Scenario Analysis of Profitability of New Offerings under Different Business Contract Models
- **Alex Kachkine** (L. VELASQUEZ-GARCIA)
Additively Manufacturing High-Performance, Low-Cost Electrospray Ion Sources for Point-of-Care Mass Spectrometry
- **Quang Kieu** (J. LANG)
Design and Fabrication of an Electric-Field Induction Motor
- **Ching-Yun (Irene) Ko** (L. DANIEL)
Revisiting Contrastive Learning through the Lens of Neighborhood Component Analysis
- **Andrew Mighty** (L. DANIEL)
Autonomous Drone Assisted Aircraft Inspections
- **Aaron Yeiser** (J. LANG)
A Fully-Implantable Low-Noise EMI-Resistant Piezoelectric-Polymer Micro-phone and Amplifier for the Middle Ear

M. ENG

- **Alejandro Diaz** (L. VELASQUEZ-GARCIA)
Through Iron & Ice: Searching for Sterile Neutrinos at the IceCube Neutrino Observatory
- **Torque El Dandachi** (K. BERGGREN)
Efficient Simulation of Large-Scale Superconducting Nanowire Circuits
- **Zachary Gromko** (L. DANIEL)
Accelerated Channel Operating Margin for Automated Context and Applications to Design Optimization

- **Zhiye Song** (A. CHANDRAKASAN)
Algorithm and Hardware Co-optimization for Image Segmentation in Wearable Ultrasound Devices: Continuous Bladder Monitoring

PH.D.

- **Saamil Bandyopadhyay** (D. ENGLUND)
Accelerating Artificial Intelligence with Programmable Silicon Photonics
- **Ruicong Chen** (H.-S. LEE)
Analog-to-Digital Converters For Secure and Emerging AIoT Applications
- **Rebecca Ho** (H.-S. LEE)
Driving Emerging Technologies From Concept to Reality: A Case Study of Carbon Nanotubes
- **Jaehwan Kim** (H.-S. LEE)
Monolithic Integration of Fluidics, Electronics, and Photonics using CMOS Foundry Processes
- **John Lake** (K. VARANASI)
Physicochemical Interactions at Interfaces: Mass and Charge Transfer at Chemically Reacting Interfaces
- **Victor Leon** (K. VARANASI)
Active Interfaces: From Biointerfaces to Mineralization
- **Ang-Yu Lu** (J. KONG)
Artificial Intelligence-Aided Synthesis and Characterization of 2D Materials
- **Elaine McVay** (T. PALACIOS)
Visible and Infrared Light Detection Using 2D Materials
- **Rishabh Mittal** (H.-S. LEE)
A Continuous-Time Pipeline ADC with Reduced Sensitivity to Clock Jitter
- **Murat Onen** (J. DEL ALAMO)
Devices and Algorithms for Analog Deep Learning
- **Crystal Owens** (J. HART)
Extrusion Printing of Carbon Nanotube Inks, from Rheology to Electronics
- **Jatin Patil** (J. GROSSMAN)
Rapidly-Deployable Materials Processing Approaches for Energy Applications and Chemical Separations
- **Mihika Prabhu** (R. RAM)
Large-scale Programmable Silicon Photonics for Quantum and Classical Machine Learning
- **Taqiyyah Safi** (L. LIU)
Tailoring Charge to Spin Conversion in Novel Materials for Efficient

PH.D. (CONTINUED)

- **Jose E. Cruz Serralles** (L. DANIEL)
Integral Equation-Based Inverse Scattering and Coil Optimization in Magnetic Resonance Imaging
- **Yanjie Shao** (J. DEL ALAMO)
Ultra-scaled III-V Vertical Tunneling Transistors
- **Alexander Sludds** (D. ENGLUND)
Delocalized Photonic Deep Learning on the Internet's Edge
- **Ella Wassweiler** (V. BULOVIC)
Vapor Transport Deposition for Perovskite Solar Cells
- **Yannan Nellie Wu** (V. SZE)
Systematic Modeling and Design of Sparse Tensor Accelerators
- **Mantian Xue** (T. PALACIOS)
Graphene-based Biochemical Sensing Array: Materials, System Design and Data Processing
- **Mengyang Yuan** (T. PALACIOS)
GaN Electronics for High-Temperature Applications
- **Pengxiang Zhang** (L. LIU)
Current-induced Dynamics of Easy-Plane Antiferromagnets
- **Zhengxing Zhang** (D. BONING)
Adjoint Methods and Inverse Modeling for Process Variation Analysis in Silicon Photonics

Startups Affiliated with MTL and MIT.nano Faculty

Vladimir Bulović

- QD Vision
- Kateeva | <https://kateeva.com/>
- Ubiquitous Energy | <https://ubiquitous.energy>
- Swift Solar | www.swiftsolar.com
- Optigon | www.optigon.us
- Active Surfaces | www.linkedin.com/company/activesurfaces

Tonio Buonassisi

- Xinterra Pte.Ltd. | <https://xinterra.tech>

Dirk R. Englund

- QuEra Computing, Inc | www.quera.com
- Lightmatter Inc | www.lightmatter.ai
- Quantum Network Technologies, Inc | www.qunett.com
- Dust Identity Inc | <https://dustidentity.com/>

Eugene Fitzgerald

- nsc pte ltd | www.nscinnovation.com/

Ruonan Han

- Cambridge Terahertz | <https://www.thzcorp.com>

Juejun (JJ) Hu

- 2Pi Inc. | <https://www.2pioptics.com/>
- InSpek SAS | <https://www.inspek-solutions.com/>
- LyteChip Inc. | <https://lytechip.com/>

Hae-Sueng (Harry) Lee

- Omni Technologies | www.omnidesigntech.com

William D. Oliver

- Atlantic Quantum | www.atlantic-quantum.com

Tomás Palacios

- Finwave Semiconductor | www.finwavesemi.com

David Perreault

- Artic Sand |
- Onchip power/Finsix |
- Eta Devices | www.linkedin.com/company/eta-devices-inc-/about/
- Eta Wireless | www.etawireless.com

Charlie Sodini

- Prescient Devices | www.prescientdevices.com

Kripa Varanasi

- LiquiGlide Inc. | <https://liquiglide.com>
- Dropwise Corp. | www.drop-wise.com
- Infinite Cooling | www.infinite-cooling.com
- AgZen Inc. | www.agzen.com
- Alsym Energy | www.alsym.com
- CoFLo Medical | www.coflo-medical.com

Luis Fernando Velásquez-García

- FORAY Bioscience | www.foraybio.com

Glossary

TECHNICAL ACRONYMS

ADC	Analog-to-Digital Converters
CMOS	Complementary Metal–Oxide–Semiconductor
CNT	Carbon Nanotubes
ECP	Electro-Chemical Plating
FET	Field-Effect Transistor
HSQ	Hydrogen Silsesquioxane
InFO	Integrated Fan Out
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
nTRON	Nanocryotron
RDL	Re-distribution Layers
RIE	Reactive Ion Etching
SNSPDs	Superconducting Nanowire Single Photon Detectors
SS	Subthreshold Swing
TMAH	Tetramethylammonium Hydroxide
TREC	Thermally Regenerative Electrochemical Cycle

MIT ACRONYMS & SHORTHAND

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
↑ IRG	Interdisciplinary Research Group
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
ISN	Institute for Soldier Nanotechnologies
KI	David H. Koch Institute for Integrative Cancer Research
LL	Lincoln Laboratory
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MIT-CG	MIT/MTL Center for Graphene Devices and 2D Systems
MITEI	MIT Energy Initiative
MIT-GaN	MIT/MTL Gallium Nitride (GaN) Energy Initiative

MISTI	MIT International Science and Technology Initiatives
MIT-SUTD	MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
↑ SMART	Singapore-MIT Alliance for Research and Technology Center
↑ SMART-LEES	SMART Low Energy Electronic Systems Center
SUTD-MIT	MIT-Singapore University of Technology and Design Collaboration Office
UROP	Undergraduate Research Opportunities Program

U.S. GOVERNMENT ACRONYMS

AFOSR	U.S. Air Force Office of Scientific Research
↑ FATE-MURI	Foldable and Adaptive Two-dimensional Electronics Multidisciplinary Research Program of the University Research Initiative
AFRL	U.S. Air Force Research Laboratory
ARL	U.S. Army Research Laboratory
↑ ARL-CDQI	U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO	Army Research Office
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
DARPA	Defense Advanced Research Projects Agency
↑ DREaM	Dynamic Range-enhanced Electronics and. Materials
DoD	Department of Defense
DoE	Department of Energy
↑ EFRC	U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA	U.S. DoD Defense Threat Reduction Agency
IARPA	Intelligence Advanced Research Projects Activity
↑ RAVEN	Rapid Analysis of Various Emerging Nanoelectronics
NASA	National Aeronautics and Space Administration
↑ GSRP	NASA Graduate Student Researchers Project
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
↑ NCI	National Cancer Institute
NNSA	National Nuclear Security Administration

NRO	National Reconnaissance Office
NSF	National Science Foundation
↑ CBMM	NSF Center for Brains, Minds, and Machines
↑ CIQM	Center for Integrated Quantum Materials
↑ CSNE	NSF Center for Sensorimotor Neural Engineering
↑ E3S	NSF Center for Energy Efficient Electronics Science
↑ GRFP	Graduate Research Fellowship Program
↑ IGERT	NSF The Integrative Graduate Education and Research Traineeship
↑ NEEDS	NSF Nano-engineered Electronic Device Simulation Node
↑ PECASE	Presidential Early Career Awards for Scientists and Engineers
↑ SEES	NSF Science, Engineering, and Education for Sustainability
↑ STC	NSF Science-Technology Center
ONR	Office of Naval Research

OTHER ACRONYMS

CNRS Paris	Centre National de la Recherche Scientifique
CONACyT	Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE	Institute of Electrical and Electronics Engineers
IHP Germany	Innovations for High Performance Microelectronics Germany
KIST	Korea Institute of Science and Technology
KFAS	Kuwait Foundation for the Advancement of Sciences
MASDAR	Masdar Institute of Science and Technology
NTU	Nanyang Technological University
NUS	National University of Singapore
NYSCF	The New York Stem Cell Foundation
SRC	Semiconductor Research Corporation
↑ NEEDS	NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD	Singapore University of Technology and Design
TEPCO	Tokyo Electric Power Company
TSMC	Taiwan Semiconductor Manufacturing Company

Principal Investigator Index

A

Agarwal, Anuradha M.iv, 51
Akinwande, Akintunde I.v, 35
Anthony, Brianiv
Antoniadis, Dimitri A.29, 122

B

Baldo, Marc A.v, 60, 73, 123
Barbastathis, George78
Bawendi, Moungi G.49, 60
Beach, Geoffrey S.99
Berggren, Karl K.iv, v
Boning, Duane S.ii, 23, 51, 54, 68, 76, 113, 124
Boyden, Edward S.104, 125
Bulović, Vladimiri, iii, iv, 46, 47, 48, 49, 55, 88, 89, 126, 160
Buonassisi, Tonio160

C

Chandrakasan, Anantha P.v, 14, 16, 17, 19, 67, 77, 127
Chen, Kevin84, 128
Comin, Riccardo129

D

Daniel, Luca131
del Alamo, Jesús A.v, 29, 31, 34, 74, 75, 130
Doyle, Patrick S.94

E

Emer, Joel S.63
Englund, Dirk R.v, 20, 56, 132, 160

F

Fitzgerald, Eugene A.160

H

Han, Jongyoon26, 88, 133
Han, Ruonanii, 15, 16, 17, 20, 117, 134, 160
Han, Song9, 64, 65, 67, 70, 71, 72, 77, 110, 135
Hart, A. Johnv
Heldt, Thomas2, 4
Hu, Juejunv, 57, 59, 61, 136, 160
Hu, Qing137

J

Jaramillo, Rafael45, 90, 91, 138
Jarillo-Herrero, Pabloiv, v, 95, 101, 102, 139
Ju, Longv, 103, 140

K

Kimerling, Lionel C.51
Kim, Jeehwanv, 43, 69, 141
Kong, Jingv, 30, 36, 92, 97, 100, 142

L

Lang, Jeffrey H.ii, 10, 68, 88, 143
LeBeau, James M.iv, 45
Lee, Hae-Seung9, 14, 19, 66, 144, 160
Liu, Luqiao24, 26, 73, 145
Lozano, Paulov

M

Manalis, Scott R.93, 146

N

Niroui, Farnazv, 97, 98, 105, 147
Notaros, Jelena52, 53, 58, 108, 148

O

Oliver, William D.iv, v, 107, 109, 149, 160

P

Palacios, Tomási, ii, iii, iv, v, 6, 27, 30, 32, 33, 35, 37,
.....38, 39, 40, 41, 42, 118, 150
Perreault, David J.151, 161
Portela, Carlos M.152

R

Reiskarimian, Negar13, 153
Ross, Caroline A.v
Ross, Frances M.iv, 91

S

Sarkar, Deblinav
Smith, Henry I.114
Smith, Zachary P.115
Sodini, Charles G.2, 119, 154, 161
Soljačić, Marin104
Swagger, Timothy M.115
Sze, Vivienneii, 18, 63, 155

T

Thompson, Carl V.iv, 23, 156
Tisdale, William A.60, 96
Tuller, Harry L.46

V

Varanasi, Kripa K.iv, 5, 161
Velásquez-García, Luis F.ii, iv, 3, 22, 25, 28, 80, 81,
.....82, 83, 85, 112, 157, 161
Voldman, Joel8, 11

W

Wang, Evelyn N.v

Y

Yildiz, Bilgeii, v

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Analog Devices, Inc.
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Lam Research
NCSOFT
NEC
Raith
UpNano