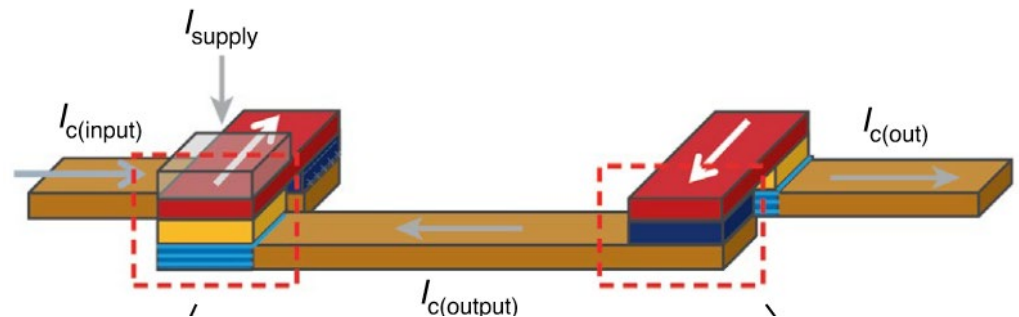
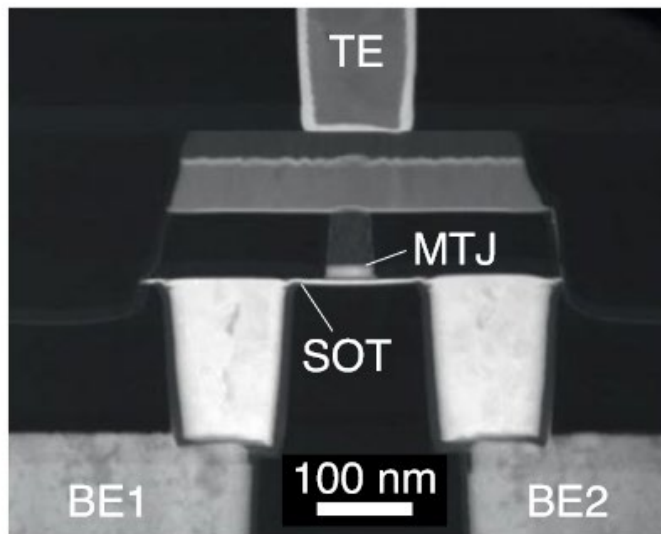


Spintronic Material and Devices

Luqiao Liu, Department of EECS

Mar 6th, 2024

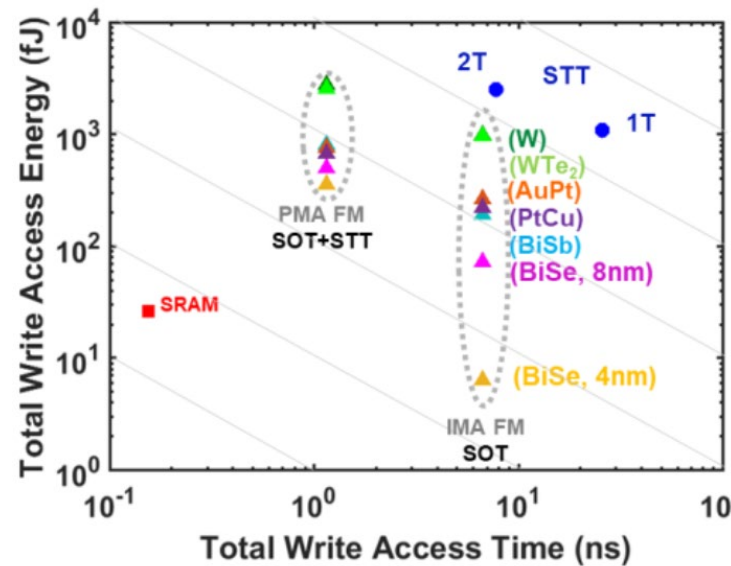
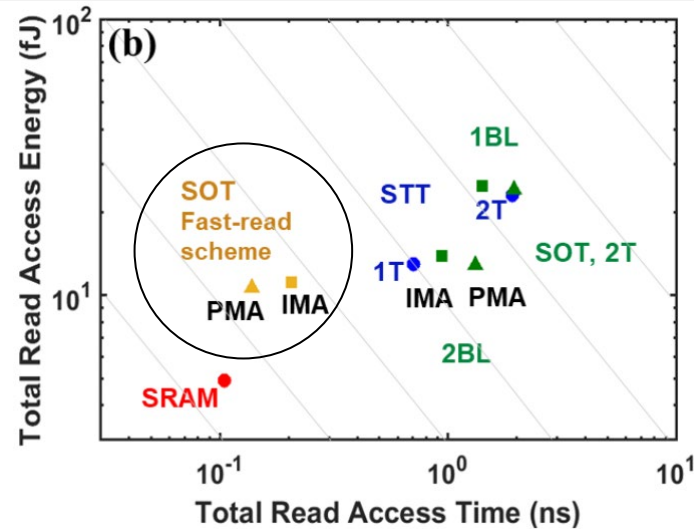
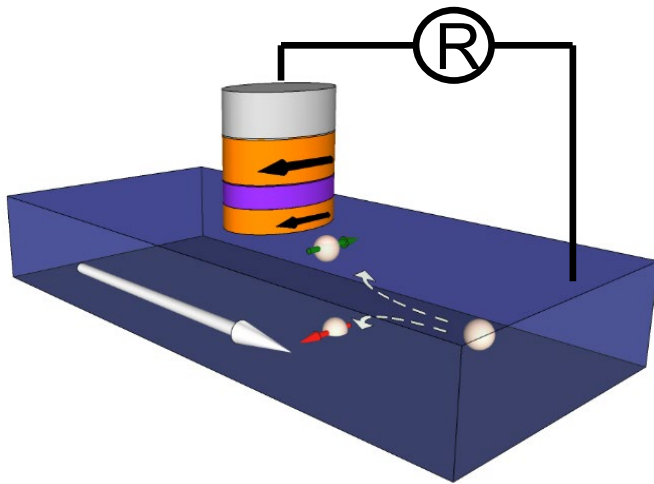


Research directions in our lab

- **New Materials and Physics for better magnetic memory and spin logic**
- **Spintronics for new computing schemes**

SOT-MRAM as a Potential Replacement for Cache and Main Memory

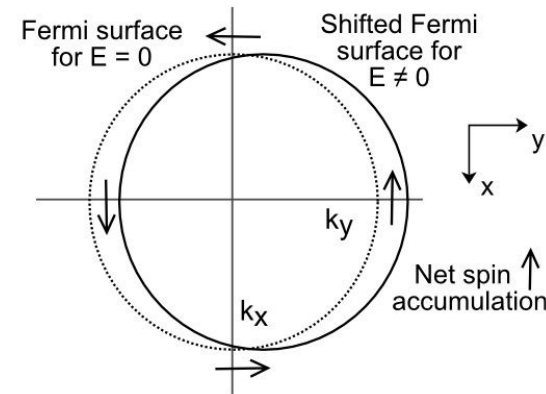
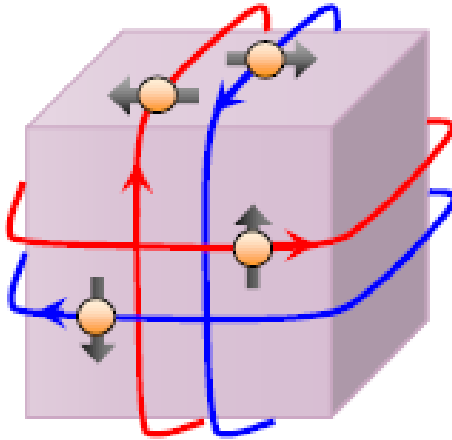
SOT MRAM



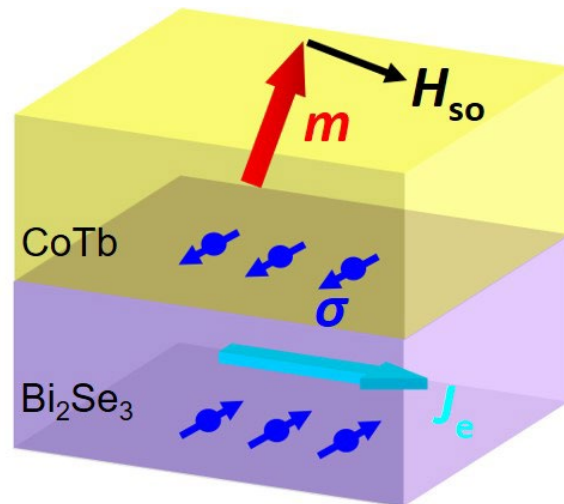
DOI: 10.1109/IEDM13553.2020.9371979

1. Lowering the switching power with topological materials

Topological insulator: spin – momentum coupling in surface states

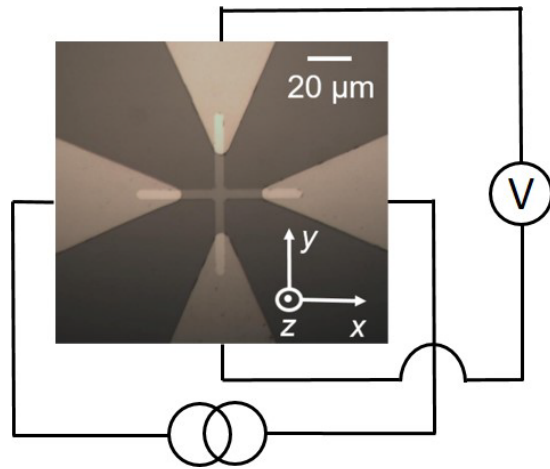


Can we use the surface spins to switch magnetic moment in MRAM?



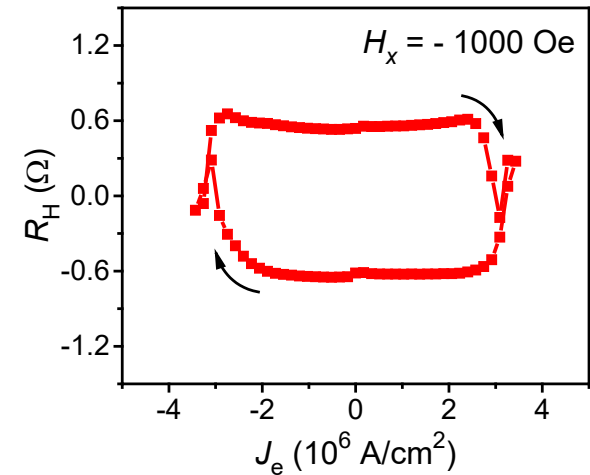
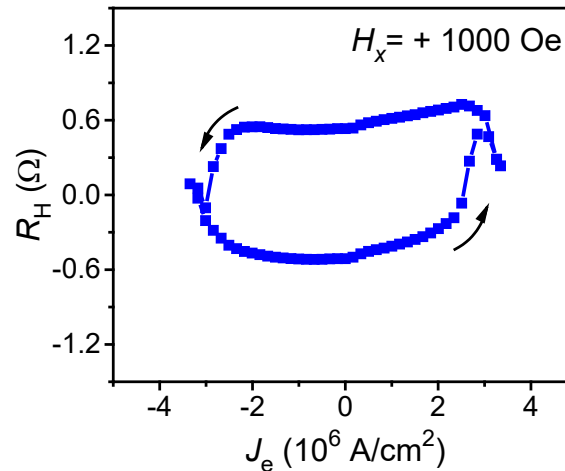
- An efficient switching mechanism for generating spin current
- Are topological insulator surface states stable enough at Room temperature?
- Will the strong magnetism in ferromagnet destroy topological insulator?

Topological Insulator Induced Magnetic Switching at Room Temperature

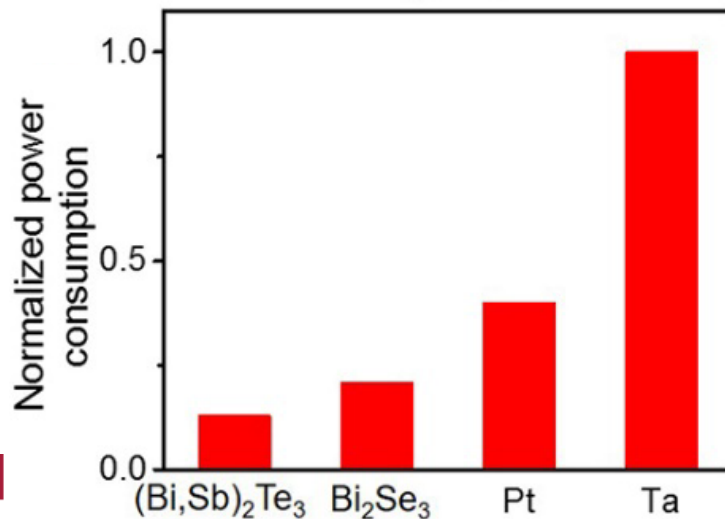


MBE $\text{Bi}_2\text{Se}_3/\text{Co}_{1-x}\text{Tb}_x/\text{SiN}_x$

R vs I



Benchmark on Power Consumption

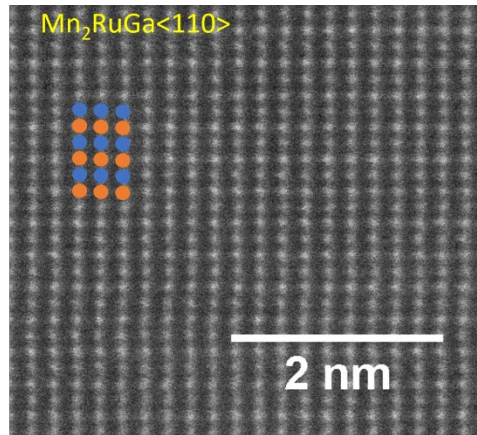
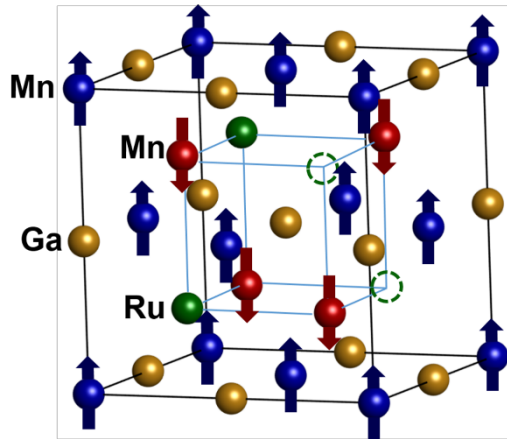


Power consumption is reduced by 10X via the usage of topological insulator

J. Han, *et al*, L. Q. Liu, PRL, 119, 077702 (2017)

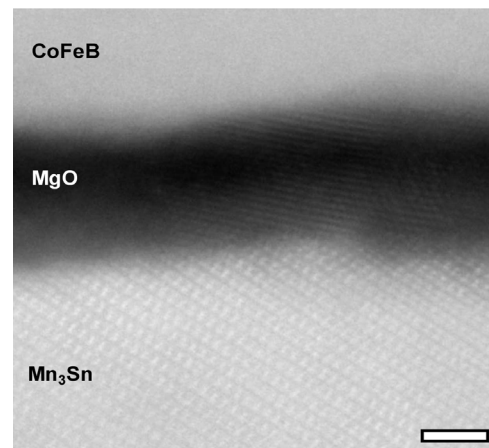
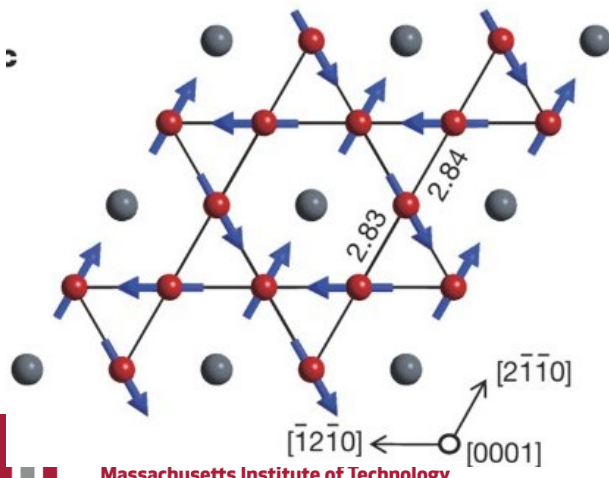
2. Increasing the switching speed by using zero moment magnet

- ✓ zero momentum magnet with collinear spin ordering



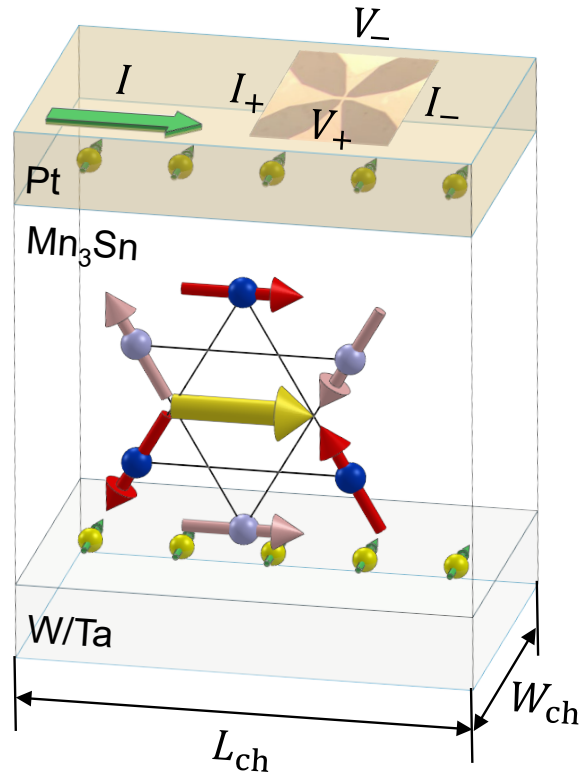
J. Finley et al. Adv. Mater. 31, 1805361 (2018)

- ✓ Non-collinear antiferromagnet with zero magnetic momentum - Mn_3Sn

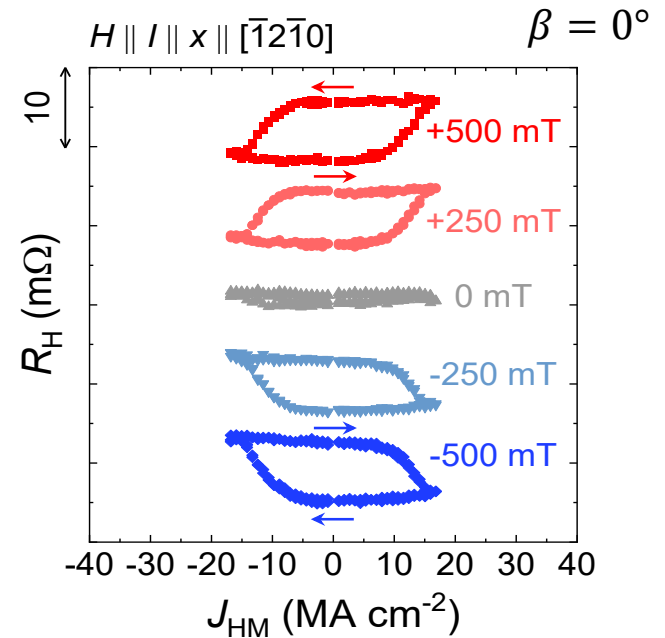


Can we switch antiferromagnet with SOT?

Constructive Rotation from Sub-Lattices



□ Electrical manipulation

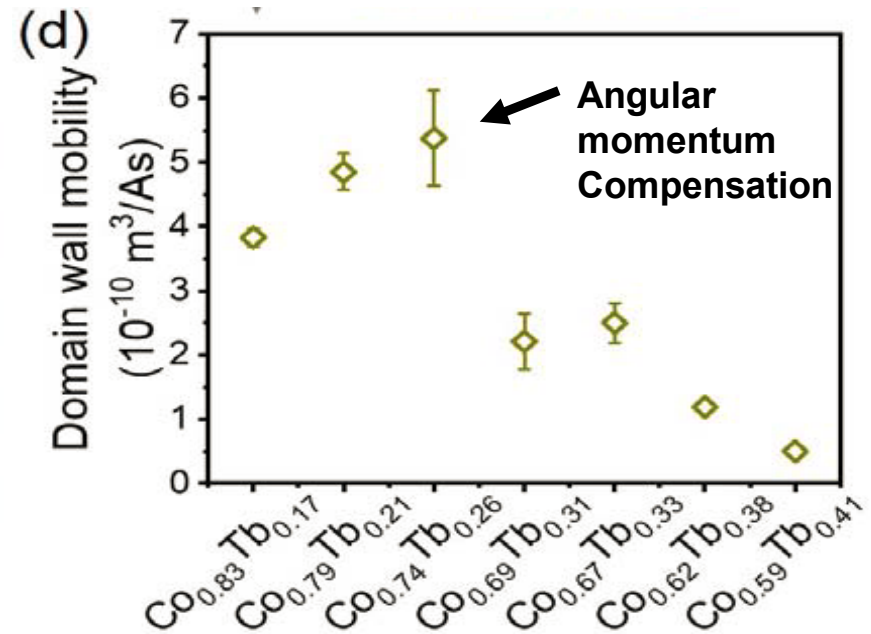
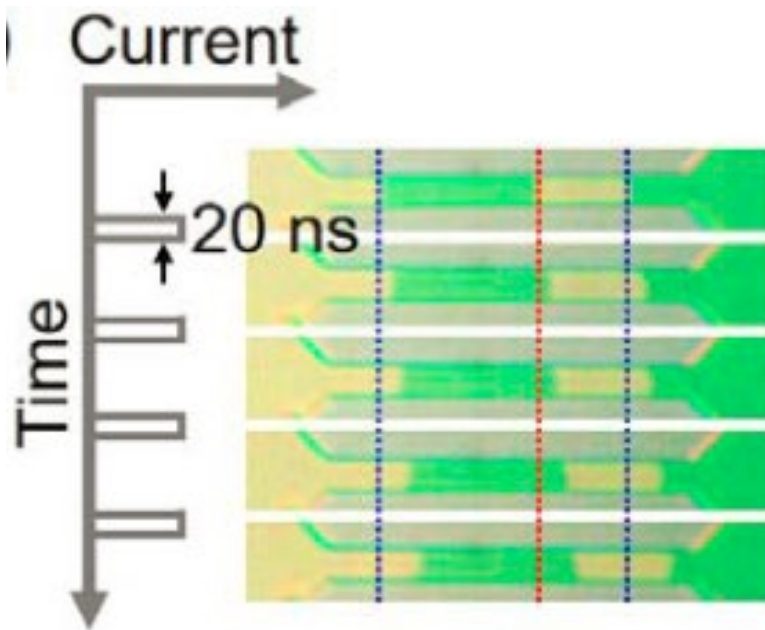


J.-Y. Yoon et al., L. Liu, Nat. Mater (2023)

- SOT can switch overall AFM ordering with an efficiency similar to regular ferromagnetic free layer (e.g., CoFeB)

Speed advantage by using zero moment magnet

- ✓ Faster switching speed of magnetic domains

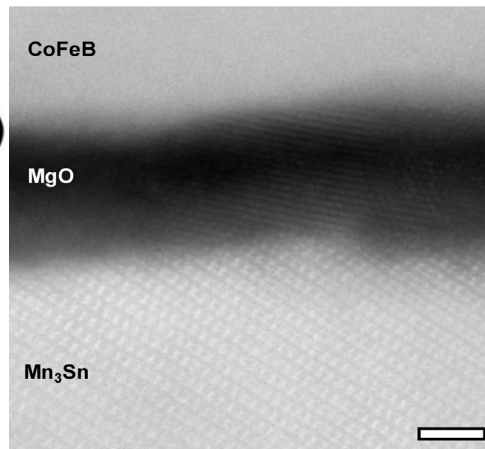
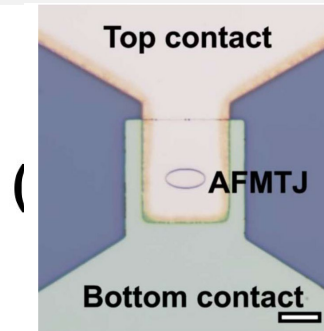
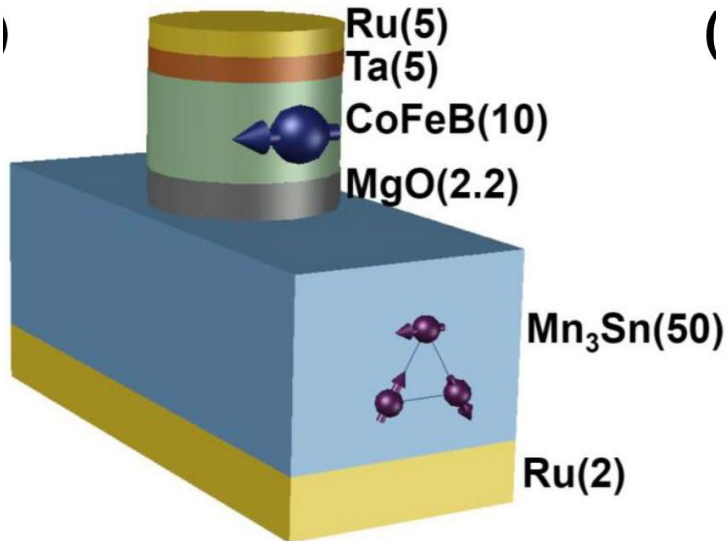


S. Siddiqui, et al, L. Liu, PRL 121, 057701 (2018)

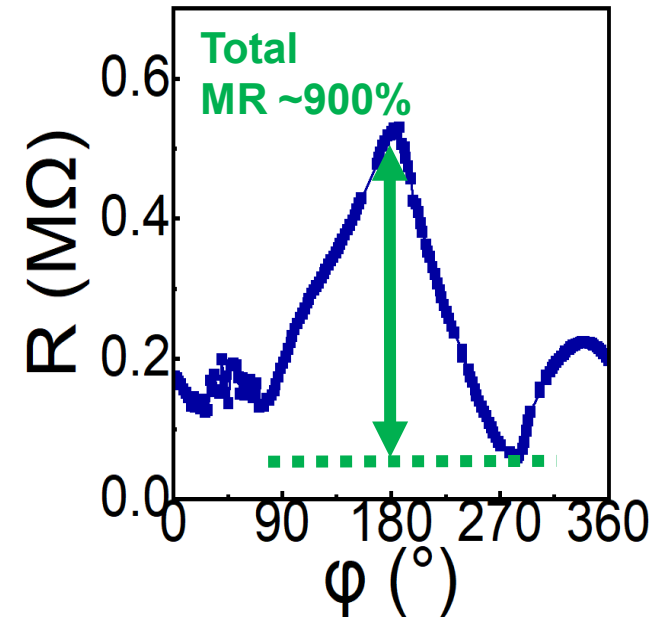
This corresponds to sub-ns switching time in scaled devices (30 nm).

3. Improving the reading performance

Antiferromagnetic MTJ



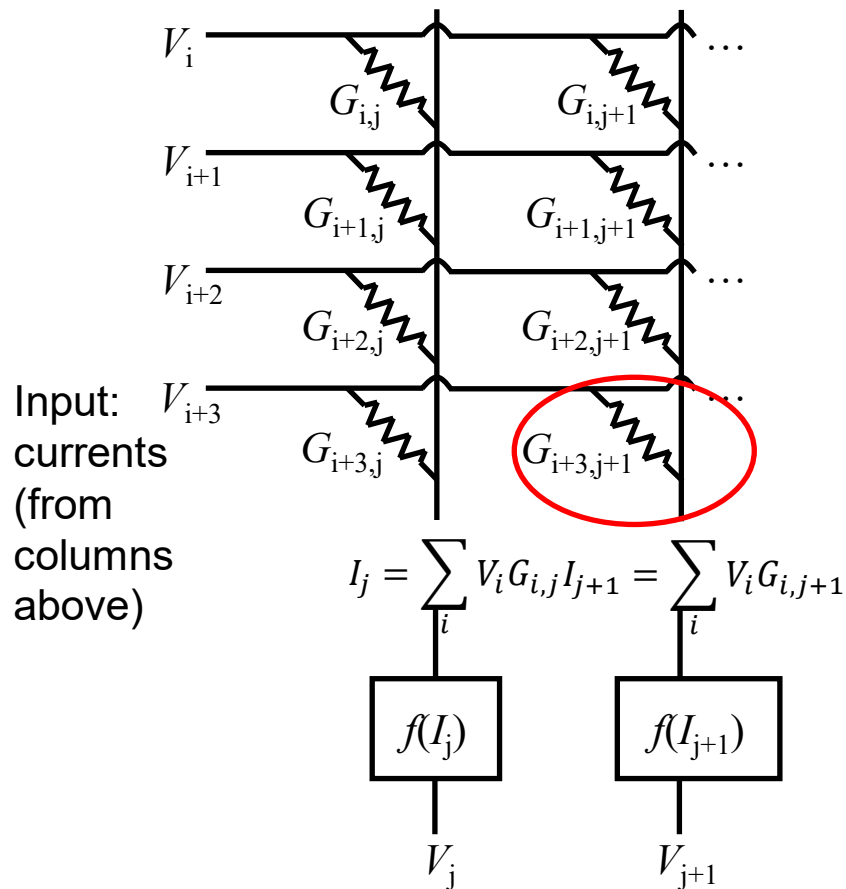
Tunneling magnetoresistance



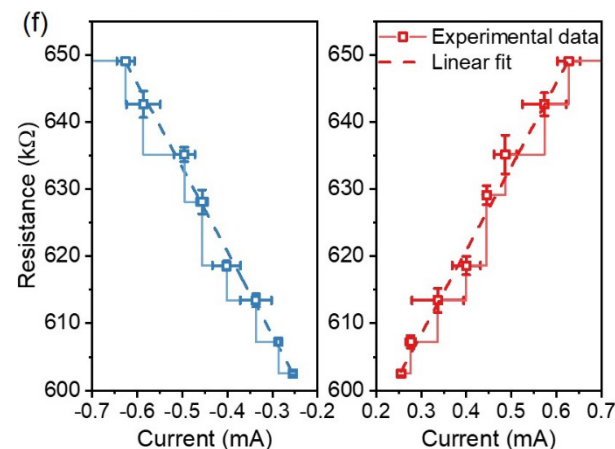
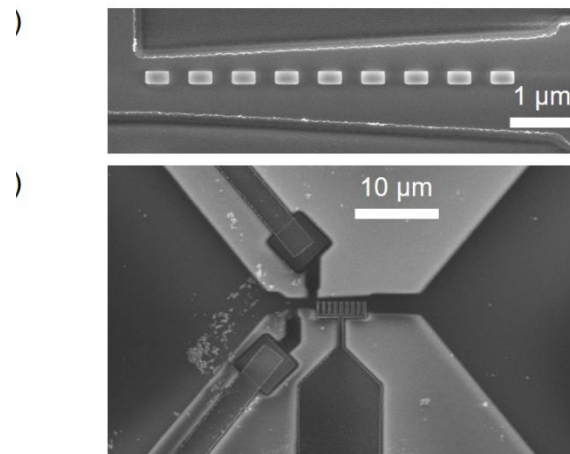
- An higher TMR (close to 1000%) than regular CoFeB/MgO/CoFeB can be achieved with new antiferromagnetic tunnel junctions

4. spintronics for neuromorphic in-memory computing

Architecture for in-memory computing: Neural network



Sumit, et al, NANOARCH.2017.8053724 (2017)



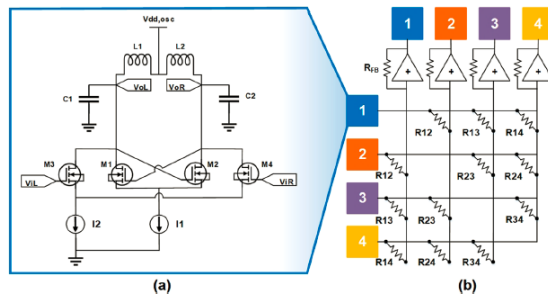
S. A. Siddiqui, et al, *Nano Letters*, (2019).

The output resistance is a linear function of the input current

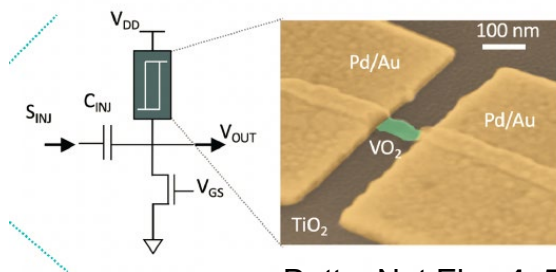
5. Coupled spin oscillators for Ising Machine

Coupled Oscillators Network

LC oscillator

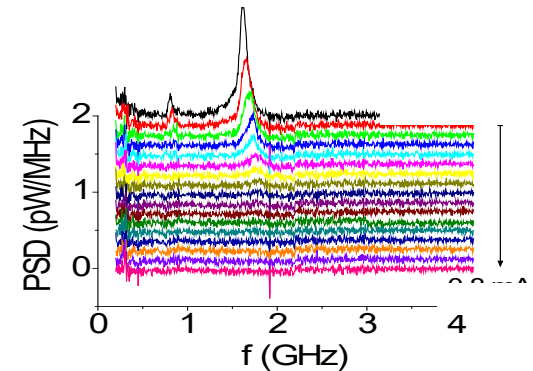
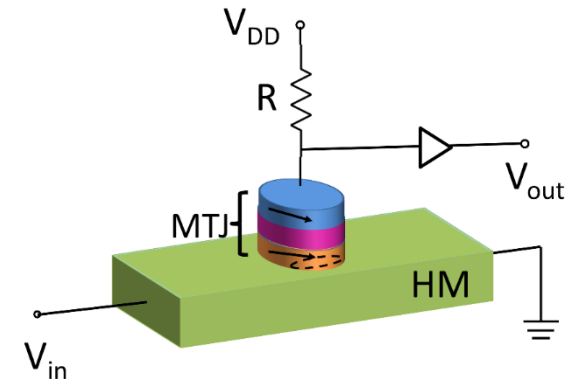


Phase transition oscillator



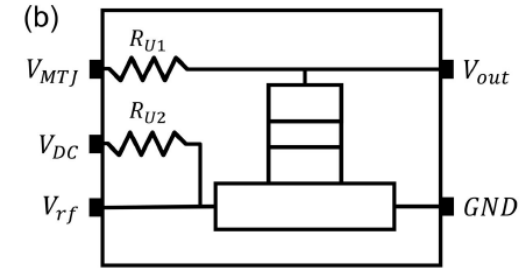
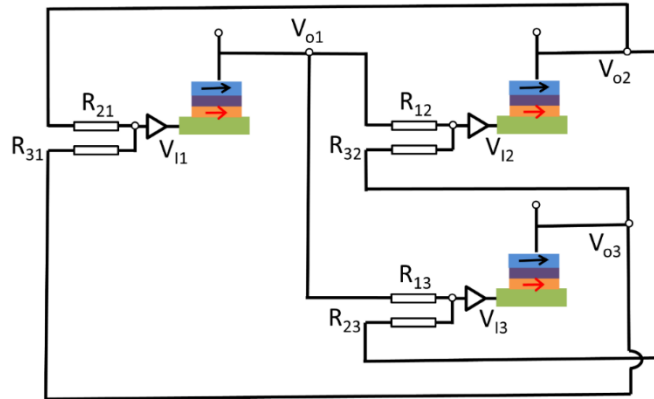
Datta, Nat Elec 4, 502–512 (2021)

GHz nanoscale spin torque oscillator



Liu, Ralph, et al, Phys. Rev. Lett., 109, 186602, 2012

Coupled spin oscillator for Ising Machine



Benchmarking

TABLE II. Performance comparison between the SHNO Ising machine in this work and previous implementations of the Ising machine. Time and energy values are standardized to a size-100 problem. Acronym key: D-WAVE = quantum annealing, OPO = optical parametric oscillator, PTNO = phase transition nano-oscillator.

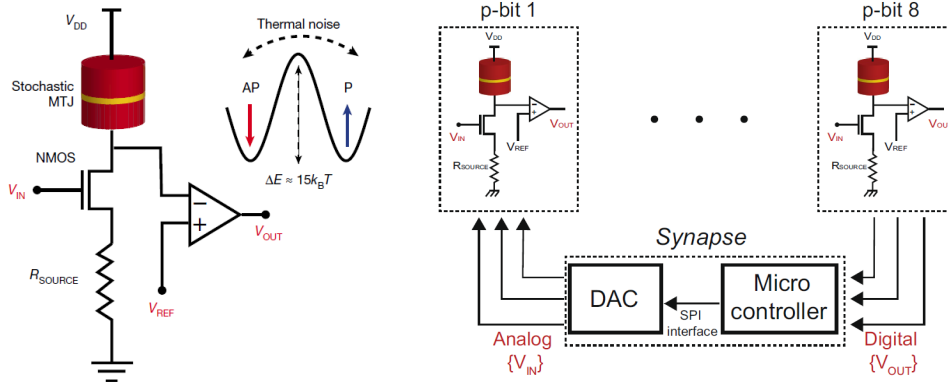
	CPU [8]	GPU [52]	D-WAVE [53]	OPO [4, 54]	LC [6, 55]	PTNO [8, 56]	SHNO [this work]
Solution time	246ms	100 μ s	30ms	2ms	2.5ms	25.5 μ s	359ns
Power	60W	≤ 250 W	25kW	-	2.5mW	1.2mW	486 μ W
Energy to solution	14.8J	≤ 25 mJ	750J	-	6.3 μ J	30.6nJ	175pJ
Energy efficiency (sol/s/W)	6.7×10^{-2}	≥ 40	1.3×10^{-3}	-	1.6×10^5	3.26×10^7	5.73×10^9
Size (one element)	-	-	-	1km fiber	0.1mm ²	0.2 μ m ²	0.024 μ m ²
Room temperature	Y	Y	N	Y	Y	Y	Y

- Advantage with 3-Terminal MTJs: solution time, energy, room temperature operation

Physical Review Applied **17**, 014006 (2022).

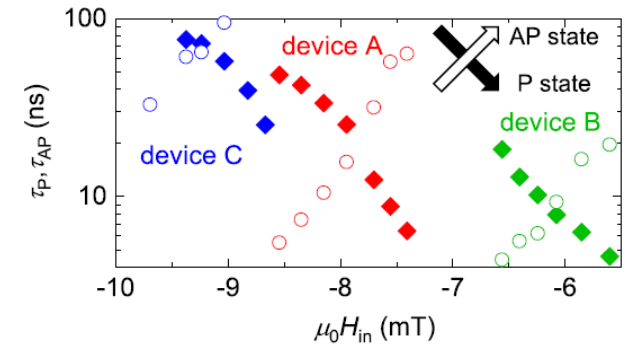
5. Spintronics for stochastic computing

Previous work: P-bit as stochastic neuron (activation)



Boarders et al, Nature, 573, 390 (2019)

Large device to device variation



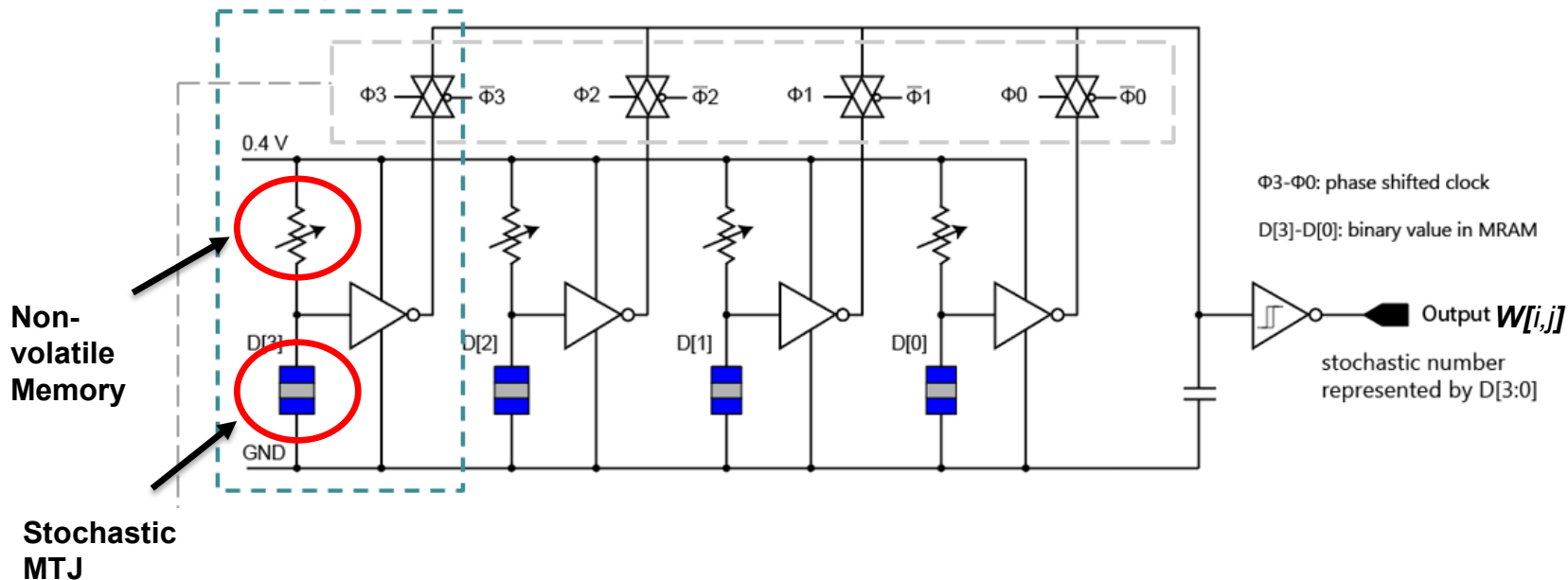
Phys. Rev. Lett. 126, 117202 (2021)

In this literature:

- Demonstration of integer factorization with a 4-node network
- Challenges:
 - × High DA/AD overhead
 - × Susceptible to device variations
 - × Conventional matrix-array multiplication in micro-controller → heavy data movement

Stochastic Computing with Digital Protection

Circuit design

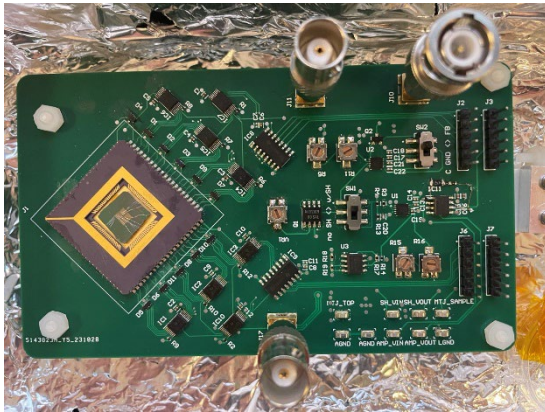
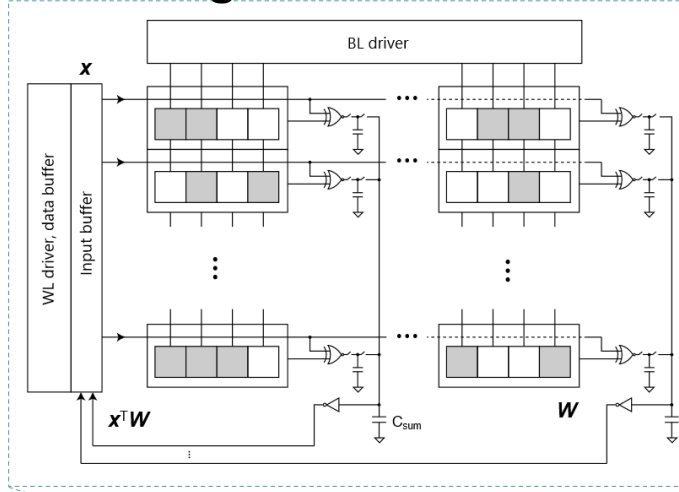


Our approach: P-bit as entropy source for stochastic in-memory computing

- Advantages:
 - ✓ No DA/AD overhead
 - ✓ Digital noise rejection, insensitive to device variation
 - ✓ Highest area efficiency and memory density
 - ✓ In-memory computing

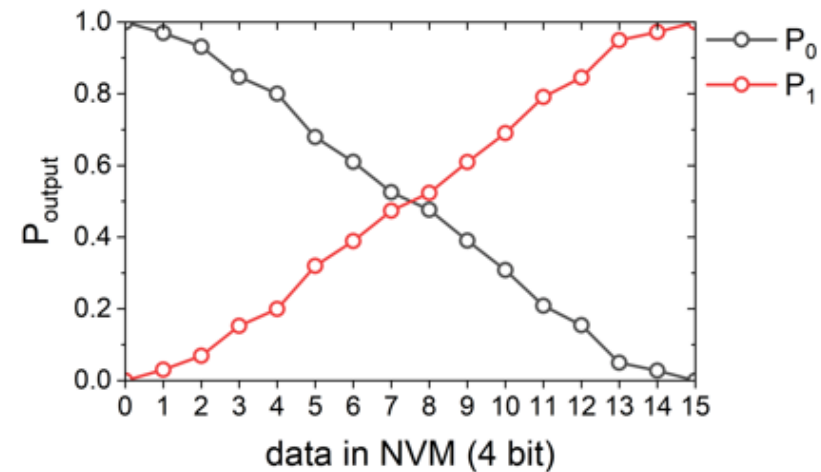
Circuit Design and Preliminary Data

Block Diagram of Neural Network



Preliminary results

Output probability from a 4bit stochastic node



Example of a RNN block:

- Dense weight matrix stored in NVM
- No data conversion, all local computation
- Few transistors, high area efficiency
- Details to be followed by elevator pitch talk this afternoon

Spintronic Material and Devices

- **New materials and physics for better magnetic memory and spin logic**
 - ✓ **Topological insulator for lower power consumption**
 - ✓ **zero moment magnet for faster speed and higher On/Off**
- **Spintronics for new computing schemes**
 - ✓ **Multi-state MRAM for neuromorphic computing**
 - ✓ **Spin torque oscillator for solving optimization problem**
 - **MTJ-based in-memory stochastic computing: No need for DA/AD, Robust against device variation**