Electronics for Extreme Environments

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What is an e*X*treme Environment?

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- High Temperature
- High Energy (RF) Flux
- Radiation (natural)
- Radiation man made (strategic and other man made environments)
- Chemical / Biological /Medical Implants Immersive Environments
- Undersea (High Pressure + Low Temperature)
- Low Temperature
- High shock/g-force/vibration
- High Pressure

Slide courtesy of Tayo Akinwande (MIT)

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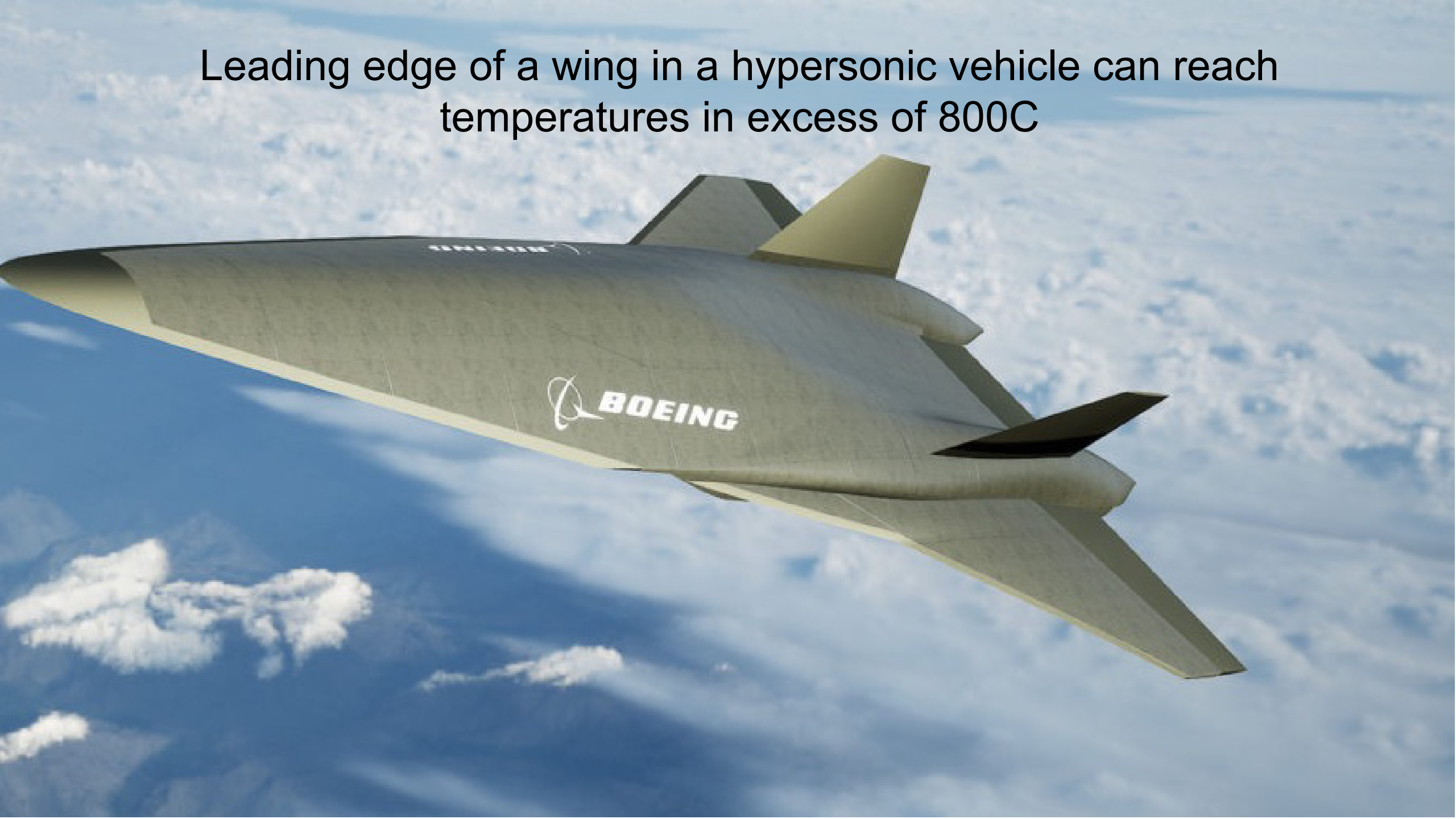
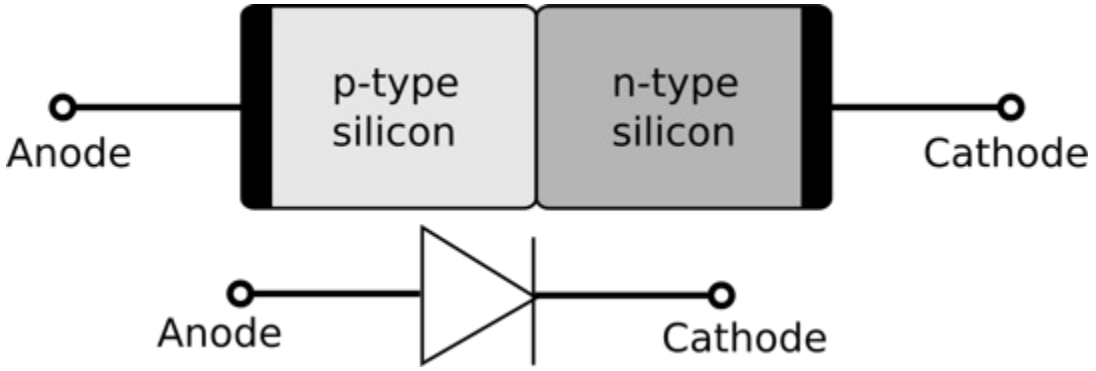
Slide courtesy of Tayo Akinwande (MIT)

Leading edge of a wing in a hypersonic vehicle can reach temperatures in excess of 800C

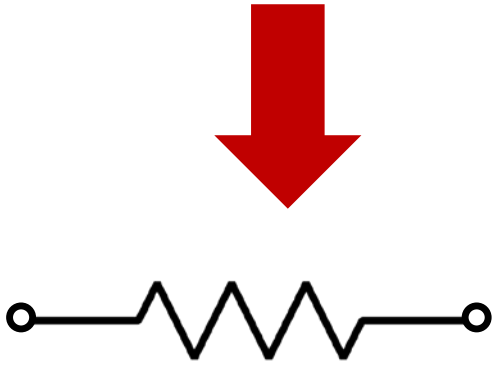


P-N Junction at High Temperature



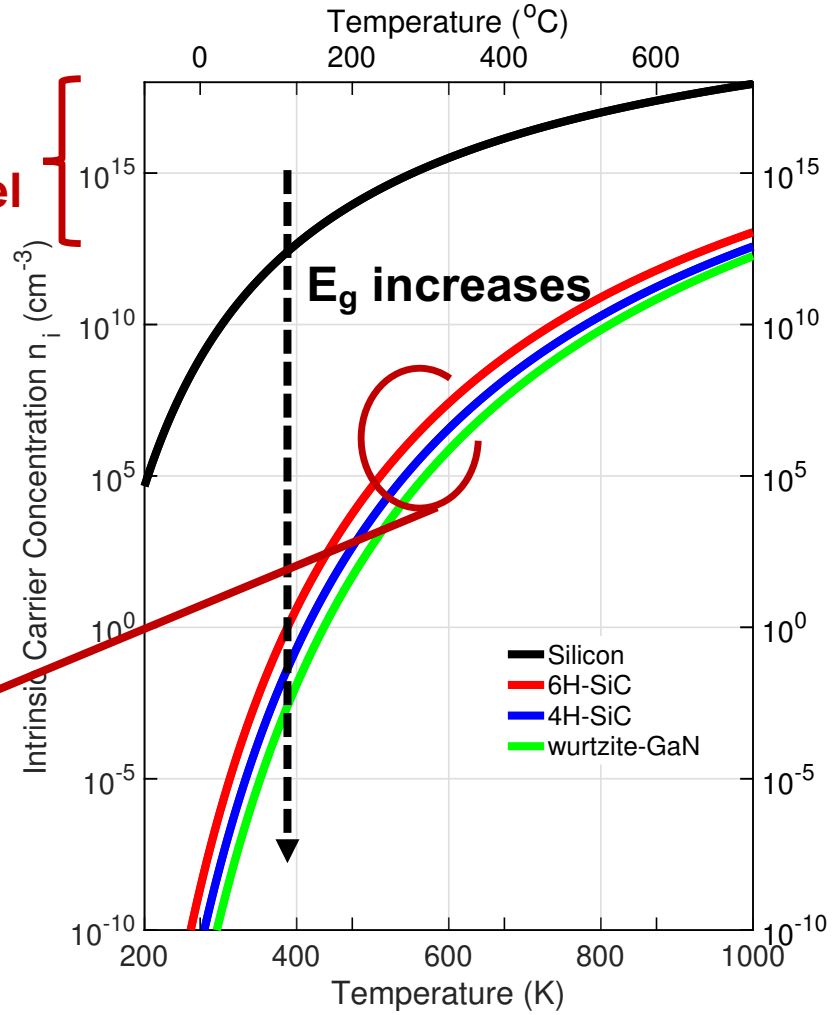
Fundamental limitations:

N_i is close to the level of doping (10^{13} to 10^{18} cm^{-3})!



Wide Bandgap!

Fig. 1 Intrinsic carrier concentration vs. temperature.



SiC is the most mature option

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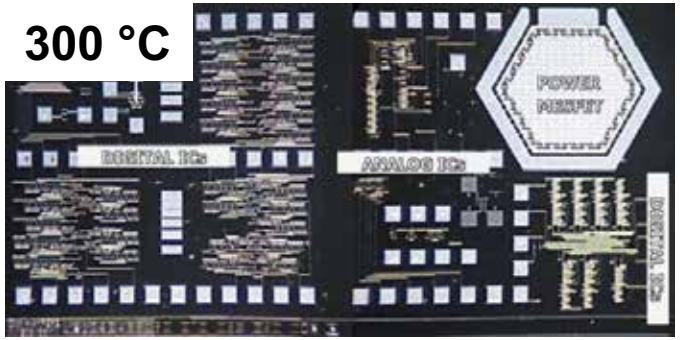
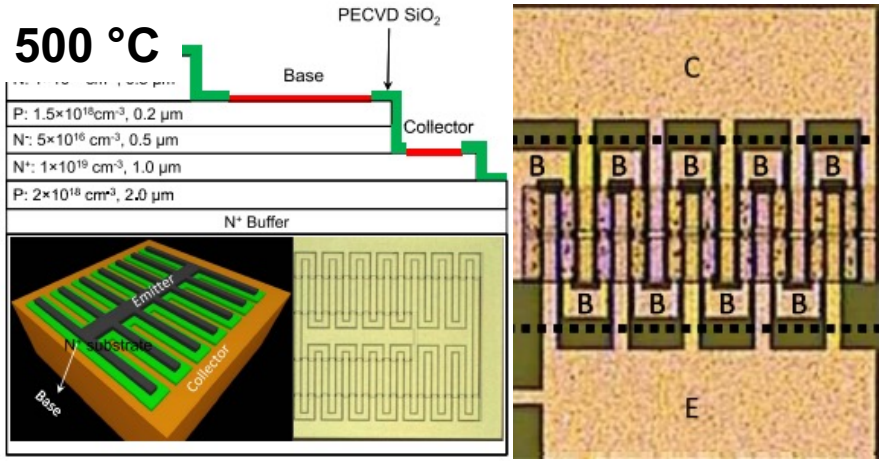
300 °C



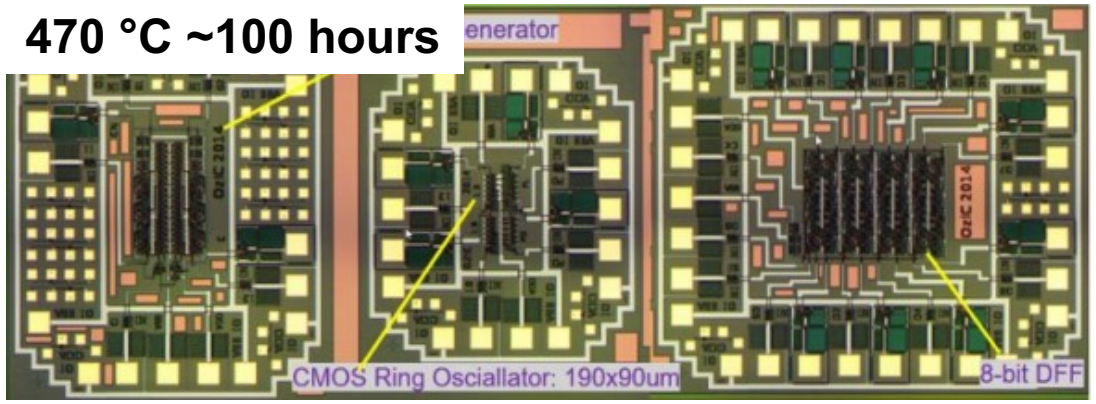
IMB-CNM SiC MESFET [1]

500 °C



KTH SiC BJT [3]

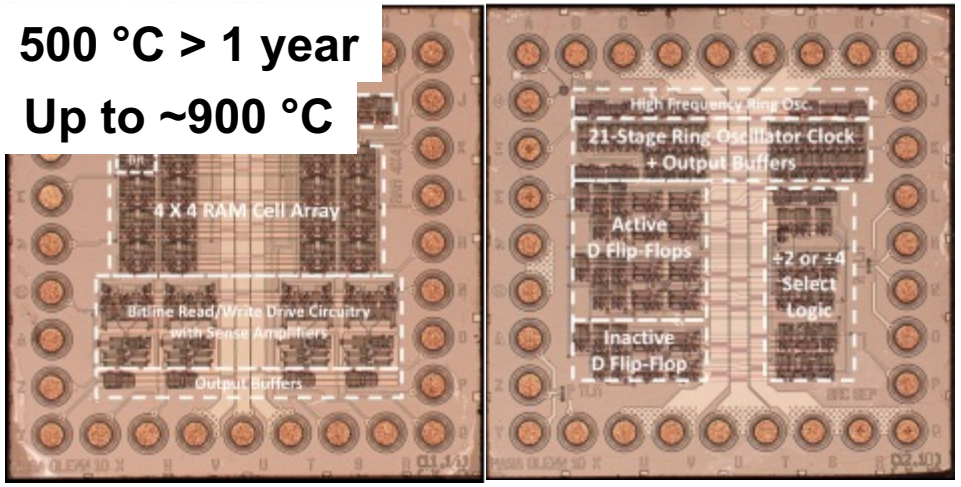
470 °C ~100 hours



Raytheon UK's HiTSiC® CMOS [2]

500 °C > 1 year

Up to ~900 °C



NASA Glenn Research Center SiC JFET [4]

[1] M. Alexandru et al., doi: 10.1109/TIE.2014.2379212.
[2] A. M. Francis et al., doi: 10.4071/2016-HITEC-242.
[3] H. Elahipanah et al, doi: 10.1109/LED.2017.2737558
[4] P. G. Neudeck et al. doi: 10.4071/imaps.729648.

Problems of SiC HT IC

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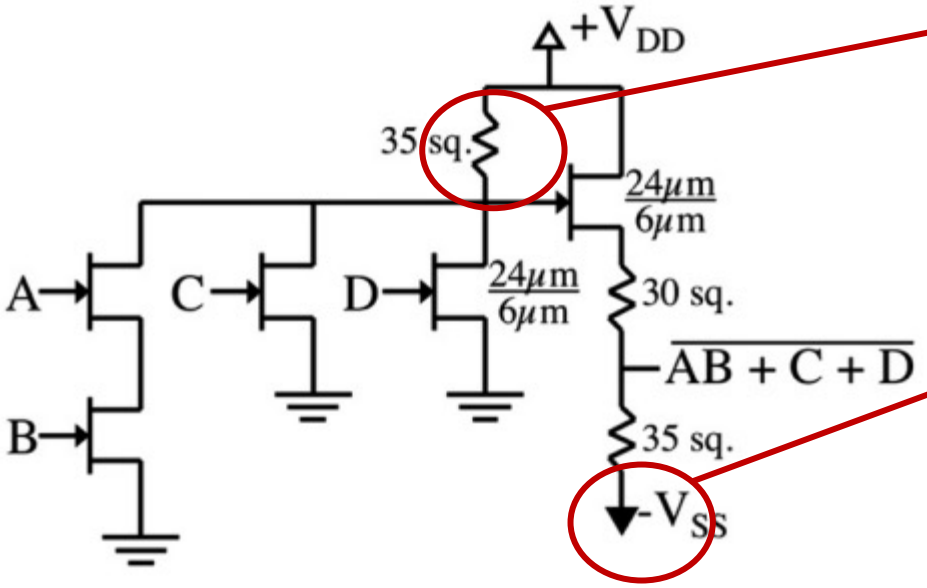
Schematic of SiC JFET logic gate



Resistor-Transistor Logic (RTL)

- Match temperature behavior of resistor and transistor
- Low speed, voltage swing, noise margin.
- Large area overhead

Complex Circuit Design

- Need of V_{SS}
- Need of separate data input control voltage level

Limited Transport Properties → low operating frequency

Need better logic family, as well as normally-off (enhancement-mode) operation!

[1] P. G. Neudeck et al. doi: 10.4071/imaps.729648

HT GaN-on-Si Platform

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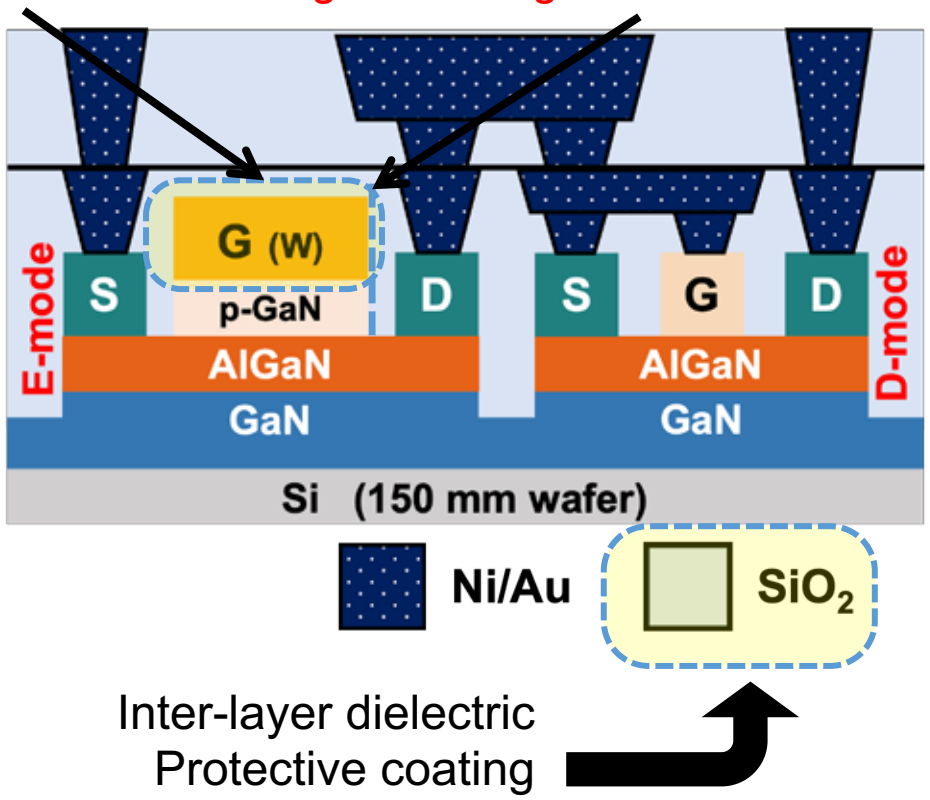
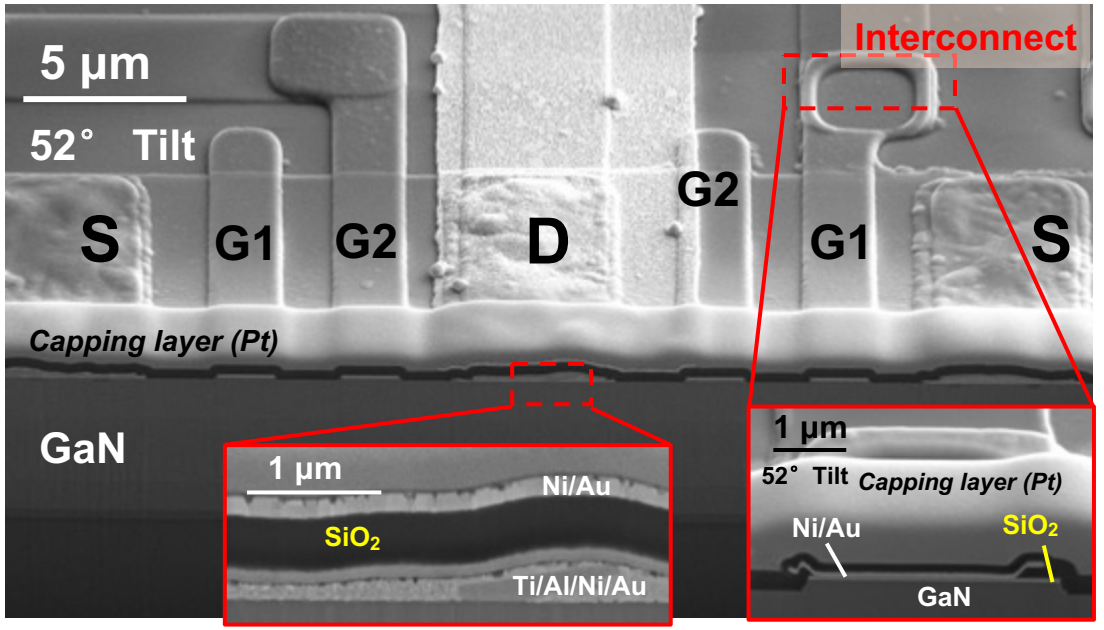
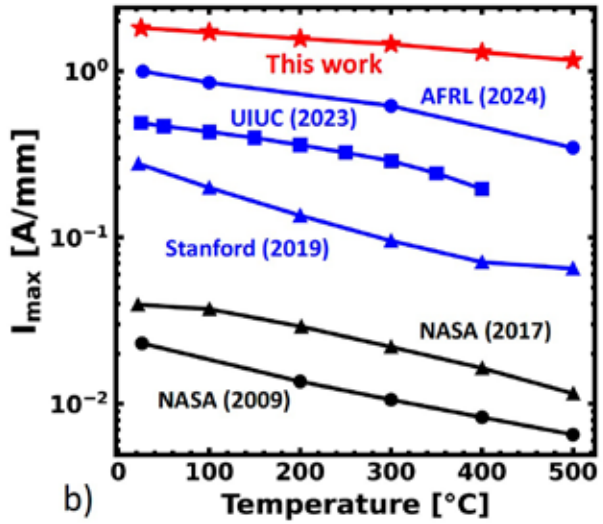
Refractory metal gate
Robust in harsh environment

Self-aligned W/p-GaN, gate-first
Reduced hysteresis and gate leakage in scaled devices

Ion-implanted ohmic contacts (not in this work)







[1] Yuan et al., *EDL*, 2023. [2] Xie et al., *IEDM*, 2022. [3] Yuan et al., *EDL*, 2022. [4] Zhang et al., *IEDM*, 2021.

HT GaN-on-Si Platform pGaN HEMT I-V

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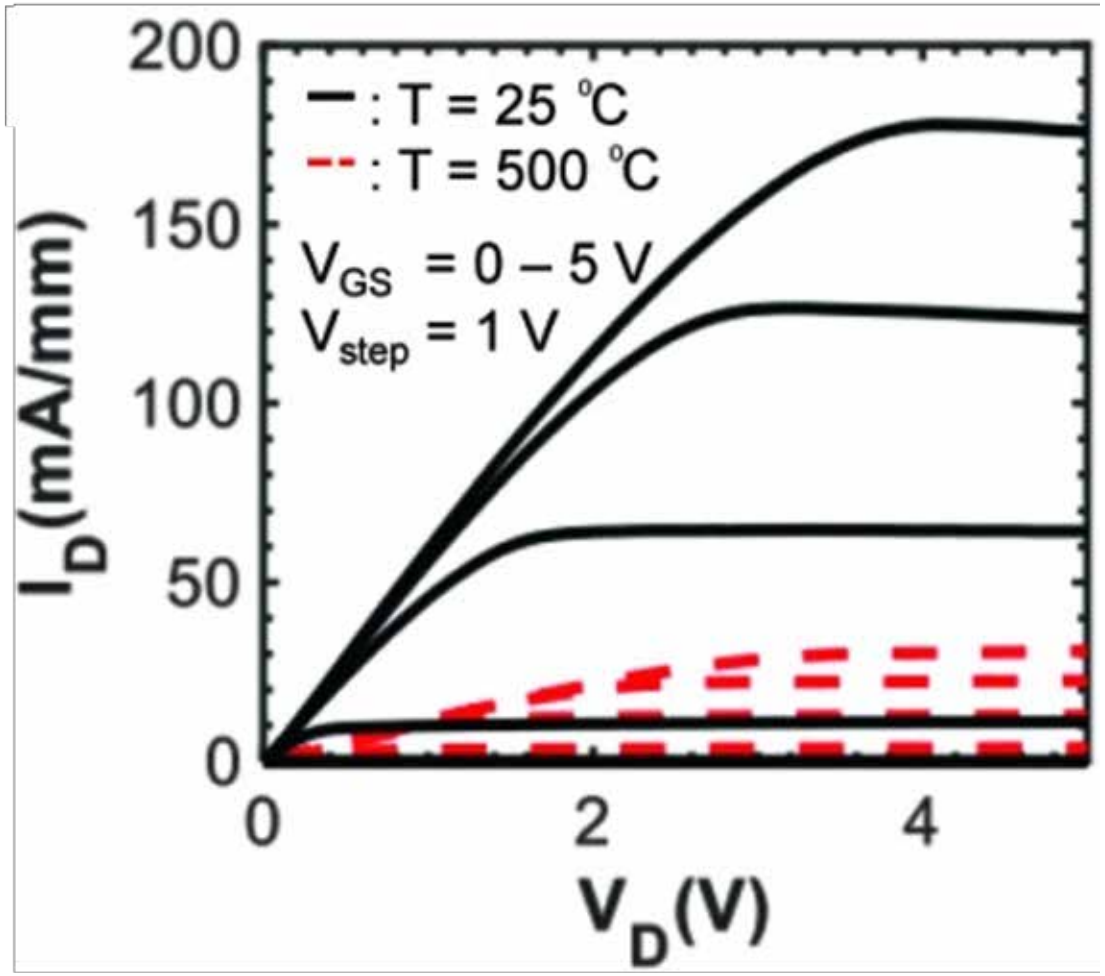

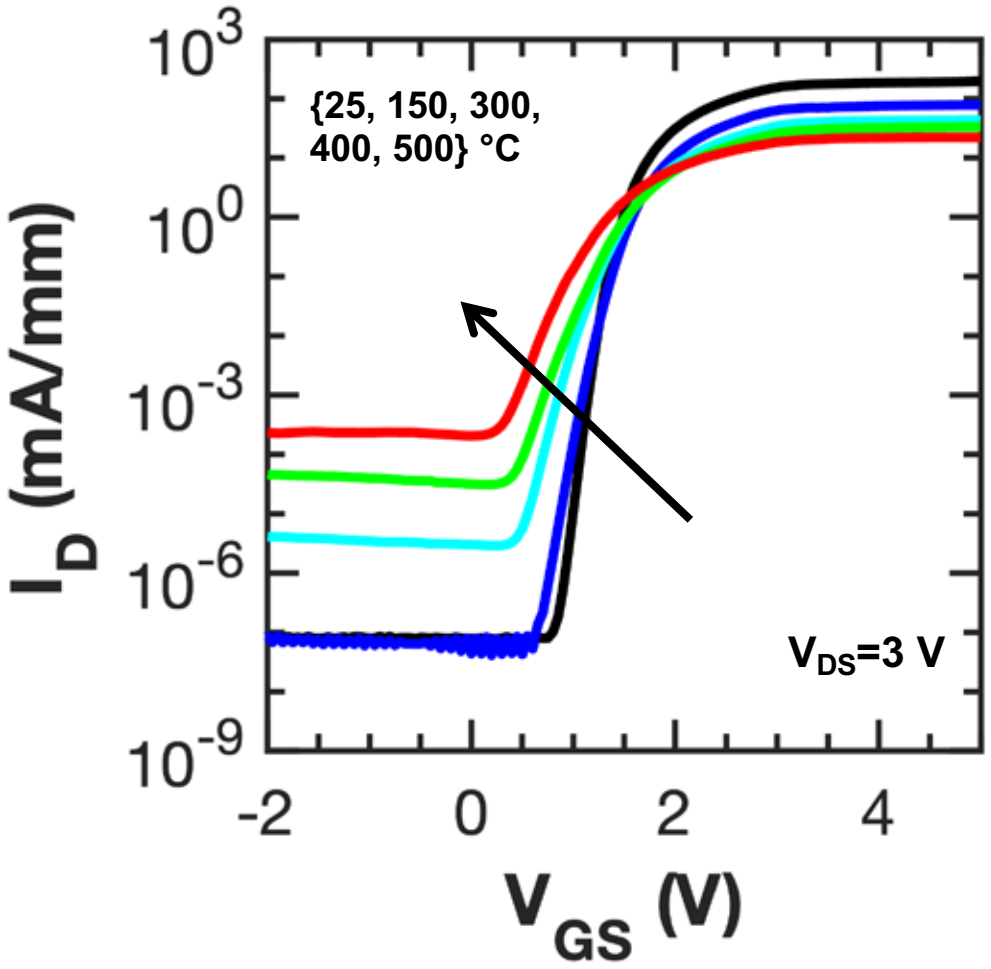

GaN HT Circuit Demonstrations

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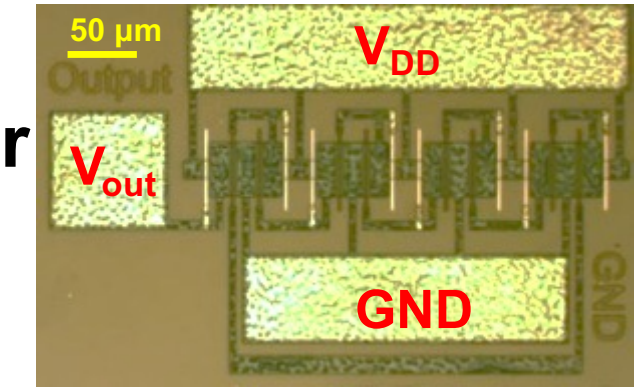
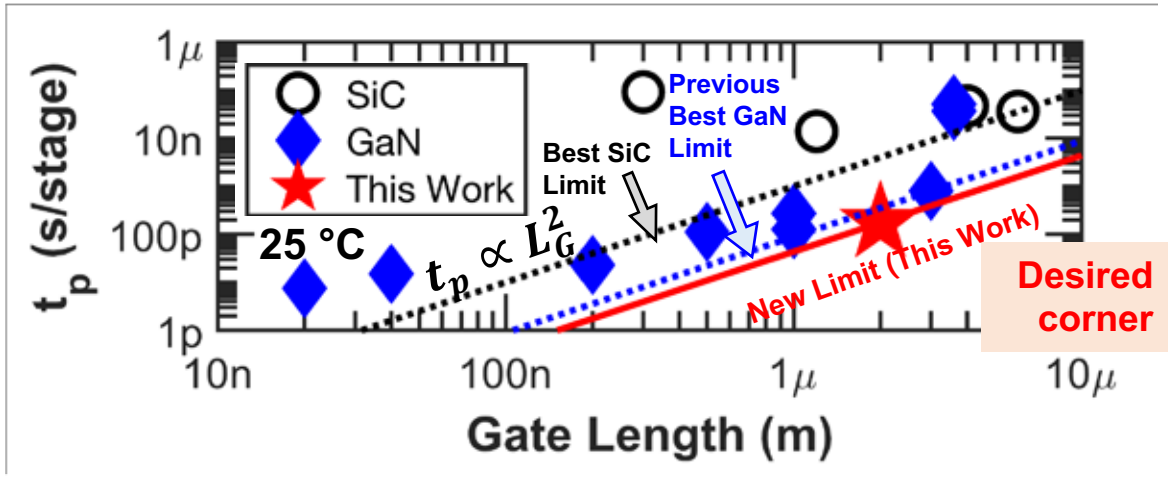
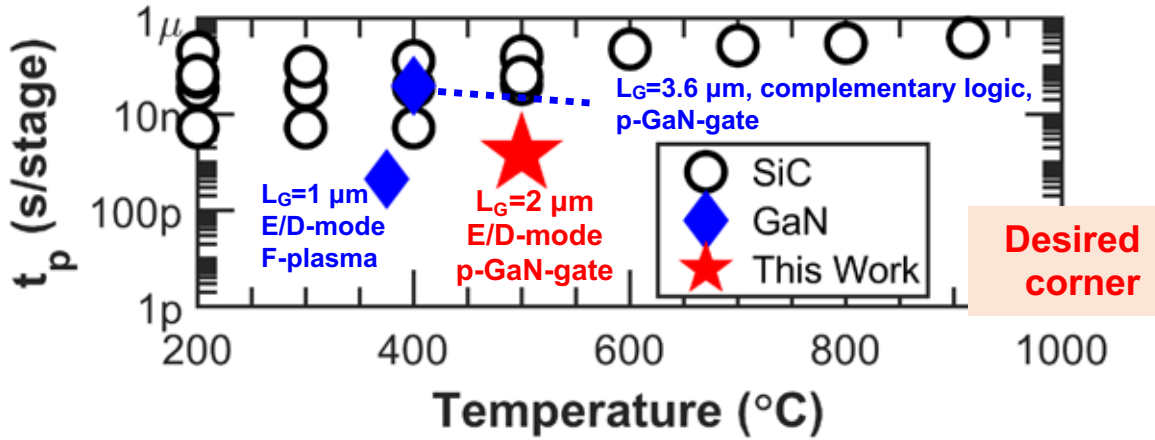
Ring oscillator
(7-stage)







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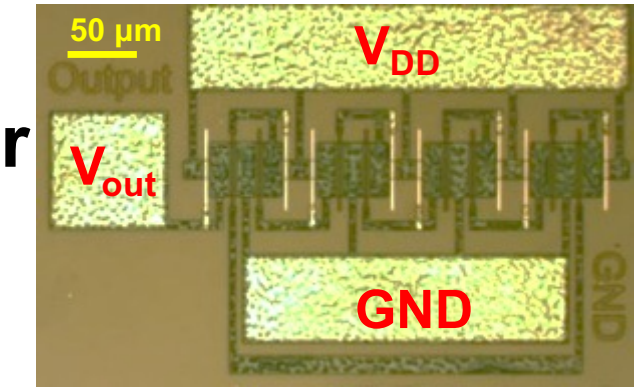
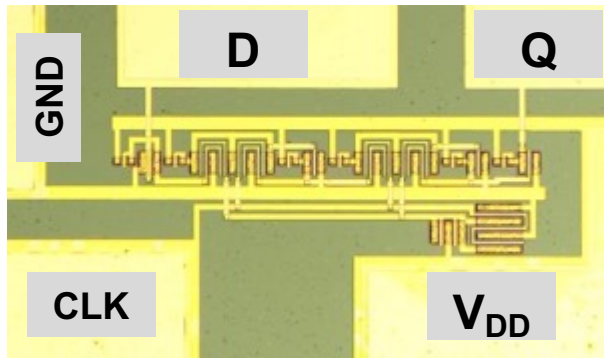
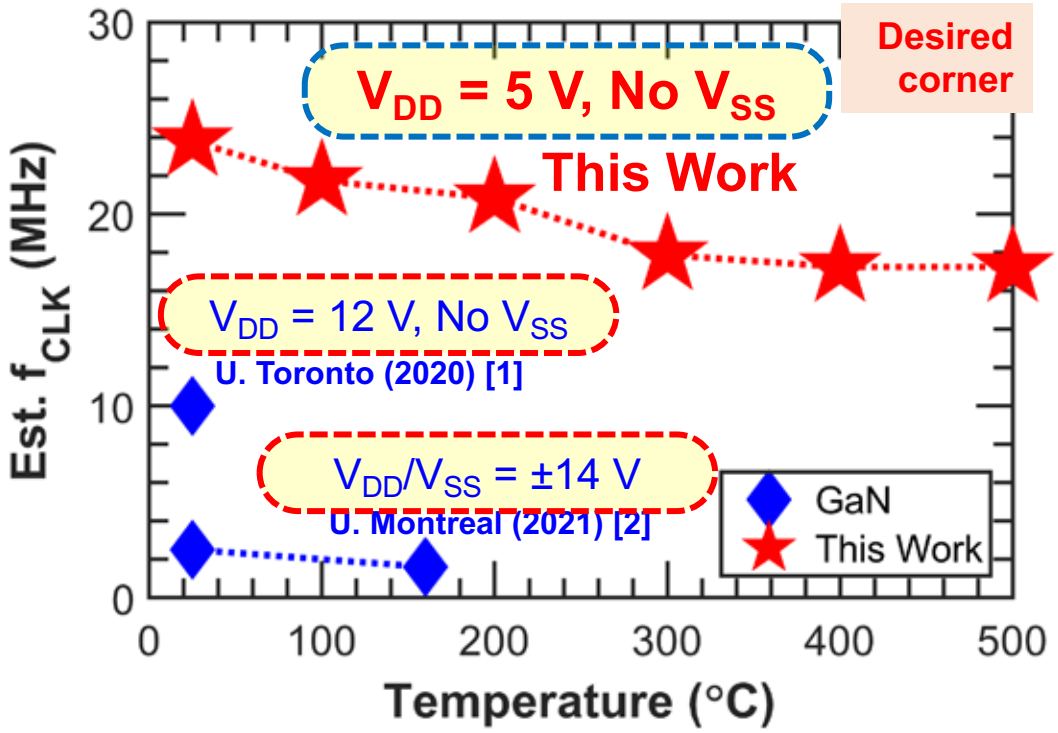


Memory Cell
(D flip flop)



No data on f_{CLK} of SiC D flip flops is available.



[1] Jiang et al., *VLSI*, 2020.
[2] Hassan et al., *Electronics*, 2021.

GaN ROM & SRAM

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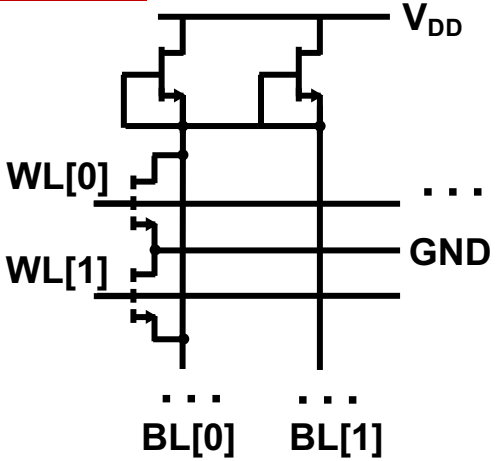
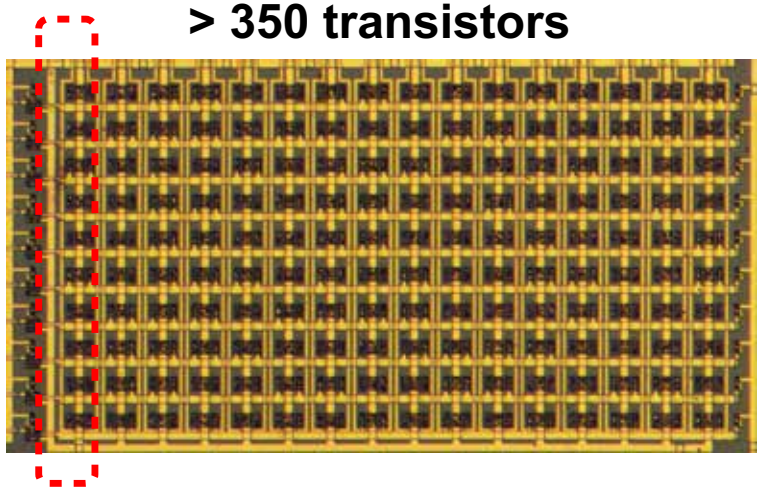
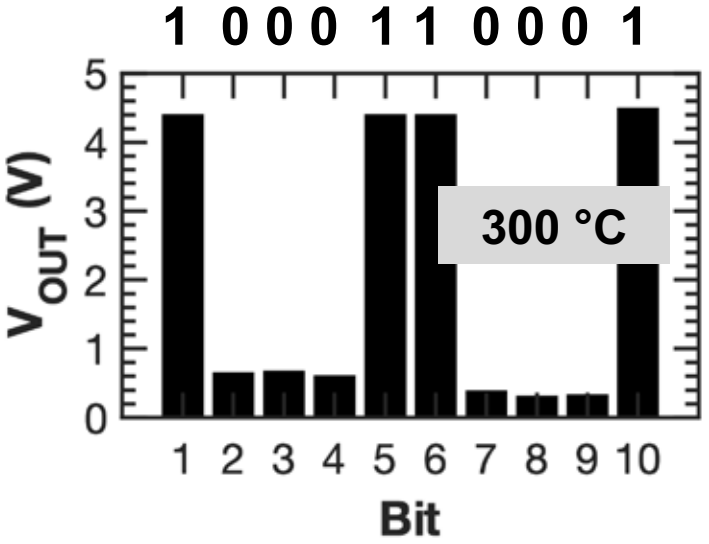
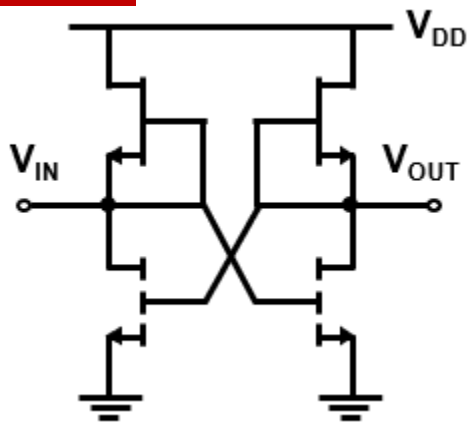
ROM

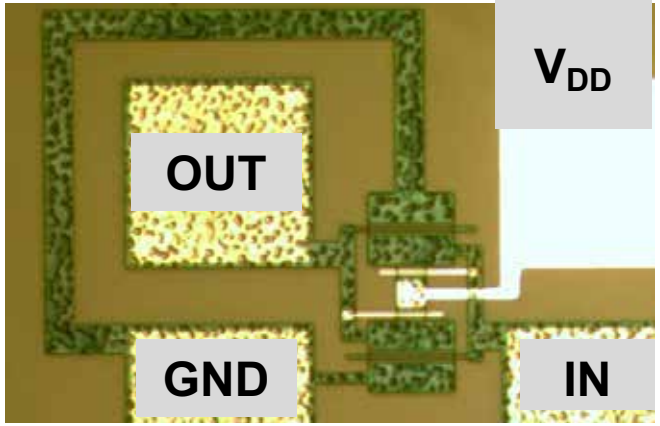


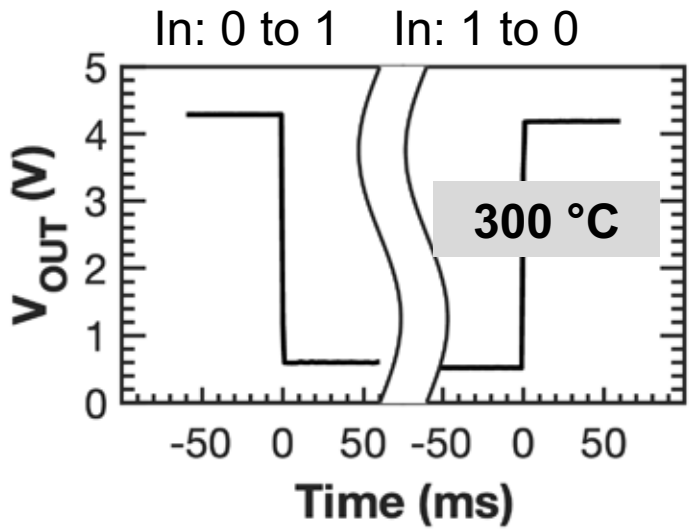




SRAM







GaN Arithmetic Logic Unit

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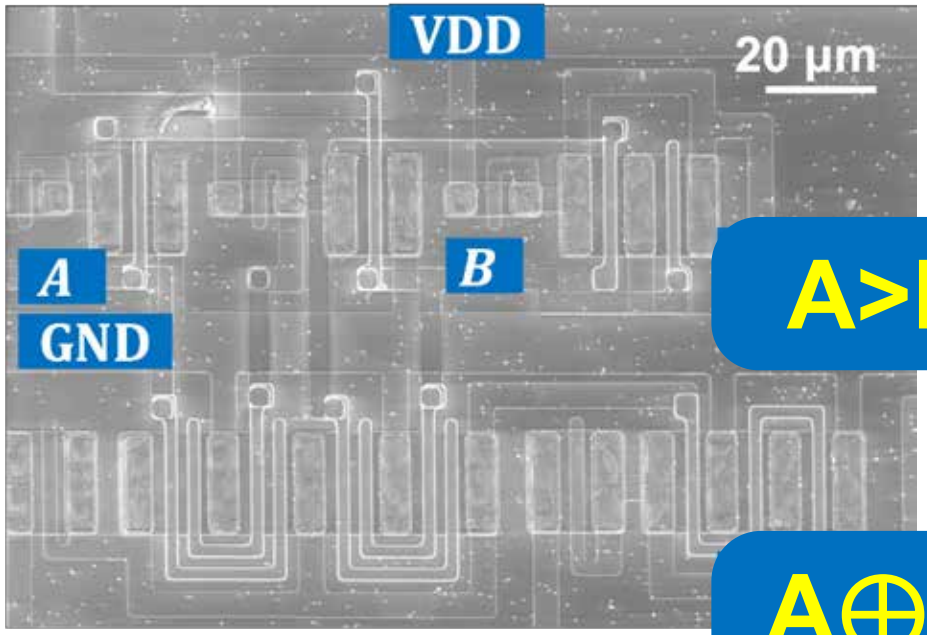
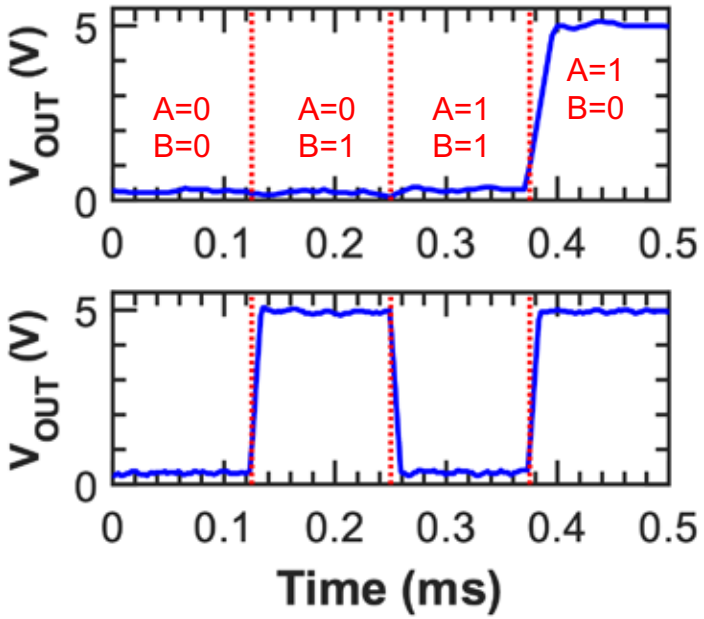


Outputs of ALU

A>B

A⊕B

Operation at 300 °C



For more complex circuits (i.e. microprocessor) we need complete CAD framework!

GaN Computer: Progress

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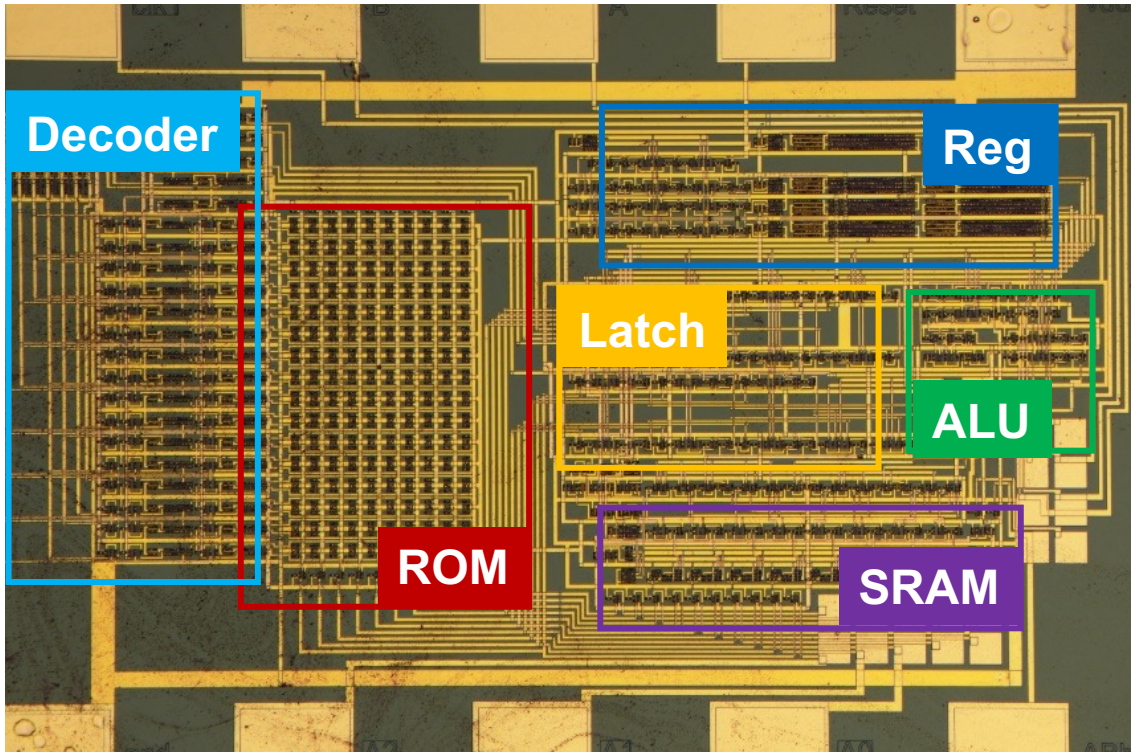
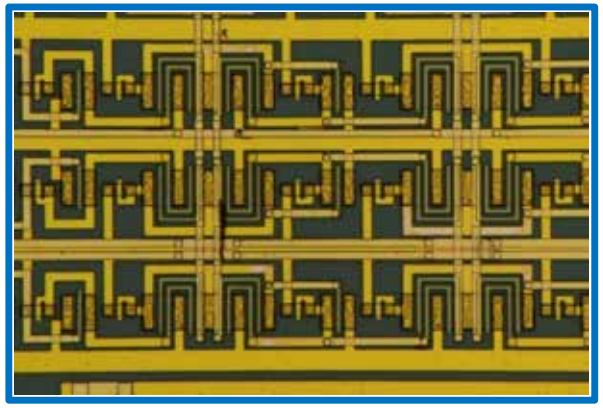
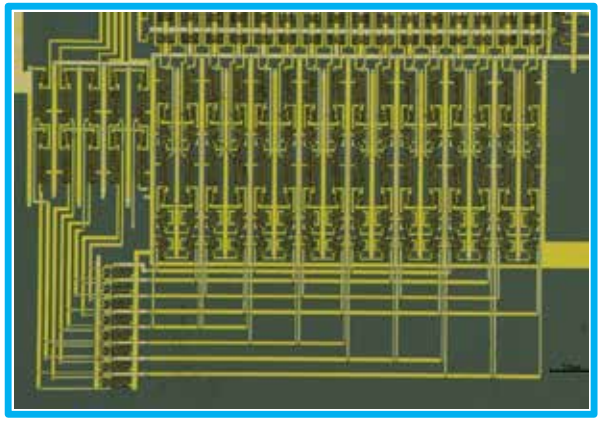
GaN OISC



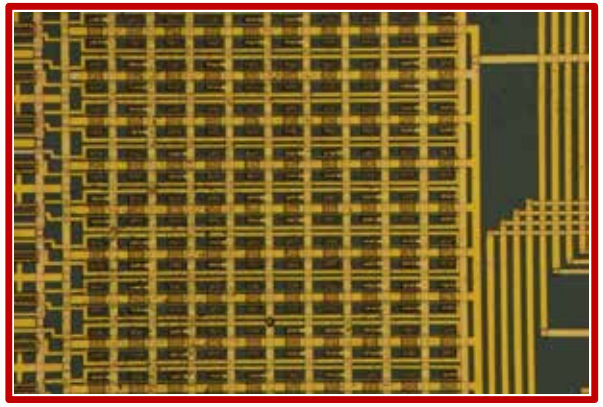
Register Array/Clock Generator



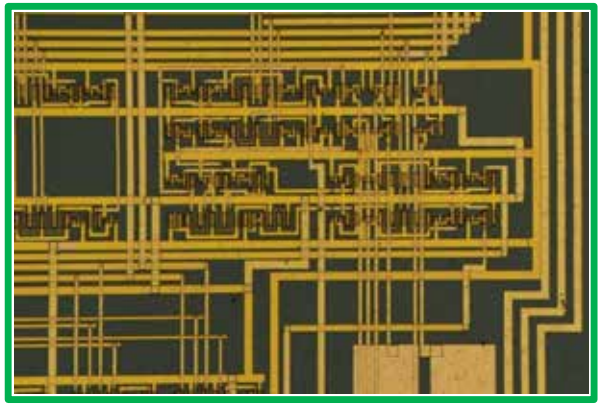
Decoder



ROM array

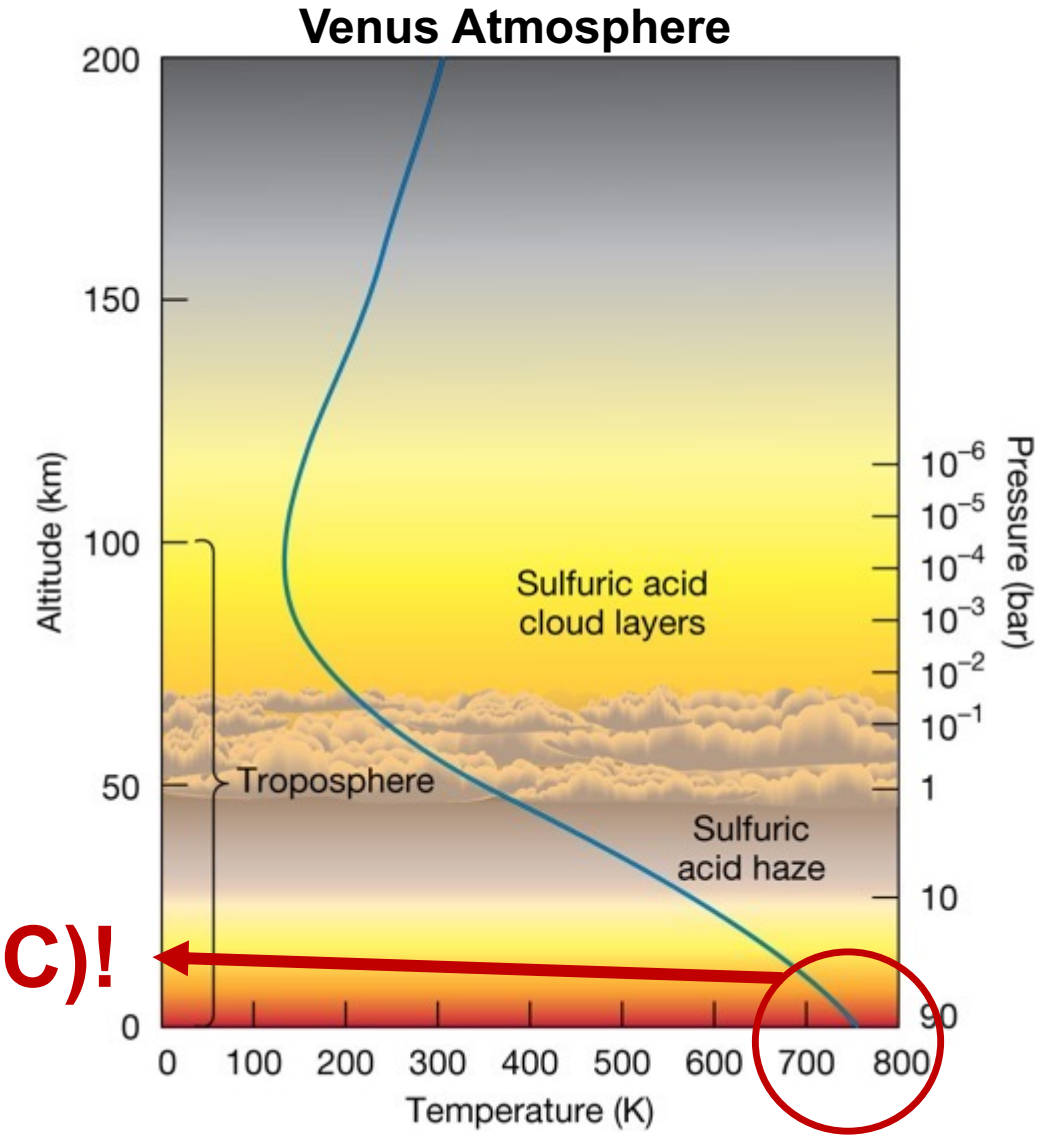


ALU (Arithmetic Unit)



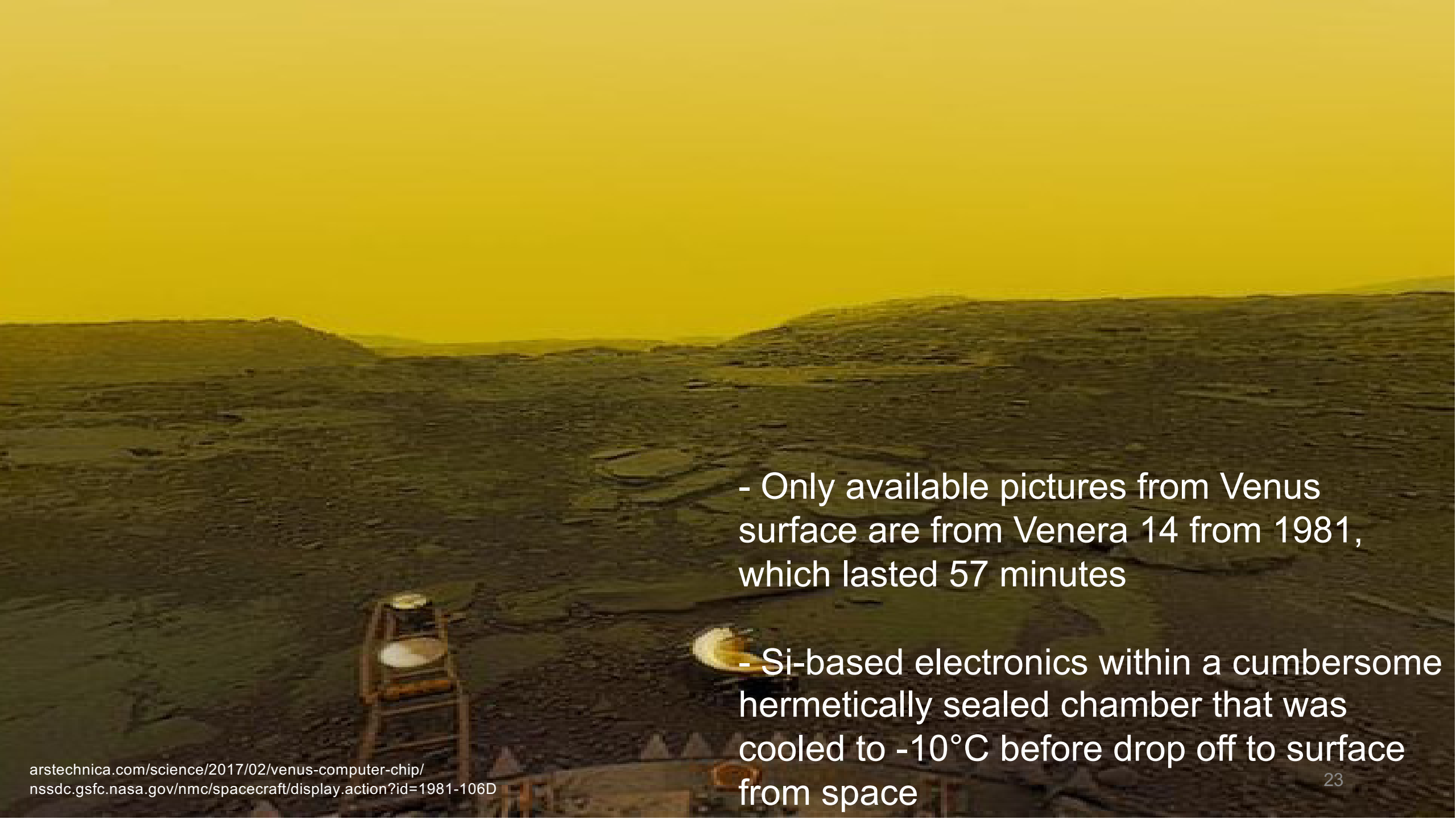
User case example

Venus Exploration



Venus Surface is at 750 K (~500°C)!

[1] "Venus", solarsystem.nasa.gov/planets/venus/.
[2] Jim Brau, *Venus Atmosphere*, physics.uoregon.edu/~jimbrau/astr121.



- Only available pictures from Venus surface are from Venera 14 from 1981, which lasted 57 minutes

- Si-based electronics within a cumbersome hermetically sealed chamber that was cooled to -10°C before drop off to surface from space

arstechnica.com/science/2017/02/venus-computer-chip/
nssdc.gsfc.nasa.gov/nmc/spacecraft/display.action?id=1981-106D

P-GaN/AlGaN/GaN Device in Simulated Venus Environemnt

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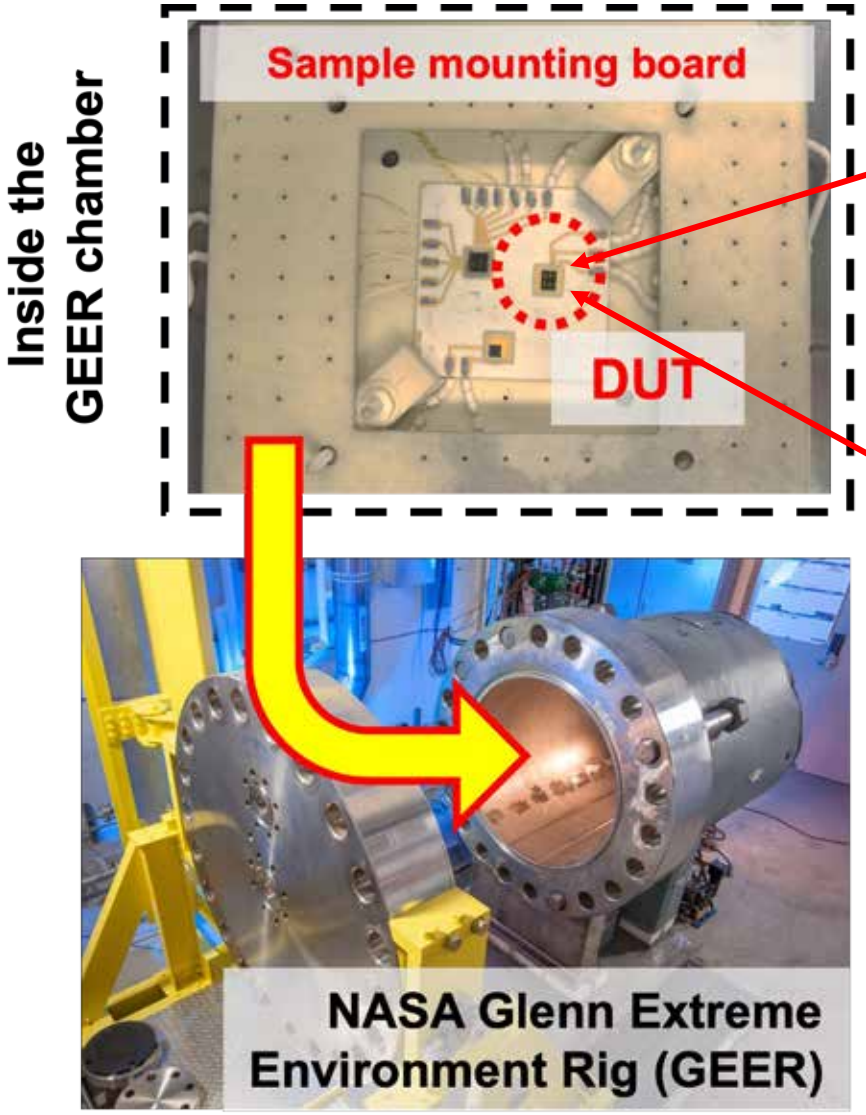

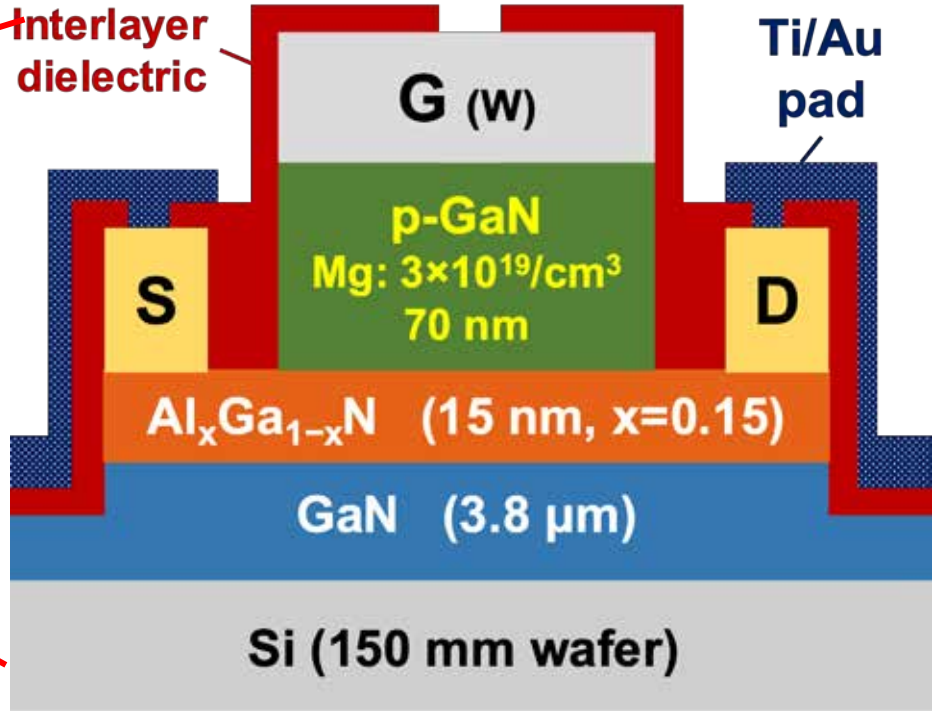

- Simulated Venus environment (465C, 92 atm, $N_2/CO_2/SO_2$) at NASA GEER for 11 days
- Continuous, automated in-situ electrical measurements performed throughout testing period

Device Characteristics at 465°C During *11 Day Venus Testing at GREER*

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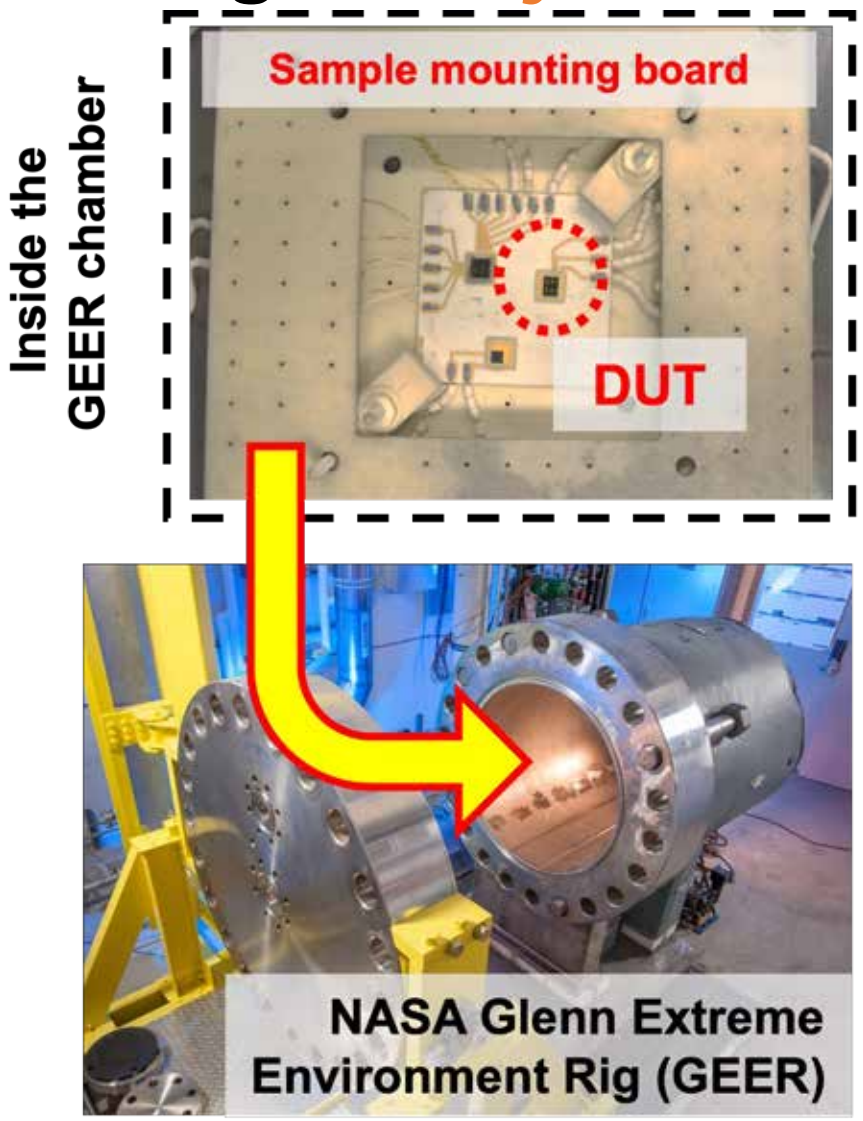

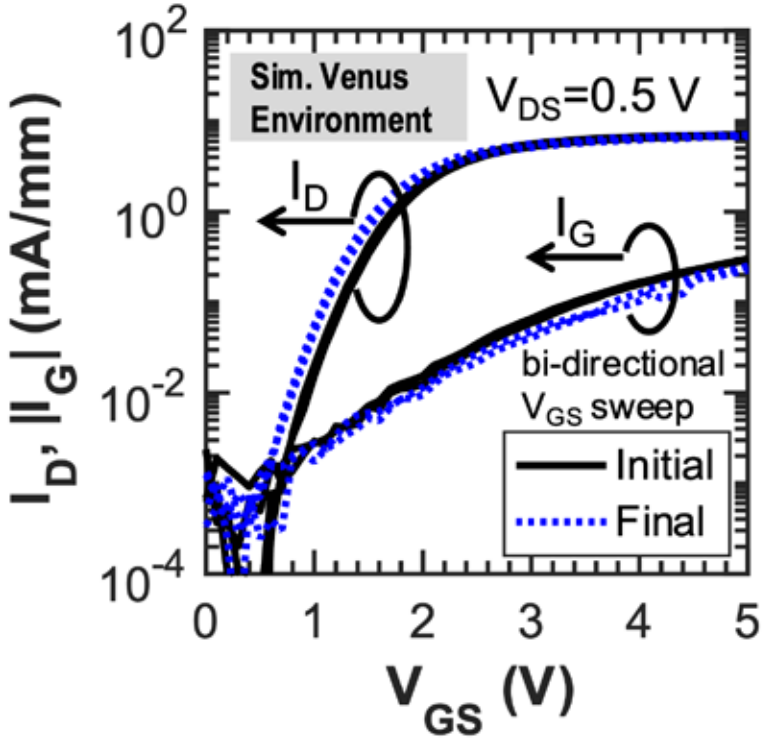

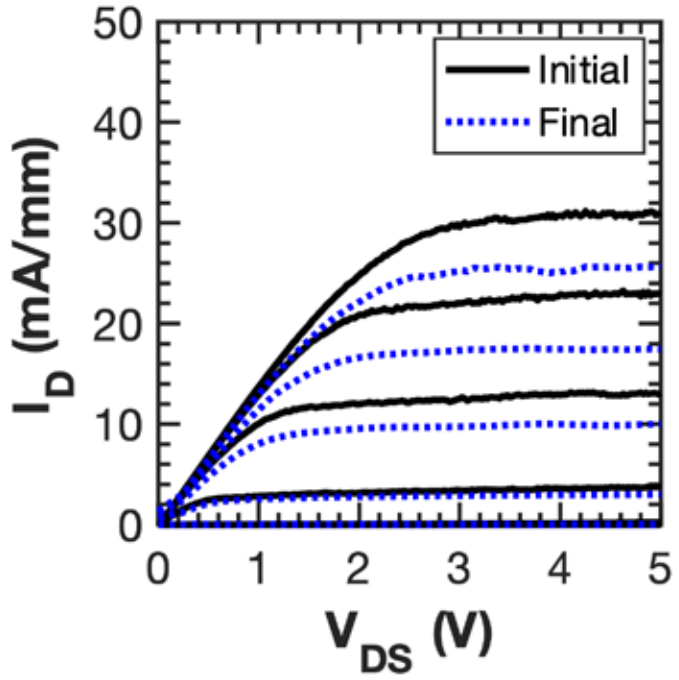

Transfer and output characteristics show little degradation over the full testing period at 465 °C Venus environment

Opportunities…

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- GaN, AlGaN are strong candidates

- Very limited knowledge on degradation mechanisms
- New materials with minimum mobility degradation
- Self-healing materials

- We need transistors, but also sensors, memory, etc
- Circuit complexity has been very limited
- Packaging is critical

Other relevant projects…

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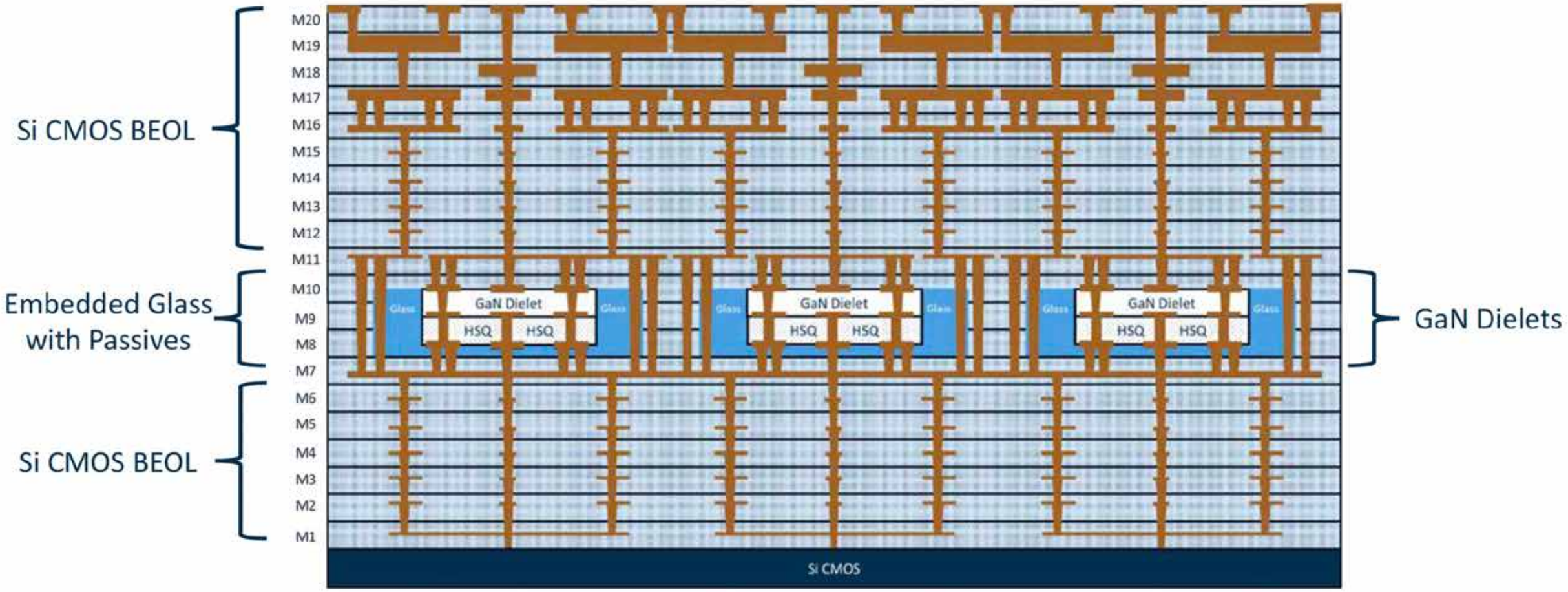
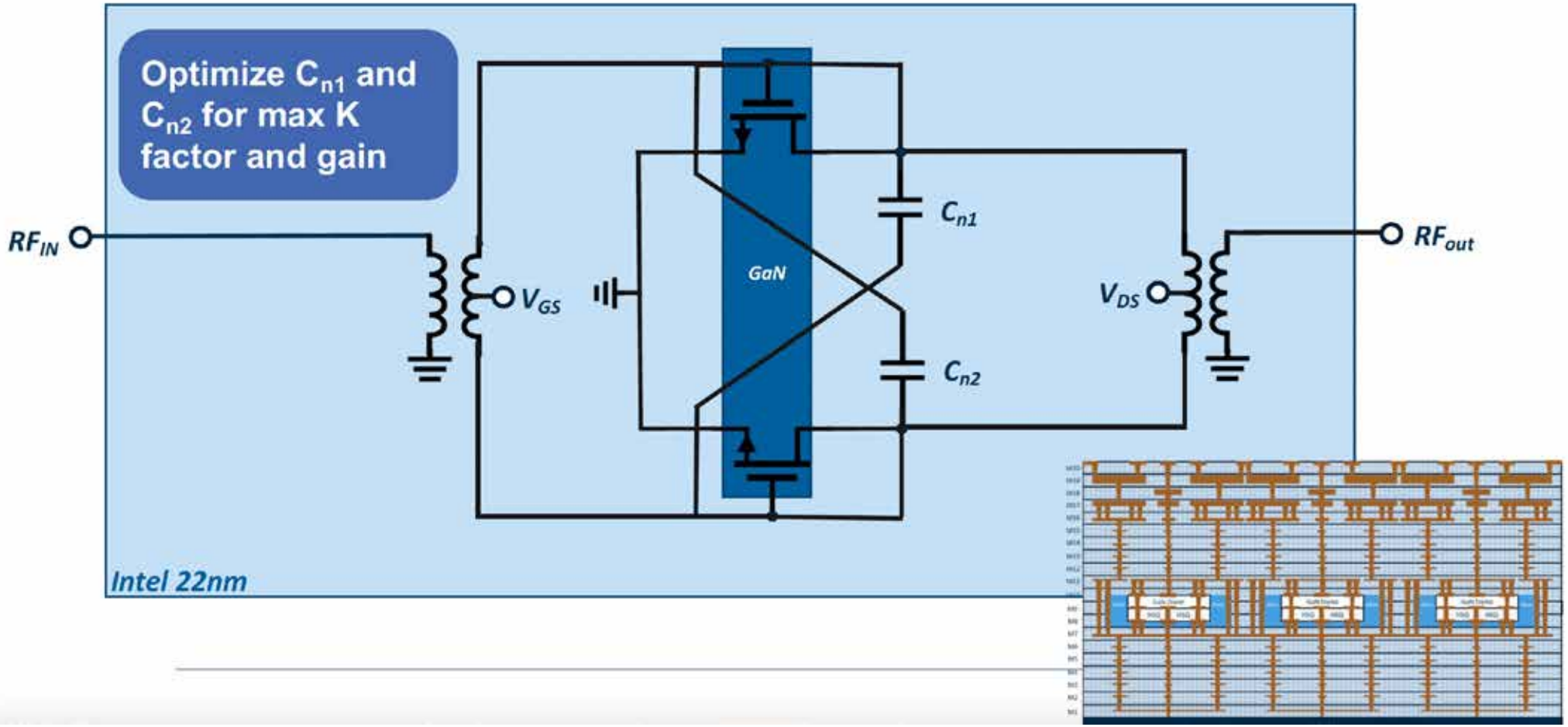


Single chip 3DIC with multiple GaN chiplets leveraging Si BEOL and embedded glass for passives

Intel16 22nm FINFET CMOS Cross Neutralization Capacitor Demonstration



Publications on High Temperature Electronics (2020 – present)

(In reverse chronological order by date of publication)

[1] M. Yuan, J. Niroula, Q. Xie, N. S. Rajput, K. Fu, S. Luo, S. K. Das, A. J. B. Iqbal, B. Sikder, M. F. Isamotu, M. Oh, S. R. Eisner, D. G. Senesky, G. W. Hunter, N. Chowdhury, Y. Zhao, and T. Palacios, "Enhancement-Mode GaN Transistor Technology for Harsh Environment Operation," *IEEE Electron Device Lett.* (accepted).

[2] Q. Xie, M. Yuan, J. Niroula, B. Sikder, S. Luo, K. Fu, N. S. Rajput, A. B. Pranta, P. Yadav, Y. Zhao, N. Chowdhury, and T. Palacios, "Towards DTCO in high temperature GaN-on-Si technology: Arithmetic logic unit at 300 °C and CAD framework up to 500 °C," *2023 Symposium on VLSI Technology and Circuits*, Jun. 2023.

[3] J. Niroula, Q. Xie, M. Yuan, P. Yadav, D. Brock, J. Nichols, J. J. Callahan, and T. Palacios, "High Temperature Modeling of Commercial GaN HEMTs Using an Enhanced MVSG Framework," *Government Microcircuit Applications & Critical Technology Conference (GOMACTech) 2023*, Mar. 2023.

[4] M. Yuan, Q. Xie, J. Niroula, N. Chowdhury, and T. Palacios, "GaN Memory Operational at 300 °C," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2053-2056, Dec. 2022.

[5] M. Yuan, Q. Xie, J. Niroula, M. F. Isamotu, N. S. Rajput, N. Chowdhury, and T. Palacios, "High temperature robustness of enhancement-mode p-GaN-Gated AlGaN/GaN HEMT technology," *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, pp. 40-44, Nov. 2022.

[6] M. Yuan, Q. Xie, K. Fu, J. Niroula, J. A. Greer, N. Chowdhury, Y. Zhao, and T. Palacios, "GaN Ring Oscillators Operational at 500 °C Based on a GaN-on-Si Platform," *IEEE Electron Device Lett.*, vol. 43, no. 11, pp. 1842-1845, Nov. 2022.

[7] N. Chowdhury, J. Jung, Q. Xie, M. Yuan, K. Cheng, T. Palacios, "Performance estimation of GaN CMOS technology," *2021 Device Research Conference (DRC)*, Jun. 2021.

[8] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 820-823, Jun. 2020.

Enhancement-Mode GaN Transistor Technology for Harsh Environment Operation

Mengyang Yuan, John Niroula, Qingyun Xie, Nitul S. Rajput, Kai Fu, Shisong Luo, Sagar Kumar Das, Abdullah Jubair Bin Iqbal, Bejoy Sikder, Mohamed Fadil Isamotu, Minsik Oh, Savannah R. Eisner, Debbie G. Senesky, Gary W. Hunter, Nadim Chowdhury, Yuji Zhao, Tomás Palacios, *Fellow, IEEE*

***Abstract*—This letter reports an enhancement-mode (E-mode) GaN transistor technology which has been demonstrated to operate in a simulated Venus environment (460 °C, ~ 92 atm., containing $CO_2/N_2/SO_2$ etc.) for 10 days. The robustness of the W/p-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) was evaluated by two complementary approaches, (1) *in-situ* electrical characterization, which revealed proper transistor operation (including E-mode V_{TH} with < 0.09 V variation) in extreme environments; and (2) advanced microscopy investigation of the device after test, which highlighted the effect of the stress conditions on the epitaxial and device structures. To the best of the authors' knowledge, this is the first demonstration and comprehensive analysis of E-mode GaN transistors in such harsh environments, therefore establishing the proposed GaN technology as a strong contender for harsh environment mixed-signal electronics.**

***Index Terms*—GaN, transistor, enhancement-mode, mixed-signal, harsh environment, Venus, high temperature, high pressure, corrosive gas, degradation, microscopy**

I. Introduction

ELECTRONICS operating at high temperature (HT), well above the effective 250–300 °C rating of silicon-on-insulator (SOI) technology, are critical in extreme industrial applications (e.g. jet engines, nuclear reactors, deep oil well drilling), as well as in outer space, from the solar system to exoplanetary exploration [1], [2]. A promising solution, which avoids the thermal generation of carriers in conventional Si electronics, is the use of GaN and other wide band gap materials. Thanks to their wide band gap, and superior electrical, mechanical, and chemical properties, these materials have enabled a wide range of devices including transistors, MEMS and solar cells [3]–[5]. GaN electronics have demonstrated excellent performance in extreme environments (from cryogenic to high temperatures) across RF [6]–[8], power [9], [10] and mixed-signal applications [11].

Although initial experiments have highlighted the promising potential of E/D-mode n-FETs (E: enhancement; D: depletion) [12] and complementary (n-FET and p-FET) configurations [13], [14] for GaN HT integrated circuits, more work is needed to improve the performance and robustness of the E-mode transistor. These devices, as exemplified by p-GaN-gate AlGaN/GaN HEMTs, are of significant interest thanks to their possibility of monolithic integration in both E/D-mode and complementary platforms [15]. Given the rapid advancement of GaN HT technology, in particular in mixed-signal circuits [11], [16]–[18], it is an opportune time to examine the robustness of E-mode GaN technology under harsh environments to further optimize these transistors.

This letter presents advancements in GaN HT electronics in the following aspects, when compared to other works and the authors' earlier report [19]: (1) an E-mode GaN transistor technology has been demonstrated, characterized, and analyzed up to 500 °C; (2) testing of the transistor in harsh environment beyond SOI rating (simulated Venus environment), therefore revealing the unexplored potential of E-mode GaN technology for these applications; (3) *in-situ* electrical measurement confirms the continuous operation of the DUT over a prolonged period in harsh environment; (4) after harsh environment testing, a comprehensive microscopy investigation of the p-GaN-gate HEMT structure was conducted. This reveals the intactness/degradation of various device components and offers insights on areas of improvement in device design and fabrication.

II. Transistor Technology

The process flow of the proposed p-GaN-gate AlGaN/GaN-on-Si HEMTs [Fig. 1(a)] begins with the RF magnetron sputtering of tungsten (W, 200 nm) on p-GaN. W and p-GaN are patterned using an optimized low-damage GaN/AlGaN selective etch recipe, while maintaining self-alignment between the two layers [20]. A combination of gate-first process, a refractory metal gate, and self-alignment in metal/p-GaN-gate distinguish the proposed transistor from a conventional p-GaN-gate HEMT. It is noted that, sputtering of W has been reported to cause some damage under the gate for an AlGaN MESFET [21], while its specific effect in p-GaN-gate HEMTs remains to be studied. Nevertheless, the above-mentioned device features have resulted in improved thermal stability, reduced hysteresis [22], and high scaling potential

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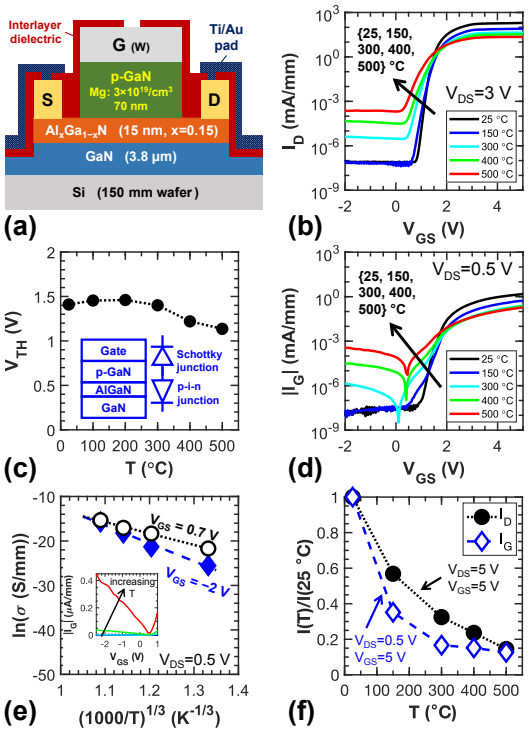

Fig. 1. Temperature dependency of the Tungsten/p-GaN-gate AlGaN/GaN HEMT up to 500 °C. (a) Device structure. (b) I_D *vs.* V_{GS}. (c) V_{TH}. (Inset: A simple two-diode model for the gate region.) (d) $|I_G|$ *vs.* V_{GS}. (e) 2D-VRH model. I_G (linear scale) near $V_{GS} = 0$ V bias is shown in the inset. (f) I_D and I_G *vs.* temperature normalized to their room temperature values, for $V_{DS} = V_{GS} = 5$ V, corresponding to the ON-state of the transistor.

[15]. Next, Ti/Al/Ni/Au (20/100/25/50 nm) ohmic metal stack is deposited by electron beam evaporation and alloyed at 825 °C in N_2 ambient. As an improvement to [19], a SiO_2 layer (200 nm) was deposited using tetraethoxysilane (TEOS) precursor to passivate the device. After via opening, Ti (20 nm)/Au (300 nm) bonding pads were formed.

III. Temperature Dependency

The bare die was characterized in a probe station with a thermal chuck (rating of 500 °C) in air. As shown in Fig. 1(b)–(c), V_{TH} is relatively stable below 300 °C. The small initial increase of V_{TH} from room temperature to 200 °C could be attributed to a higher acceptor (Mg) ionization ratio in p-GaN at increasing temperature. Above 300 °C, a decrease in V_{TH} is observed. The gate region may be modeled as two back-to-back junctions [Fig. 1(c) inset] [23]. The trend of V_{TH} can be explained by the lower forward turn-on voltage of p-i-n junction, and reduced Schottky barrier height.

The gate leakage current characteristics is shown in Fig. 1(d). Below the turn-on voltage of the p-i-n junction, the vertical junction current is blocked by the p-i-n junction. The gate leakage current is dominated by the surface current (two-dimensional variable range hopping, 2D-VRH), as shown in the good fit of $\sigma \propto \exp\left(-T^{-1/3}\right)$ [Fig. 1(e)] [23]. Therefore, I_G increases with temperature. Here, a reasonable approximation for 2D-VRH was made using I_D-V_{GS} data at a small $V_{DS} = 0.5$ V. At highly positive V_{GS}, which corresponds to the ON-state of the transistor and the forward bias regime of the p-i-n junction, the vertical junction current dominates. The turn-on current I_G decreases with increasing temperature due to increased resistance in the drift region of p-i-n junction. I_G shows a similar trend as I_D up to 500 °C due to the reduced mobility [Fig. 1(f)] [24].

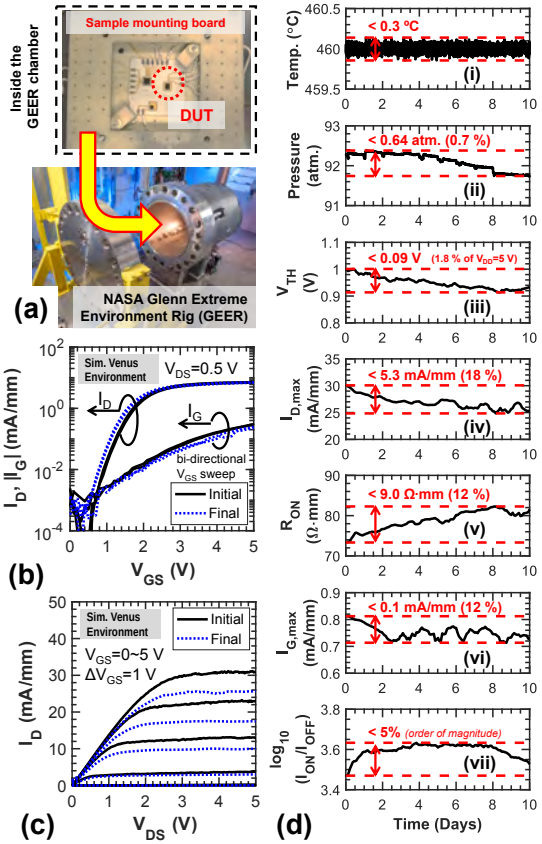

Fig. 2. (a) Setup which allows for the *in-situ* measurement of the DUT in a simulated Venus environment. (b)–(c) Transfer and output characteristics of the DUT for the initial measurement and the final measurement of the DUT in the simulated environment. (d) Variation of (i)–(ii) chamber conditions and (iii)–(vii) key transistor metrics during the reported duration of the test. For each metric, the absolute peak-to-peak value (in parenthesis: percentage of the peak-to-peak value with respect to the initial value, unless otherwise stated) are labelled.

IV. Robustness in Harsh Environment

The device under test (DUT) was packaged using HT-rated components [2], [19] and placed in a simulated Venus environment (460 °C, ~ 92 atm., mainly CO_2/N_2, traces of SO_2 [25]) for 11 days in the NASA Glenn Extreme Environments Rig (GEER) [Fig. 2(a)] [26]. The length of 11 days excludes ramp up and cool down times, and is pre-determined by the test facility. A burn-in effect was observed in the transistor characteristics over the first day of the test, where $I_{D,max}$ started from 5 mA/mm (first instance of Venus conditions being met) and experienced large fluctuation before settling down at 30 mA/mm (at the time instance defined as day 0). In this letter, the data presented is taken from the remaining 10 days. An automated setup ensured that *in-situ* measurements of the DUT could be made at regular time intervals (≈ 70 min.). Given that the measurement setup was shared among several devices (through a switching matrix), the DUT of this work was left unbiased during each measurement. A comparison of the DC characteristics [Fig. 2(b)–(c)] reveals that good transistor operation was maintained at the end of the test. The chamber temperature and pressure were accurately maintained over the

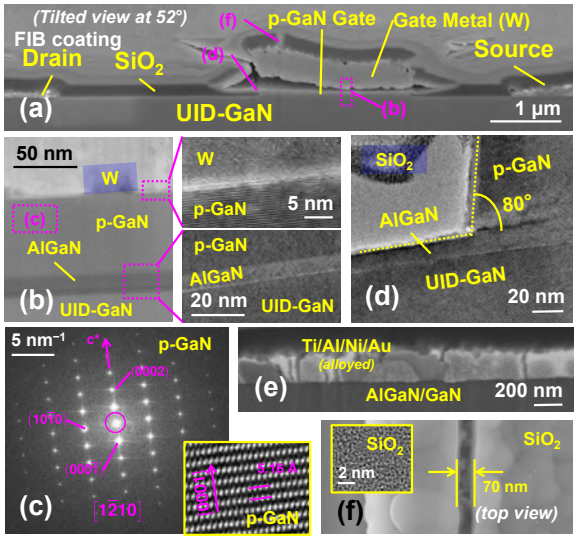

Fig. 3. Advanced microscopy investigation of the device after test. (a) FIB cross-sectional image of the DUT after the testing. (b) Zoom-in view of an intact region of the W/p-GaN/AlGaN/GaN structure (HAADF-STEM). The interfaces are shown in the insets (TEM). (c) Crystallinity (reciprocal lattice) of p-GaN (FFT of TEM). The inset shows the corresponding HRTEM image. (d) Sidewall of the p-GaN-gate region (TEM). (e) Drain contact located on the AlGaN/GaN surface (SEM). The original p-GaN on top of AlGaN was etched to expose the AlGaN surface for formation of ohmic contacts. (f) Small crack in the SiO_2 layer (top view, SEM). The inset shows the amorphous SiO_2 (TEM). All images are cross-sections unless otherwise stated. (FIB: focused ion beam; SEM: scanning electron microscope; TEM: transmission electron microscope; HAADF-STEM: high-angle annular dark-field scanning TEM; FFT: fast Fourier transform; HRTEM: high resolution TEM; UID: unintentionally doped.)

duration of the test [Fig. 2(d)(i)–(ii)]. $I_{D,max}$ of the packaged DUT (30 mA/mm) was lower than that of the bare die DUT (50 mA/mm), likely due to the degradation of the packaging (e.g. bond pad) [19].

The transistor metrics over time during the harsh environment stress are presented in Fig. 2(d)(iii)–(vii). A stable V_{TH} of $0.9 \sim 1$ V (E-mode) was maintained. Assuming $V_{DD} = 5$ V operation and no V_{SS} [22], the peak-to-peak variation (< 0.09 V) corresponds to 1.8 % of the rail-to-rail voltage. The current decreased by < 5.3 mA/mm (18 %), and R_{ON} increased by 9 Ω·mm (12 %), likely caused by degradation of the intrinsic transistor (e.g. ohmic contacts, two-dimensional electron gas channel) and bond pad in the test environment. A stable gate leakage (< 0.1 mA/mm variation, 12 %) and current ON-OFF ratio (< 5 % variation in terms of order of magnitude, limited by gate leakage) was maintained.

At the end of the test, the DUT was characterized using advanced microscopy. The device structure was found to be largely intact [Fig. 3(a)]. The p-GaN-gate region deserves special attention because it enables E-mode operation of the DUT, but the effect of harsh environment conditions. A p-GaN/AlGaN/GaN heterostructure was maintained, as reflected in the smooth interface between the epitaxial layers [Fig. 3(b)], and the crystallinity in p-GaN [Fig. 3(c)]. No noticeable degradation was found in the etched sidewall and AlGaN surface (etch stop layer) [Fig. 3(d)]. Similarly, the Ti/Al/Ni/Au contacts remained structurally intact [Fig. 3(d)–(e)], though it has been noted in other works that prolonged HT exposure might lead to degradation [27]. A small crack (width 70 nm) was found in the SiO_2 layer [Fig. 3(f)], likely resulting from a mismatch in the thermal expansion coefficient between W (gate metal) and the surrounding SiO_2. As compared to [19], W remained intact despite the presence of corrosive gases (e.g. SO_2), which could be attributed to the passivation. The structure is generally intact, despite some incipient cracks.

TABLE I
ROBUSTNESS STUDIES OF GAN HEMTS IN HARSH ENVIRONMENT.

E/D-mode	Epitaxial Structure	Reference	Temp. (°C)	Ambient	Duration (h)	$\Delta I_{D,max}$ (%) [2]	ΔV_{th} (V) [2]
D	AlGaN /GaN	[7]	250	5% H_2/95% N_2	24	3	0.2
		[28]	400	Air	25	72	1.4
		[29]	175	N.A.	500	5	0.1
		[30]	525	N.A.	25	10	0.6
	InAlN /GaN	[31]	900	Vacuum	50	100	N.A.
		[6]	1000	Vacuum	25	55	0.3
		[2]	465	Venus	240	30	0.04
E	p-GaN /AlGaN /GaN	[32]	125	N.A.	5000	N.A.	0.15
		[33]	85	High humidity	1000	N.A.	1
		[19]	500	N_2	24	35	0.05
		This Work	**460**	**Venus (complete chemical env.)**	**240**	**18**	**0.09**

[1] Duration of *in-situ* measurement at the specified HT. [2] Peak-to-peak data across the duration of test at the specified temperature. Values, if not explicitly reported, are based on best estimates from the published data.

The robustness of the proposed transistor [Fig. 2(d)] was benchmarked against similar studies of GaN HEMTs in Table I [2], [6], [7], [19], [28]–[33]. To the best of the authors' knowledge, this is the first study of an E-mode GaN transistor working above 300 °C, in high pressure and under a highly harsh environment (simulated Venus atmosphere). The reported transistor features competitive robustness, as reflected in the relatively small degradation in both $I_{D,max}$ and V_{TH}.

V. CONCLUSION

An E-mode GaN transistor technology was proposed and characterized up to 500 °C. Its robustness in harsh environment was evaluated through both *in-situ* electrical characterization, and comprehensive microscopy of the epitaxial and device structures. This work demonstrated continued operation of the transistor after 11 days in simulated Venus condition, while slight degradations of device operation and structure were observed. The results establish the proposed GaN technology a strong contender for harsh environment mixed-signal electronics. This study also offers insights to p-GaN-gate HEMTs for harsh environment power electronics.

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Towards DTCO in High Temperature GaN-on-Si Technology: Arithmetic Logic Unit at 300 °C and CAD Framework up to 500 °C

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Abstract: This article reports advances in high temperature (HT) GaN-on-Si technology by taking pioneering steps towards design technology co-optimization (DTCO). A computer-aided design (CAD) framework was established and experimentally validated up to 500 °C, the highest temperature achieved by such a framework for GaN technology. This framework was made possible thanks to (1) demonstration of multiple key functional building blocks (e.g. arithmetic logic unit (ALU)) by the proposed technology at HT; (2) experimentally calibrated transistor compact models up to 500 °C (highest temperature modeled for an Enhancement-mode GaN transistor). Excellent agreement was achieved between experimental and simulated circuits in the static characteristics (<0.1 V difference in voltage swing) and trends of dynamic characteristics (timing) were accurately captured. By adopting complementary approaches in experiment and simulation, this work lays the foundation for the scaling-up of HT GaN-on-Si technology for mixed-signal applications of HT (>300 °C) electronics.

Keywords: GaN, arithmetic logic unit, VLSI, high temperature, compact modeling, MVSG, computer-aided design (CAD).

Introduction

High temperature (HT) electronics is critical for emerging applications in automotive (electric vehicles), renewable energy (geothermal), oil and gas exploration (deep drilling), and aerospace (hypersonic aircraft) [1]. Such harsh environments (> 250 °C) exceed the typical rating of Silicon-on-Insulator (SOI) technology. These applications call for the deployment of wide band gap (WBG) semiconductors, where GaN, alongside SiC, stands out as a promising candidate [2].

Experimental research thus far has focused on proof-of-concept HT GaN transistors and circuits, based on a variety of logic families (Enhancement/Depletion-mode n-FET, complementary n-/p-FETs etc. [3]–[5]), transistor technologies (*p*-GaN-gate, fluorine-plasma etc. [3]–[4]), and integration (monolithic or heterogeneous [6]). However, more research effort is required on: (1) improving the performance of HT circuits; (2) accessing the long-term robustness of the transistors; (3) monolithic integration on a scalable platform to accelerate commercialization; and (4) leveraging computer-aided design (CAD) framework to achieve rapid scaling-up and reduce time-to-market.

Technology Foundation and Roadmap

The HT GaN technology used in this work (Fig. 1) stands out thanks to (1) state-of-the-art propagation delay $t_p \propto L_G^2$ at 25 °C and operational at 500 °C (highest temperature of GaN ring oscillators (ROs)) [7]; (2) long-term robustness in harsh environment (Table I and [8]); (3) monolithically integrated on 150 mm GaN-on-Si platform [7]. The technology is based on E/D-mode *n*-FETs, where the E-mode driver is the *p*-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) and the D-mode load (gate-source tied) is the AlGaN/GaN HEMT. A refractory metal (tungsten) self-aligned gate process is used to achieve high uniformity and eventual scaling for HT, high-speed applications [9].

Using complementary approaches of experiment and simulation, this work advances a roadmap for the proposed technology (Fig. 2). At its core is a novel computer-aided design (CAD) framework that is then calibrated with experimental data at both the device-level (HT transistors) and circuit-level (more complex circuits, e.g. arithmetic logic unit (ALU)). The differences between the simulation and experimental circuits are used to provide feedback on future improvements to the proposed technology.

Demonstration of Arithmetic Logic Unit (ALU)

An important milestone for the development of HT electronics would be the demonstration of a microprocessor unit (MPU). Using the proposed technology, a variety of building blocks were fabricated. NAND and NOR gates were operational at 300 °C (Fig. 3(a)–(b)). The ALU, which consists of the control bit (*A*>*B*) and an output bit (XOR), exhibits correct operation at 300 °C (Fig. 3(c)–(d)). The results are achieved at V_{DD}=5 V (a low bias for WBG circuits [10]) and without a negative bias (V_{SS}) terminal (commonly needed in SiC-based circuits [10]). The ALU maintains a voltage swing of ~4.7 V (V_{DD}=5 V) at 300 °C which indicates high noise margin at HT, and will serve as a key component of the future HT one-instruction set computer (OISC) [11].

Experimentally Verified CAD Framework for HT GaN-on-Si Technology

A CAD framework of the proposed technology would serve as a first step towards the scaling up and eventual design technology co-optimization (DTCO) [12]. A unique challenge in this framework is the need for modeling and validation over a wide temperature range. To this end, a HT-enhanced version of the industry-standard MIT Virtual Source GaN Transistor Model (MVSG) [13] was adopted to achieve excellent fit up to 500 °C (Fig. 4). Table II presents 6 key MVSG parameters with up to second-order temperature dependencies. The E-mode transistor features a unique trend in V_{TH} due to its *p*-GaN-gate. A slightly increasing V_{TH} was found up to 300 °C, which could be attributed to the increasing ionization ratio of Mg (dopant) in *p*-GaN. A decrease in V_{TH} above 300 °C is due to a lower turn-on voltage of the *p*-*i*-*n* junction (in *p*-GaN-gate) and a reduced Schottky barrier (gate metal/*p*-GaN) height [14]. A two-part equation (Eq. (1)) for V_{TH} was inserted in the enhanced MVSG.

Besides the conventional "CAD simulation path" (Fig. 2), this work also pursues the "experimental circuit validation path," which takes advantage of the experimental results to benchmark the accuracy of the proposed CAD framework. Excellent agreement is obtained in the static characteristics of the inverter and ALU at HT, as shown in the <0.1 V difference in the voltage swing (Fig. 5(a)–(b)). In terms of the dynamic (transient) characteristics, excellent fit between the experimental and simulated t_p of the RO was achieved up to 500 °C (Fig. 5(c)). A constant ~10 % deviation was found, which could be improved by using future experimental data of higher-stage ROs. For the D flip-flop (DFF), the simulation underestimates the setup time (t_{su}). However, a similar temperature-dependent trend (increase of ~8 ns) in t_{su} was found from 25 ºC to 500 ºC (Fig. 5(d)). This is the first study of GaN-based DFF up to 500 ºC. A major reason for the difference in deviations (absolute values) of t_p and t_{su} is layout parasitics, given that the fabricated RO has a significantly more compact layout than that of the DFF (Fig. 5(e)–(f)). The simulation study confirms that, at HT, the increase in t_p and t_{su} is attributed to the lower $I_{D,max}$ and higher R_{ON} in the E-mode transistor.

Benchmarking and Conclusion

To the best of the authors' knowledge, the proposed technology advances the frontier of HT electronics through the following aspects, for the first time: (1) demonstration of an ALU at 300 °C; and (2) E-mode GaN transistors were systematically characterized and modeled up to 500 °C (benchmarking in Table III). These experimental advances are supported by, and have strengthened the CAD framework for HT technology (benchmarking in Table IV): (1) the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology; (2) simultaneous verification and tuning of the models of two types of transistors (E-mode and D-mode) using >6 temperature-dependent parameters in the HT-enhanced MVSG; and (3) verification of CAD framework by multi-transistor (>10) ICs.

This work lays the technology roadmap of the proposed HT GaN technology and takes concrete steps towards the realization of a HT MPU and its DTCO. As part of future research, the proposed roadmap will be extended to HT (>300 °C) analog mixed-signal and power ICs. In the broader context, this work offers insights for the scaling-up of nascent semiconductor technologies (as exemplified by the proposed technology) to deliver practical microsystems.

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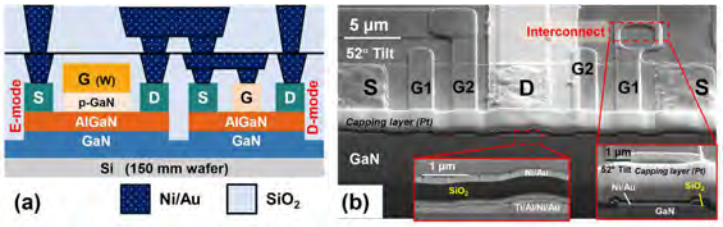

Fig. 1. (a) Proposed GaN high temperature (HT) technology based on an E/D-mode GaN-on-Si platform. (b) Tilted view shows the device structure and the cross-section (focused ion beam cut) of the fabricated circuit. Double-gate transistors are presented. The metal stack and interconnect are presented in the insets.

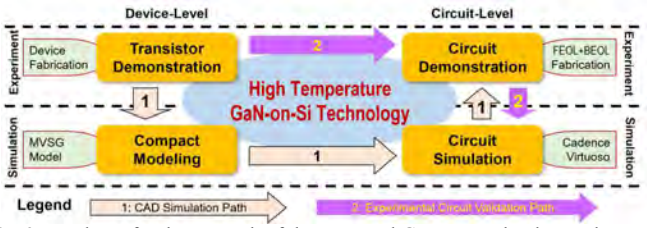

Fig. 2. Roadmap for the research of the proposed GaN HT technology. The green shapes indicate the key task or tool necessary for the accomplishment of each module. The numbered arrows indicate the two complementary pathways adopted in this work to scale up the proposed technology.

TABLE I. ROBUSTNESS OF THE PROPOSED TECHNOLOGY IN HARSH ENVIRONMENT

Specification	Change over 6 days
V_{th}	− 5 %
$I_{D,max}$	− 20 %
$\log(I_{ON}/I_{OFF})$	− 7 %
R_{ON}	+ 3 %

The E-mode transistor was tested in a simulated harsh environment (465 °C, 90 atm., corrosive gases) over 6 days. Excellent robustness was achieved, therefore serving as the technology foundation for the HT circuits of this work.

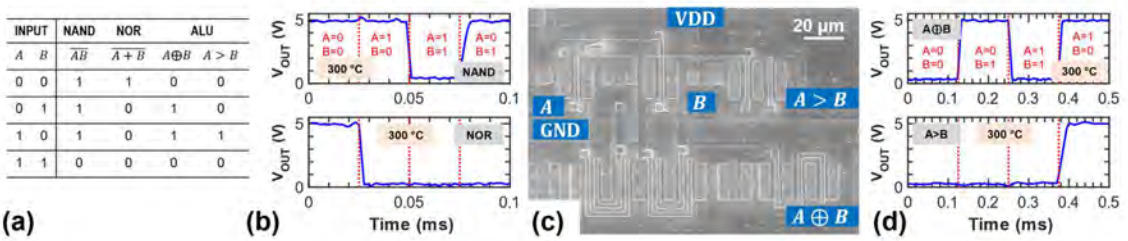

Fig. 3. Experimental demonstrations of logic gates and the arithmetic logic unit (ALU) at HT. (a) Logic table of NAND, NOR, and the ALU including their Boolean expressions. (b) Measured waveforms of NAND and NOR. (c) Micrograph of ALU after HT measurement. (d) Measured waveforms of the ALU outputs. These circuits are connected to V_{DD}=5 V and GND without the need of a negative bias (V_{SS}) terminal. The circuits are measured in a probe station with a thermal chuck whose rating is 300 °C.

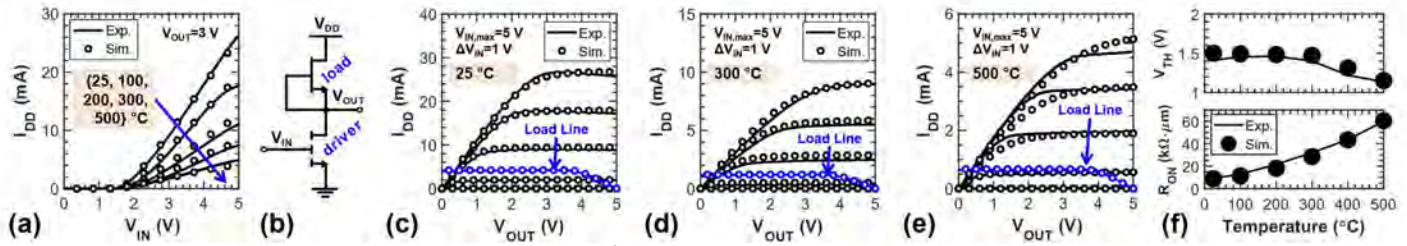

Fig. 4. Characterization and compact modeling of the transistors up to 500 °C. Industry-standard MIT Virtual Source GaN Transistor Model (MVSG) was used. (a) Transfer characteristics of the E-mode transistor (driver, W/L=36/2 μm/μm). (b) E/D-mode inverter. (c)–(e) Output characteristics of the driver with the load line (D-mode transistor, W/L=12/2 μm/μm), at {25, 300, 500} °C, respectively. (f) Summary of the key parameters of the driver transistor, V_{TH} (calculated by linear extrapolation at V_{DS}=3 V) and R_{ON} (calculated at V_{GS}=5 V, V_{DS}=0.1 V). Excellent fit was achieved using a single model for each type of transistor across a wide temperature range.

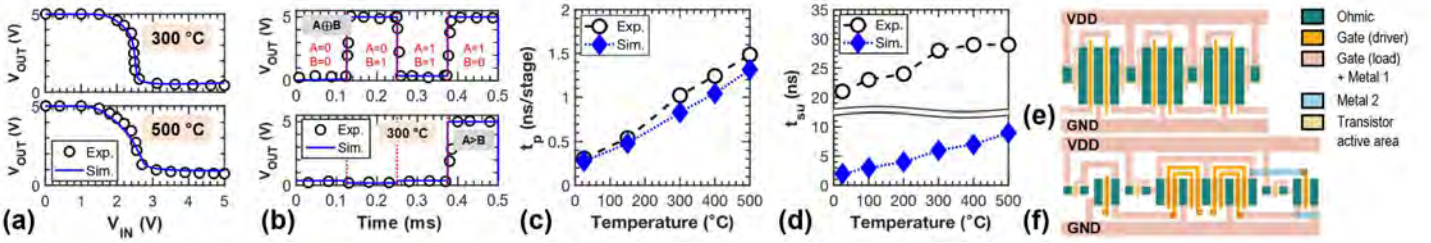

Fig. 5. Convergence of "CAD simulation path" and "experimental circuit validation path": Experimental results of the circuit proof-of-concept demonstrations are used to compare against the simulations. (a) Inverter voltage transfer curves at 300 and 500 °C. (b) Waveform of the ALU at 300 °C. (c) Ring oscillator (RO) (7-stage) propagation delay *vs.* temperature up to 500 °C. (d) D flip-flop (DFF) setup time *vs.* temperature. This is the first study of GaN-based DFF up to 500 ºC. (e)–(f) Layouts of the RO and DFF, respectively. This comparison illustrates the importance of a compact layout and the need for accurate parasitic extraction in the proposed technology. The fabricated circuits are measured up to the rating of the thermal chuck in the particular probe station (two different probe stations with ratings of 300 °C and 500 °C were used). In all circuits, V_{DD}=5 V and no V_{SS}.

TABLE II. KEY PARAMETERS OF THE MVSG MODELS

Parameter	E-mode	D-mode	Parameter	E-mode	D-mode
C_g (nF/cm²)	2.75	3.50	R_1 (10⁻³/K)	1	6
$v(T_0)$ (10⁶ cm/s)	6.5	10	R_2 (10⁻⁶/K²)	22	3.6
v_ζ (10³/K)	1	1	$SS(T_0)$ (mV/dec)	110	110
$\mu(T_0)$ (cm²/V·s)	220	550	$V_{TH}(T_0)$ (V)	1.5	−1.6
$R_{sh}(T_0)$ (Ω/□)	1050	920	$V_{TH\zeta}$ (10⁻⁴ V/K)	1	−2
$R_c(T_0)$ (kΩ·μm)	1.1	1.1	$V_{TH\zeta 2}$ (10⁻³ V/K)	−1.6	0

Eq. (1): Modified equation for $V_{TH}(T)$ of the E-mode transistor

$$V_{TH}(T) = V_{TH}(T_0) + V_{TH\zeta} \times (T - T_0) + V_{TH\zeta 2}(T) \times (T - T_1)$$

$$V_{TH\zeta 2}(T) = \{0 \text{ if } T < 300,\quad V_{TH\zeta 2} \text{ if } T > 300\},\ \{T_0, T_1\} = \{25{,}300\}\ °C \quad -(1)$$

TABLE III. BENCHMARKING OF HT E-MODE GAN HEMTS

Feature \ Publication	[3] (2007)	[16] (2022)	[14] (2015)	[17] (2020)	This Work (2023)
Transistor type	F-plasma	MIS	*p*-GaN gate	*p*-GaN gate	***p*-GaN gate**
Highest temp. (°C)	375	250	420	175	**500**
Compact modeling	–	–	–	✓	**✓**

This work features the highest temperature at which an E-mode GaN transistor is systematically characterized and then modeled.

TABLE IV. BENCHMARKING OF RECENTLY PUBLISHED HT GAN CIRCUIT SIMULATIONS

Feature \ Publication	[18] (2021)	[19] (2021)	[20] (2022)	[15] (2022)	This Work (2023)
Wafer	GaN-on-Sapphire	GaN-on-Si	GaN-on-SiC	GaN-on-SiC	**GaN-on-Si**
Technology	D-mode (HEMT)	Complementary (p-GaN-gate HEMT + *p*-FET)	D-mode (HEMT)	D-mode (HEMT)	**E/D-mode (*p*-GaN-gate HEMT + HEMT)**
Integration	3D Bonding	Monolithic	Monolithic	PCB	**Monolithic**
Highest temperature (°C)	300	300	160, 400, 550	220	**500**
V_{DD} (V)	0	5	14	20	**5**
V_{SS} (V)	−12	No V_{SS}	−14	N.A.	**No V_{SS}**
Circuit experiment	Oscillator at 1 GHz	–	NAND/NOR, DFF, Voltage ref.	Transmitter at 2 GHz	**ALU**
Circuit simulation	(same as above)	RO, SRAM	Passive components	(same as above)	**ALU, RO, DFF**
Circuit sim. verified by exp.	✓	–	–	✓	**✓**

Highlights of the proposed CAD framework include: (1) the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology; (2) simultaneous verification and tuning of the models of two types of transistors (E-mode and D-mode); (3) verification of CAD framework by multi-transistor (>10) ICs.

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High Temperature Modeling of Commercial GaN HEMTs Using an Enhanced MVSG Framework

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***Abstract*— GaN transistor technology is a promising candidate for electronics at extreme temperatures. Here we characterize the DC performance of a commercial discrete GaN HEMT device from 25°C-300°C. Furthermore, we enhance the MIT Virtual Source GaN FET (MVSG) model to account for temperature dependent leakage current, subthreshold swing, and contact resistance. This model was used to estimate the large signal performance at elevated temperatures, as the commercially available model was not designed to run at such elevated temperatures.**

Keywords—GaN; high temperature; MVSG; modeling; RF

I. Introduction

High temperature electronics is a critical component to develop a wide variety of new system platforms that will allow the exploration of energy-rich geothermal wells, flight of hypersonic aircrafts, and space exploration of the surface of Venus. Traditional Si-based electronics are typically limited to temperatures below 250°C and are unsuited for such extreme environments. However, wide-bandgap semiconductors, and especially Gallium Nitride (GaN), allow for a significantly lower intrinsic carrier concentration, which in turn makes it possible to operate at much higher temperatures. Single device performance of GaN based systems has been demonstrated up to 1000°C [1]. Furthermore, recent work has demonstrated robust GaN E/D-mode and E/E-mode memory cells and ring oscillators (E: enhancement, D: depletion) operating at 300°C and 500°C respectively [2],[3],[4].

GaN has already developed significant commercial penetration in the fields of room temperature power and RF electronics. However, efforts in high temperature RF remain relatively unexplored. Here we characterize the high temperature current-voltage (I-V) characteristics of a commercial GaN-on-SiC high electron mobility transistor (HEMT) and compare the results with the corresponding commercial models available for the characterized device. Due to the limitations of the commercial model, a new high-temperature version of the physics-based and industry-standard MVSG model [5] is proposed and used to provide accurate high-temperature modeling of the devices, and estimations of expected RF performance.

This work was partially sponsored by Lockheed Martin Corp. under grant no. 025570-00036 (Dr. John Callahan), and the Air Force Office of Scientific Research (AFOSR) under grant no. FA9550-22-1-0367 (Dr. Kenneth Goretta).

II. Characterization and Simulation Methodology

For this study, a commercial 1.25 mm DC-18 GHz discrete power GaN-on-SiC HEMT was used. The bare die device was characterized using a probe station with a heated thermal chuck starting from 25°C to 300°C in ambient air. The discrete device was bonded to a carrier with a high performance ceramic Al_2O_3 paste with temperature rating over 1500°C and wire-bonded to external pads for ease of measurement. I-V measurements were then carried out at 25°C, 150°C, and 300°C with a 15-minute wait period at each temperature in order to ensure the device and chuck were in thermal equilibrium.

The simulation compact models were taken from vendors associated with the commercial device and run in Keysight's Advanced Design System (ADS) simulator. Similarly, the MVSG developed models were also run in ADS.

III. Experimental Results and Simulations

Figure shows the results of running room temperature power sweep simulations with optimal power matching using the commercially provided model for the characterized discrete GaN device. The device was biased at V_{ds}=12 V and $I_{d,q}$ = 25 mA, and the loadpull simulations were done at 3 GHz. As seen in **Table 1**, when compared to the device datasheet, the simulation output shows good agreement with experimental device metrics, although it should be noted that the loadpull simulation in this work was performed under continuous-wave (CW) conditions, while the datasheet conditions were done under pulse-wave conditions.

Figure 2 shows the simulated DC current voltage (I-V) characteristics of the same device with the ambient temperature swept from 25°C up to 300°C using the commercially available model. Although, the room temperature device simulations match well with the experimental device datasheet, the model begins to lose fidelity as the ambient temperature setpoint is adjusted. According to this model, the transfer characteristics, in particular the off-state leakage, are virtually unchanged with

increasing temperature. This is partly due to the fact the model range is limited to below 125°C and gives a fixed performance

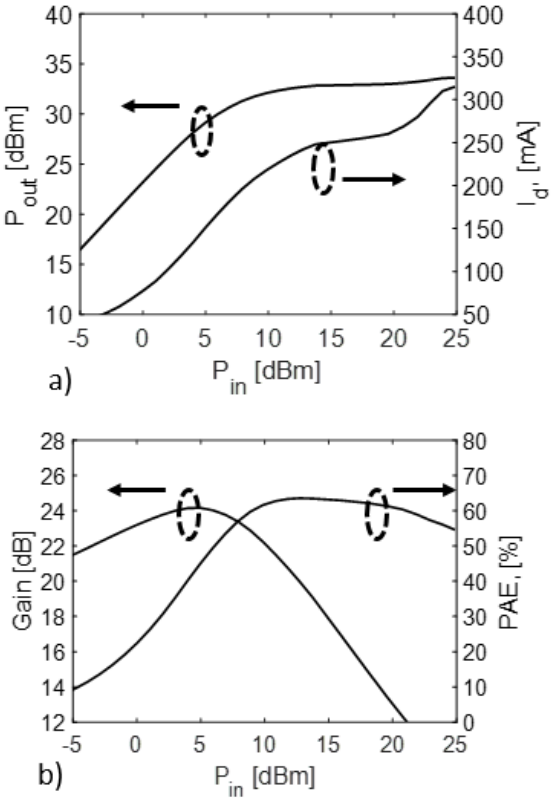

Figure 1. Simulation of the (a) output power, output current, (b) gain, and PAE of the GaN discrete device using its commercially provided model at room temperature with optimal output power impedance matching.

	Data sheet	Commercial model
Temp. (°C)	25	25
f (GHz)	3	3
$V_{DS,Q}$ (V)	12	12
$I_{D,Q}$ (mA)	25	25
Tuning	Power	Power
Waveform	Pulsed (10% Duty, 100 µs width)	CW
P_{sat} [dBm]	33.8	33.6
Peak PAE [%]	65	63
Small-signal Gain [dB]	22	21.6

Table 1 *Comparison of the loadpull power sweep of the commercially provided model at room temperature with*

outside this range. However, even from 25°C to 100°C, when compared to the experimental data the model significantly underestimates the increase in leakage current and decrease in on current. The off-state leakage current (taken at Vgs = -4V) as

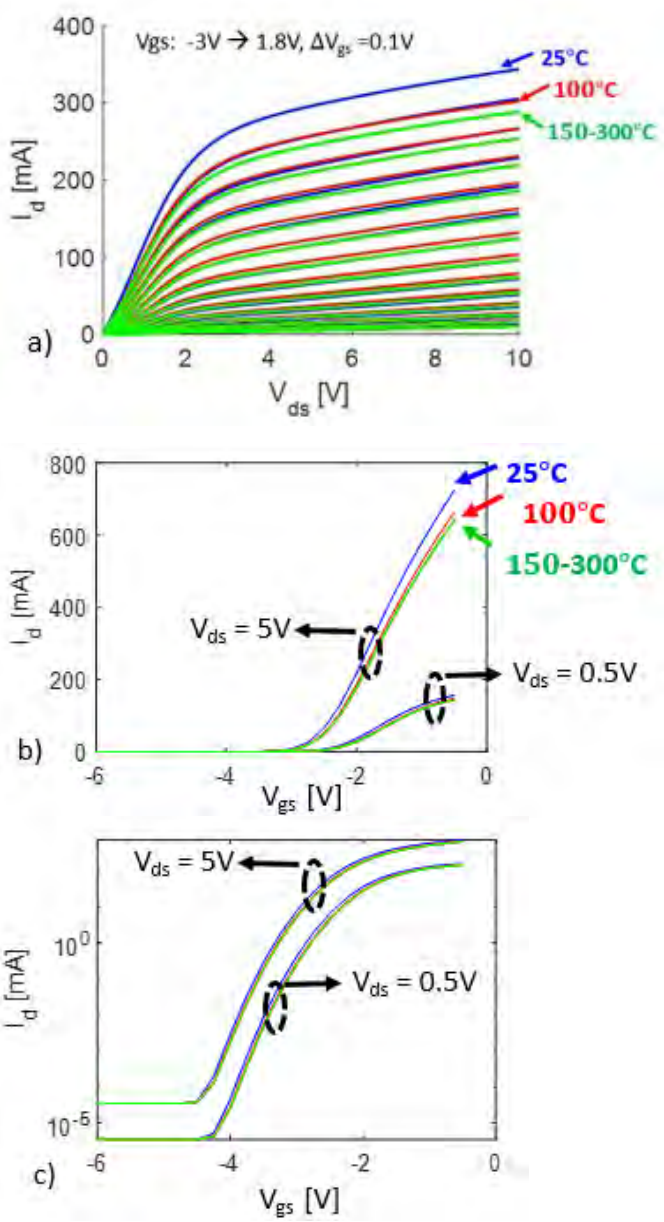

Figure 2*. Simulation of the (a) output, (b) linear-scale transfer I-V (c) log-scale transfer I-V curves of the GaN discrete device using its commercially provided model at 25°C (blue), 100°C (red), and 150-300°C (green). The commercial model is limited to below 125°C and thus 150-300°C give a fixed performance.*

a function of temperature from 25 ° C to 300 ° C of a corresponding experimental device for which the model was built is shown as an Arrhenius plot in **Figure 3**. While as seen in **Figure 2c** the commercial model keeps this off-state leakage current nearly constant as a function of temperature, in the actual device it increases by nearly three orders of magnitude, and follows an exponential temperature dependence with an equivalent energy barrier of 0.31eV for V_{ds} = 0.5V. This leakage

is likely to be Poole-Frenkel emission via trap and/or surface states which is strongly dependent on temperature, and regularly seen in AlGaN/GaN HEMT devices [6], [7]. Due to the limitations of the commercially available model, a modified MIT Virtual Source GaN FET (MVSG) physics based compact model [5] was developed and fit to the measured discrete device.

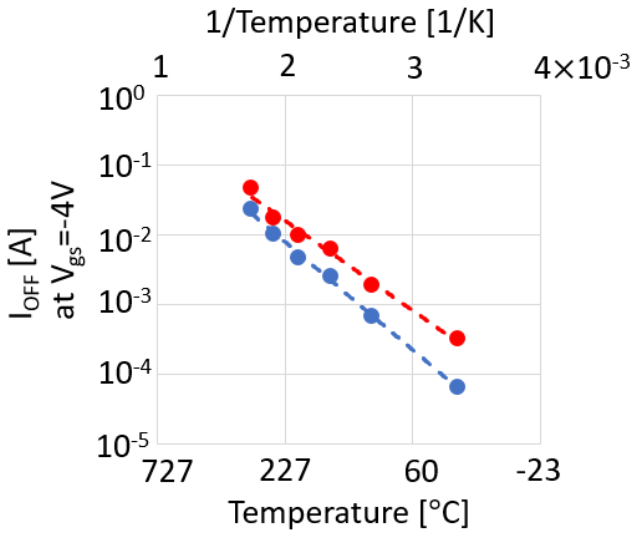

***Figure 3**. Arrhenius plot of the experimentally measured off-state drain current (measured at V_{gs} = -4V) on the commercial discrete GaN device*

The main modifications included an experimentally calibrated temperature-dependent leakage current model based off the exponential Poole–Frenkel emission via trap/surface states exhibited in **Figure 3** as well as a fitted on-resistance temperature dependence and threshold voltage shift. **Figure 4** compares the experimental data with the simulation results of I_d and I_g using the MVSG based compact model and the original commercial model. The temperature device trends are captured much more accurately, including the on-current degradation as well as the off-current increase. Together, these lead to a more accurate simulation of the experimental device data as a function of temperature from 25°C to 300°C.

With simulations from a compact model that more closely capture the trends in the experimental device data at elevated temperatures, we can then perform large-signal load-pull simulations in ADS to understand the estimated RF performance at 150°C, 300°C, and 500°C at 3 GHz with Vds=12 V and $I_{d,q}$=25mA **(Figure 5).**

A steady decrease in the saturated output power is observed which is consistent with the corresponding decrease in the maximum drain current with increasing temperature. The decrease in output power in turn leads to a declining PAE with increasing temperature. On the other hand, while the small signal gain is considerably affected, the gain at the peak PAE and afterwards is already in hard compression and not considerably affected by the ambient temperature, at least until 500°C, from which point there is a noticeable drop in the large signal gain at peak PAE. However, at 3 GHz, the gain is still greater than 15dB and thus is not a large contribution to the decrease in PAE.

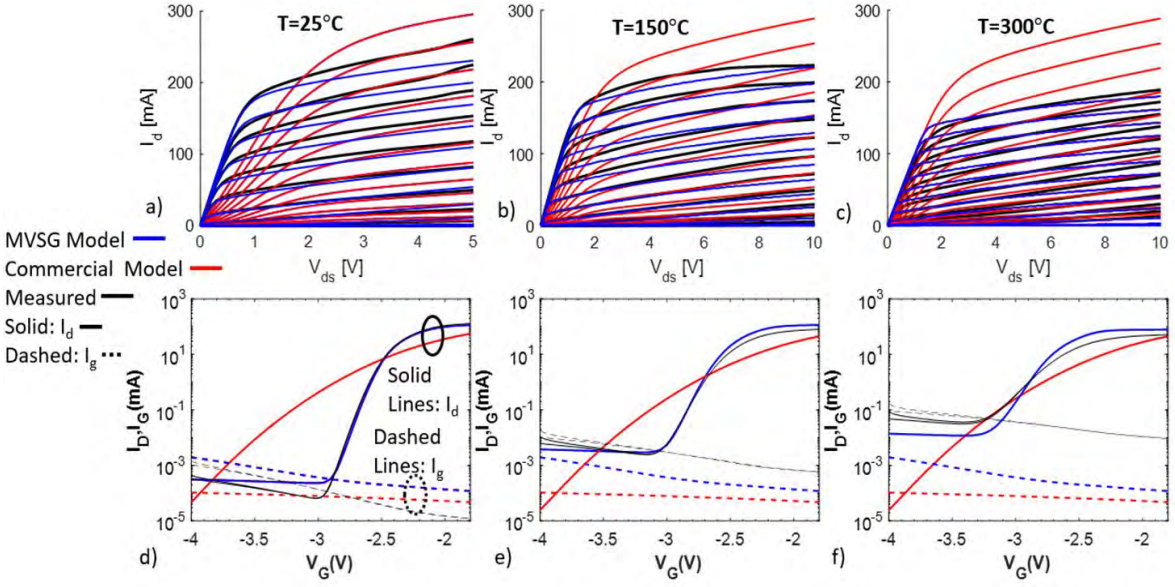

***Figure 4** Comparison of experimental device (black lines) with MVSG simulations (blue) across different temperatures for the drain current (solid lines) and gate current (dashed lines). a)-c) show output curves and d)-f) show the corresponding transfer curves at 25, 150, and 300°C respectively*

IV. Conclusion

We have shown that commercial GaN HEMTs are already capable of experimentally operating at temperatures of 300°C, which is already far beyond the typical maximum operating temperatures of traditional silicon devices. However, the current compact models are not adequate for high temperature operation. Here we have characterized the high temperature I-V characteristics of a commercial GaN HEMT and enhanced the MVSG model to more accurately capture the prevalent temperature dependencies. Furthermore, load pull simulations based on the temperature-calibrated compact models predict good performance of GaN RF HEMTs even beyond 300°C, although the performance and stability are expected to improve even further through the use of new transistor designs and fabrication technologies optimized for high temperature operation.

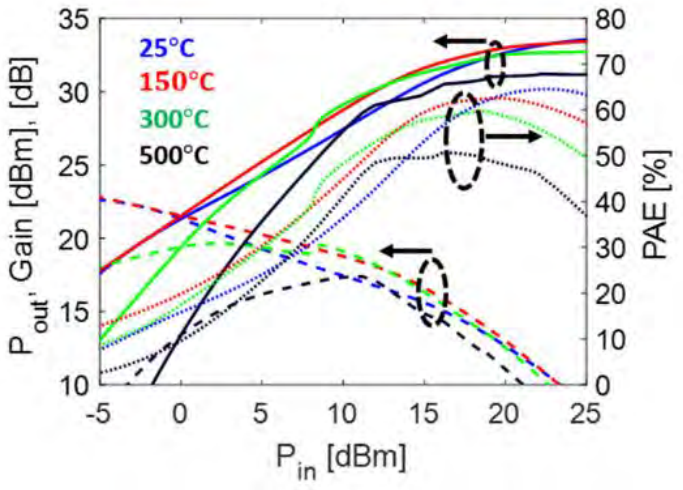

Figure 5. *Large signal loadpull simulations for optimal power match at 3 GHz with V_{ds}=12 V using the MVSG calibrated from Figure 4.*

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GaN Memory Operational at 300 °C

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***Abstract*— The most commonly used memory cells, namely a 32-bit × 10-bit read-only memory, a 1-bit 4-transistor static random-access memory, D latch, and D flip-flop (DFF), were demonstrated using high temperature (HT) GaN technology on a monolithically integrated GaN-on-Si platform and n-FET-only E/D-mode logic (E: enhancement, D: depletion). The memory cells exhibit stable operation at 300 °C. A maximum clock frequency of 36 MHz at 300 °C was estimated for the DFF using the measured setup time. To the best of the authors' knowledge, the operational temperature of the reported prototypes represents the highest value for GaN memory, paving the way for the realization of robust mixed-signal systems operating at HT.**

***Index Terms*— GaN, transistor, high temperature, E/D-mode, memory, SRAM, ROM, D latch, D flip-flop.**

I. Introduction

THE rapid growth of high temperature (HT, ≥ 300 °C) electronic applications in the fields of aerospace, automotive, oil and gas exploration and more, requires fundamental advancements in semiconductor technology [1]. Considering their wide band gap, high chemical stability, very low intrinsic carrier concentration and excellent transport properties, gallium nitride (GaN) and other III-N materials stand out, alongside silicon carbide, as leading candidates. High performance (room temperature) transistors for RF, power, and increasingly, mixed-signal applications have been demonstrated [2], [3], [4], [5], [6]. Moreover, early studies on the HT characterization of III-N transistors [7], [8], [9], [10], [11] and MEMS sensors [12], [13] have been reported.

The focus of HT GaN electronics has thus far been basic *combinational logic* building blocks [14], [15], [16], [17]. While these studies offer strong indication of the potential of GaN transistor technology for HT applications, the development of HT GaN ICs is still at its infancy due to the low level of complexity and integration demonstrated so far. Significant research is required for the next big leap of HT GaN mixed-signal ICs. Memory, which is the storage of state information, is a fundamental requirement of any complex digital system, and is realized using *sequential logic* circuits. There are very few reports of GaN sequential logic circuits [18], [19], [20], and only one experiment which demonstrates operation of such circuits at 160 °C [21] with little indication of their suitability for higher temperature (≥ 300 °C) operation.

Sequential logic requires a high level of uniformity and high operating frequency. Among the various GaN logic implementations and E-mode GaN transistor designs, the n-FET-only E/D-mode (E: enhancement, D: depletion) based on the p-GaN/AlGaN/GaN platform is preferentially considered for HT technology, thanks to its absence of gate dielectrics and its process simplicity. Unfortunately, previous experiments on GaN HT circuits [22] were based on relatively immature HT technologies with a low level of complexity.

This work demonstrates progress towards the integration of GaN HT electronics through an optimized process flow, in order to study the different trade-offs involved in HT memory cells. The proposed memory cells, namely (1) read-only memory (ROM), (2) static random-access memory (SRAM), (3) D latch, and (4) D flip-flop (DFF), show stable operation at 300 °C. The key performance metrics of the fabricated DFF, the most challenging implementation among all, were evaluated across temperature.

II. High Temperature GaN Platform

The GaN platform used in this work is based on epitaxial p-GaN/AlGaN/GaN on 150 mm Si wafer (Fig. 1(a)) which offers the scalable monolithic integration of E- and D-mode transistors [22]. The E-mode p-GaN-gate high electron mobility transistors (HEMTs) are fabricated with a self-aligned gate-first technology and tungsten gate (Schottky to p-GaN [23]). The back-end-of-line (BEOL) started with the deposition of Ni (30 nm)/Au (80 nm) to act as both D-mode Schottky gate and the first layer of interconnect. A SiO_2 interlayer dielectric was formed and opened through a via mask over the transistor electrodes. Ti (20 nm)/Au (200 nm) was deposited to serve as the contact pads and the second layer of interconnect.

In the E/D-mode logic implementation, the E-mode transistor serves as the driver and is therefore critical to the performance of the circuits. The E-mode transistor technology of this work was optimized for HT applications through features including, (1) a refractory metal (W) gate, and (2) self-alignment of p-GaN and metal through the gate-first process, which ensures a high metal/p-GaN interface quality and

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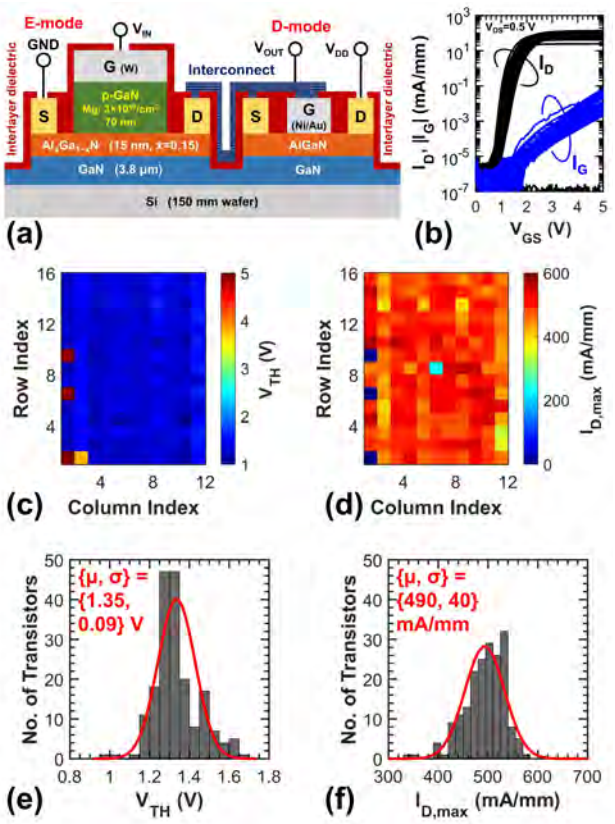

Fig. 1. Optimized GaN HT transistor technology used in this work. (a) Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter. (b) Transfer characteristics with $V_{DS} = 0.5$ V, (c) distribution and (e) histogram of V_{TH}, and (d) distribution and (f) histogram of $I_{D,max}$ of a total of 192 E-mode transistors across a 1.2 cm × 1.2 cm sample with excellent average ON/OFF ratio $> 3 \times 10^7$. V_{TH} is measured at $V_{DS} = 0.5$ V. $I_{D,max}$ is measured at $V_{GS} = 5$ V. Measurements were conducted at 25 °C.

reduces gate leakage which would become significant problems at HT [24]. Early studies indicate HT (500 °C) robustness of the transistors through long-term survival tests [25]. The sheet resistances of the AlGaN/GaN channel, 1st-, and 2nd-interconnects are 460 Ω/□, 0.59 Ω/□, and 0.21 Ω/□, respectively. The E- and D-mode transistors share the same $L_G = L_{GS} = L_{GD} = 2$ μm.

In order to achieve high uniformity, a BCl_3/SF_6-based etch stop process was optimized for the selective removal of p-GaN over AlGaN. Good uniformity was observed at 25 °C across 192 E-mode transistors ($W_G = 6$ μm) on a 1.2 cm × 1.2 cm sample with $V_{TH} = 1.35 \pm 0.09$ V, $I_{D,max} = 490 \pm 40$ mA/mm (Fig. 1(b)–(f)). As a reference, V_{TH} of D-mode transistors is −1 V.

While the results indicate the maturity of the proposed platform for higher integration in HT circuits, there are some outliers ($> 3\sigma$) in the transistor characteristics (5% for V_{th} and 3% for $I_{D,max}$) at room temperature. The circuits which incorporate transistors with significant outlying characteristics would likely not work as expected. The corresponding distributions were unable to be measured at HT due to the limitation of the measurement equipment. To mitigate the non-uniformity, in particular outlying characteristics, redundancy may be introduced to the circuit design, though this is beyond the scope of a proof-of-concept demonstration which is the

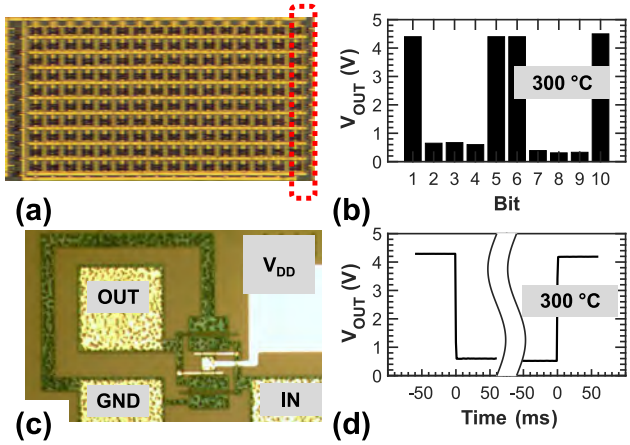

Fig. 2. GaN ROM and 4T-SRAM. (a) Micrograph of a 32-bit × 10-bit NOR-based ROM array. (b) The measured output of the 1st instruction stored in the ROM. (c) Micrograph of a 4T-SRAM. (d) Waveform of the SRAM operating at 300 °C with input transition from logic state '1' to '0' (left) and '0' to '1' (right).

focus of this work. Instead, the circuits in this work were designed with large tolerances to account for the majority of the measured distribution in transistor characteristics, therefore ensuring functionality.

III. Memory Characteristics

Several memory cells were implemented based on the GaN-on-Si platform reported in Section II. Monolithically integrated n-FET-only E/D-mode logic was used with $(W_G/L_G)_{\{E,D\}} = \{36/2, 12/2\}$ μm/μm. These devices yielded a drive/load ratio $\beta = (W/L)_E/(W/L)_D = 3$. V_{DD} was chosen to be 5 V to achieve a balance among speed, noise margin and power consumption. Future studies on the impact of V_{DD} scaling would allow for temperature-adaptive voltage techniques for operation over a wide temperature range [26]. The measurements were conducted in a probe station where the chip was placed on a thermal chuck up to 300 °C (rating of the chuck) in atmosphere. Each measurement was conducted 30 min. after the chuck reached the temperature set point.

As shown in Fig. 2(a), a 32 bit × 10 bit NOR-based ROM array was constructed with the 1st 10-bit instruction being enabled. The measured output matched the expected instruction with $BL[0:9] = [1000110001]$ at 300 °C (Fig. 2(b)). The maximum voltage of the output is limited to 4.5 V due to the voltage drop induced by the static current (IR drop) through the interconnect, which could be improved with an optimized interconnect metal stack. The minimum voltage is above 0 V due to the nature of n-FET-only logic. It should be noted that, due to the nature of the NOR-based implementation of ROM, the measurement of each word line is independent of the other lines. Therefore, the measurement of one line proves the feasibility of this implementation.

A four-transistor SRAM (4T-SRAM) was constructed from a pair of cross-coupled E/D-mode inverters as shown in Fig. 2(c). The input is first connected to ground ($V_{IN} = 0$ V) at $t = -50$ ms, driving V_{OUT} to logic state '1' (≈ 4.2 V) as shown in Fig. 2(d). At $t = 0$, $V_{in} = 5$ V is applied to the input to write a logic state '0' (≈ 0.5 V) into V_{OUT}. The above results demonstrate that the proposed 4T-SRAM cell functions as a stable memory cell at 300 °C.

TABLE I
A SUMMARY OF THE PUBLISHED GaN- AND SiC-BASED FFs

Ref.	Semiconductor	Driver (Transistor)	Logic Family	L_G (μm)	V_{DD}/V_{SS} (V/V)	Temp. (°C)	f_{CLK} (MHz)*
[27]	SiC	MESFET	D-mode, RTL	2	$+5/-12$	300	–
[28]	SiC	JFET	D-mode, RTL	6	$+25/-25$	500	–
[29]	SiC	MOSFET	E/D-mode, DCFL	–	$+20$/GND	300	–
[18]	GaN	F implanted HEMT	E/D-mode, DCFL	0.8	$+2$/GND	25	–
[19]	GaN	–	E/D-mode, DCFL	1.2	$+12$/GND	25	10
[21]	GaN	Conventional HEMT	D-mode, RTL	0.5	$+14/-14$	25 160	2.5 1.6
This Work	GaN	p-GaN-gate	E/D-mode, DCFL	2	$+5$/GND	25 300	55 36

DCFL: direct coupled FET logic; RTL: resistor-transistor logic. * Estimated lower bound value.

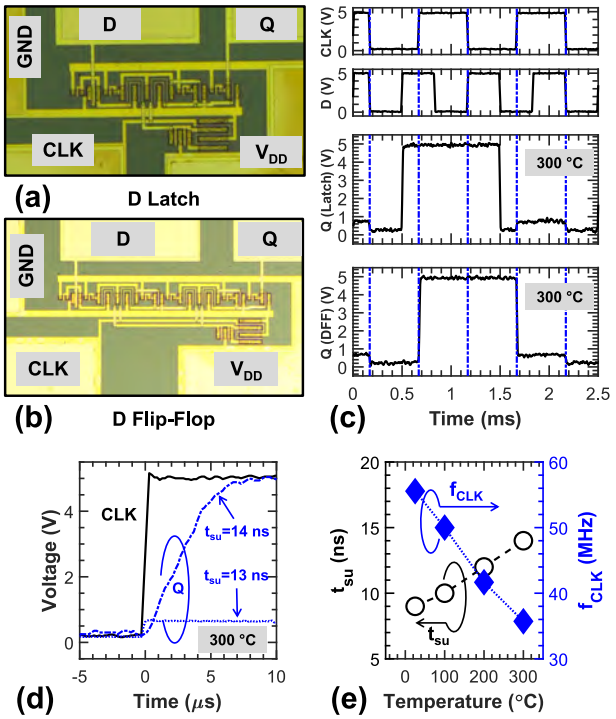

Fig. 3. GaN negative D latch and positive DFF. (a) Micrograph of a negative multiplexer-based latch. (b) Micrograph of a positive DFF using a *primary-secondary* configuration. (c) Waveforms of *CLK* at 1 kHz, *D* at 1.5 kHz, and outputs (*Q*) of both the D latch and the DFF. (d) Determination of t_{su}, using the output waveform of DFF at 300 °C as an example. (e) Trend of t_{su} and the estimated f_{CLK} *vs.* temperature.

A multiplexer-based negative D latch was constructed with input and output buffers using 13 transistors (Fig. 3(a)). As shown in Fig. 3(c), the latch becomes transparent while CLK is LOW, and holds its value while CLK is HIGH with $f_{CLK} = 1$ kHz and $f_{DATA} = 1.5$ kHz.

Lastly, a positive DFF was constructed using a *primary-secondary* (*master-slave*) configuration with a total of 20 transistors. For the fabricated positive flip-flop, the value of output (Q) is the value of input (D) sampled at the rising edge of CLK as shown in Fig. 3(c). A large voltage swing over 4 V could still be achieved for both the D latch and the DFF at 300 °C due to the matched temperature behavior of the ON-resistance for both the E- and D-mode transistors.

To evaluate the performance of the DFF across temperature, the setup time (t_{su}), an important metric to estimate maximum clock frequency ($f_{CLK} \approx 1/(t_{cq} + t_{su})$), was characterized up to 300 °C. t_{su} is the time that the data input (D) must be valid before the rising edge of CLK. Fig. 3(d) illustrates the determination of t_{su} at 300 °C, where D must be valid for a minimum of 14 ns before the rising edge of CLK ($t = 0$) to allow Q to reach state '1'. The measurement of CLK to Q time (t_{cq}) is limited due to the large load capacitance (350 pF) introduced by the measurement setup [14]. Therefore, $f_{CLK} = 1/(2 \times t_{su})$ is used to estimate the maximum clock frequency, because the estimated value of t_{cq} should be similar to the value of t_{su} based on the schematic of the fabricated DFF.

As presented in Fig. 3(e), when the operating temperature increased from 25 °C to 300 °C, the t_{su} increased from 9 ns to 14 ns, leading to a decrease of f_{CLK} from 55 MHz to 36 MHz. The decrease in performance is mainly due to the decreased ON-current of both E- and D-mode transistors resulting from the reduction of channel mobility at higher temperatures. Due to the distributions in V_{TH} and $I_{D,max}$ in the process reported in Section II, performance metrics such as t_{su} would be affected. Nevertheless, the circuits detailed here are representative circuits on the sample as a whole.

A summary of the GaN- and SiC-based FFs reported in the literature is presented in Table I. The reported DFF prototype based on the proposed GaN HT-robust technology features a simple voltage bias approach and competitive performance at room temperature. Furthermore, to the best of the authors' knowledge, the operational temperature of the reported DFF prototype is the highest among GaN-based FFs.

Several areas of improvement are identified to push the performance of GaN-based memory cells (including f_{CLK}) at HT: (1) aggressive transistor scaling, especially for the driver (E-mode transistor), to achieve higher current density with lower gate capacitance [30]; (2) reduced gate leakage at HT; (3) optimized layout for reduced parasitics and chip area; (4) HT-robust BEOL and advanced packaging [25], [31], [32]; (5) use of monolithically integrated GaN complementary technology based on a p-GaN/AlGaN/GaN-on-Si platform for higher power efficiency [14], [17], [30], [33].

IV. CONCLUSION

This letter reports the comprehensive demonstration of four different GaN memory cells, namely ROM, SRAM, D latch, and DFF, implemented by an optimized HT-robust GaN-on-Si technology. The memory cell prototypes were operational at 300 °C. By validating the potential of GaN memory cells, this work paves the way for the realization of robust mixed-signal circuits operating at HT.

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High Temperature Robustness of Enhancement-Mode p-GaN-Gated AlGaN/GaN HEMT Technology

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***Abstract*—This paper reports on the high temperature (HT) robustness of enhancement-mode (E-mode) p-GaN-gated AlGaN/GaN high electron mobility transistors (HEMTs), with an emphasis on the key transistor-level parameters for digital and analog mixed-signal applications. In-situ measurements from room temperature (RT) to 500 °C show that trends in V_{th}, R_{ON}, $I_{D,max}$ and $I_{G,max}$ are largely as expected based on first-order changes in the semiconductor properties. The fabricated transistors exhibited stable performance over 20 days at 500 °C. To the best of the authors' knowledge, this work is the first systematic study on the HT performance of E-mode p-GaN-gated AlGaN/GaN HEMTs, and sheds light on their use in mixed-signal and low-voltage power circuits.**

***Index Terms*—GaN, p-GaN, transistor, high temperature, long-term survival**

I. Introduction

Electronics that would operate reliably and robustly at high temperatures (HT, > 500 °C) are critical to push the frontiers of aeronautical engineering (e.g. hypersonic aircraft), resource extraction (e.g. deep well oil drilling), space exploration (e.g. Venus Rovers), and more. Electronic systems for these applications are all exposed to environments whose conditions well exceed the limits of silicon electronics, but offer a unique opportunity for wide band gap semiconductors, notably SiC and GaN. [1], [2] While early research on SiC high temperature power and high digital electronics has been conducted [3]–[6], GaN and other III-N materials offer potential for higher performance, in the domains of power [7]–[9], RF [10]–[12], MEMS [13], [14], digital circuits [15], [16] and sensors [17] over a wide temperature range. This wide range of potential applications allows GaN HT electronics to offer a promising path for the realization of a multi-functional, monolithically integrated HT electronics solution.

For HT digital circuits, the realization of enhancement-mode (E-mode) transistors is critical, otherwise it would be necessary to use a negative bias (V_{SS}) [18]. In the case of E-mode GaN transistors, the most commonly used technologies include, recessed MIS and p-GaN gate stacks [19]–[24]. The performance of current recessed MIS-gate transistors, though competitive at RT [25], would unfortunately be limited at HT by gate dielectric degradation and the activation of the dielectric/semiconductor interface traps [26]. On the other hand, the p-GaN-gated AlGaN/GaN HEMT technology is an attractive option thanks to the easy realization of E-mode and lack of gate dielectric. Furthermore, for eventual realization of HT GaN complementary technology, the p-GaN-gated HEMT structure allows for monolithic integration with the E-mode p-FET [15], [27] and other devices/components like D-mode n-FET (Fig. 1) and 2DEG resistors [28], [29].

Early experiments have demonstrated p-GaN-gated HEMT operation up to 420 °C, as well as their integration in E/D-mode HT (up to 500 °C) digital circuits such as ring oscillators and memory cells [30], [31]. While these initial demonstrations are encouraging, it is equally important to understand the long-term robustness (beyond quick measurements in a laboratory setting) at HT (> 500 °C) of the transistor, in order to further evaluate their potential for HT electronics.

II. Device Technology and Measurement Setup

E-mode HEMTs (devices under test, DUTs) were fabricated using a p-GaN/AlGaN/GaN-on-Si wafer as the starting material and the process flow reported elsewhere [31]. In particular, W was used as for the gate metallization due to its its properties as a refractory metal and its Schottky nature with p-GaN [32]. The bare die was packaged and placed in a furnace in N_2 ambient. The temperature was increased up to 500 °C (Fig. 2). In the measurement setup, special attention was paid to ensure all of the components are HT-rated.

III. Results and Discussion

As shown in Fig. 3(a), at HT (in-situ measurement), the maximum drain current (I_{Dmax}) is reduced and ON-resistance (R_{ON}) is increased. This is primarily the result of the degradation of mobility due to the increase of phonon scattering. As shown in Fig. 3(b), the drain current in OFF-state is dominated by the gate leakage current. In the gate diode reverse bias (negative V_{GS}) and weak forward bias regime (small positive

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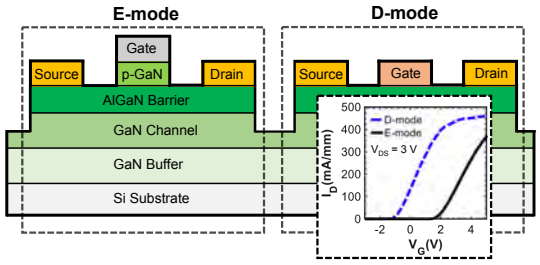

Fig. 1. Illustration of the E-mode p-GaN-gated AlGaN/GaN HEMT in this work. Its monolithic integration with a D-mode AlGaN/GaN HEMT is also illustrated. Typical transfer characteristics of both transistors are shown in the inset, with $V_{th\{E,D\}} = \{1.8, -1\}$ V.

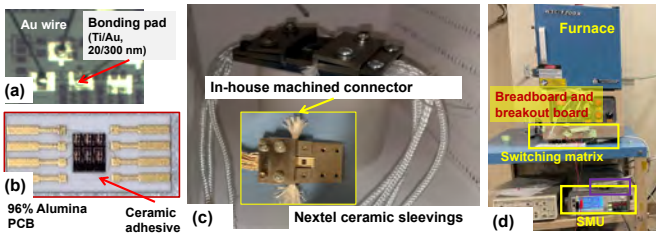

Fig. 2. Experimental setup for HT (up to 500 °C) measurement, with (a)–(d) illustrating from the DUT to the overview, in the bottom-up hierarchy order. (a) DUT. The transistor electrodes are connected to Ti/Au bonding pads. (b) Printed circuit board (PCB) made of 98% alumina. The bare die is attached using a ceramic adhesive. (c) Custom-made packaging for HT measurement, showing the in-house machined connectors and wires which are wrapped in 3M™ Nextel™ sleeving. (d) Overview of the setup. The setup shown in (c) is placed in the furnace in N_2 ambient. The switching matrix is used if more than one DUT needs to be measured.

V_{GS}) regimes, the gate leakage current increases due to two-dimensional variable range hopping (2DVRH). In the strong forward bias (highly positive V_{GS}) regime, the gate current first decreases up to 300 °C due to reduced mobility of carriers, then increases at higher temperature due to leakage through the passivation or packaging (i.e., not intrinsic DUT). A detailed study of the high temperature behavior will be reported elsewhere.

The DUTs were subjected to HT (500 °C) robustness studies. Firstly, an in-situ measurement of the DUT was conducted over 24 hours. As shown in Fig. 4, the V_{th} and I_{Dmax} remained relatively stable ($< 5\%$ variation) for over 20 hours, before some slight degradation after 24 hours.

Having established the relative stability of the DUT using

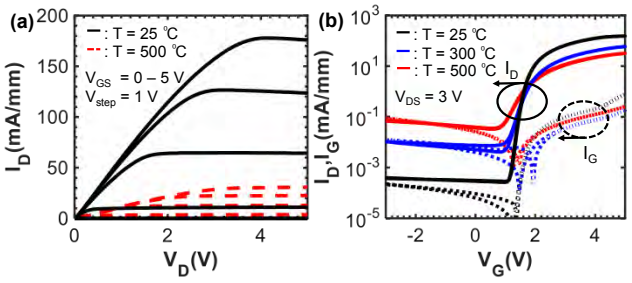

Fig. 3. (a) Output and (b) Transfer characteristics (double sweep) of the packaged DUT ($L_{SD} = 6$ µm, $L_G = 2$ µm) from RT up to 500 °C.

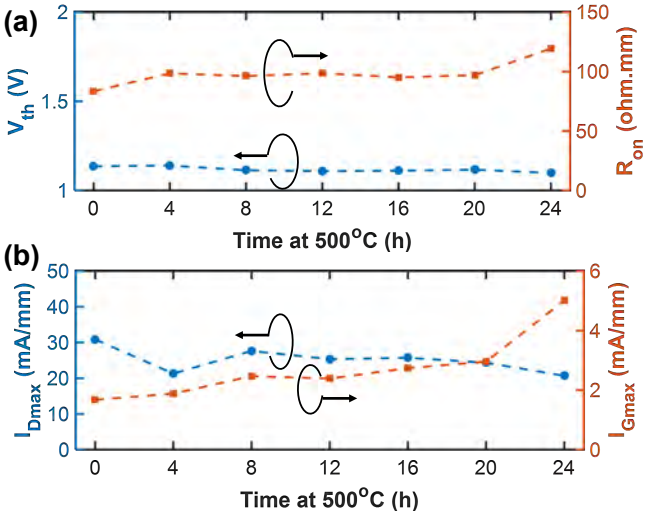

Fig. 4. In-situ measurement of packaged DUT at 500 °C in N_2 over 24 h: (a) V_{th} and R_{ON} ($V_{GS} = 5$ V), (b) I_{Dmax} ($V_{DS} = V_{GS} = 5$ V) and I_{Gmax} ($V_{DS} = 0$ V, $V_{GS} = 5$ V).

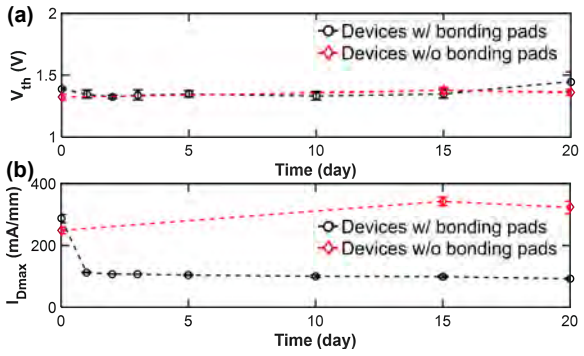

Fig. 5. Survival test of several DUTs with/without packaging (bonding pads) over 20 days in N_2 ambient. Ex-situ measurement was performed at RT: (a) V_{th}, (b) I_{Dmax} ($V_{DS} = V_{GS} = 5$ V). To the best of the authors' knowledge, this is the first report of long-term survivability of p-GaN-gated AlGaN/GaN HEMT at HT (500 °C). The results show great stability in both V_{th} and I_{Dmax}. However, the inclusion of bonding pads caused significant degradation to the measured I_{Dmax}.

in-situ measurement, a long-term survival test was conducted. For each measurement, the DUT was taken out of the furnace and cooled to RT for ex-situ characterization. It is recognized that, the packaging used in in-situ measurement might have contributed to some degradation. Therefore, in the survival test, DUTs with and without packaging were subjected to the same experiment. As presented in Fig. 5, the DUTs were found to exhibit stable DC performance over 20 days. An interesting observation is the difference between the DUTs with and without packaging, where the packaging caused a quick degradation of the measured current level on the first day.

At the end of the tests, the DUTs were inspected for structural degradation. Fig. 6(a)–(b) show that, after 1 day, minimal degradation was found to the gate structure. The DUT was no longer functional after 25 days of HT treatment. A cross-section (Fig. 6(c)) revealed that, a significant portion of the

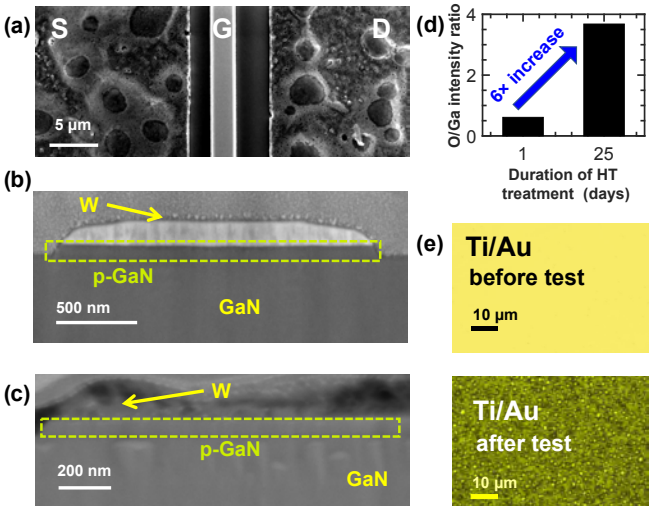

Fig. 6. Scanning electron microscopy (SEM) image of the gate region of DUT after survival test (500 °C in N_2 ambient) for 1 day, (a) top view (b) cross-sectional view. No noticeable degradation was observed in the alloyed ohmic contacts and the gate. (c) Cross-sectional view of the gate region of DUT after survival test for 25 days. A significant portion of the gate metal (W) was not present. (d) Results of the energy-dispersive X-ray spectroscopy (EDS) analysis of the 25 day HT treatment DUT (Fig. (c)). A comparison of the O/Ga intensity ratio shows an increase by a factor of 6 in the O composition relative to Ga from 1 day to 25 days of HT treatment. (e) Optical images of the Ti/Au bonding pad before and after HT survival test. The change in color indicates the change from a predominantly gold-based top layer to an inter-diffused Ti/Au alloy. The degradation of the Ti/Au bonding pad indicates the need for HT robust BEOL structures.

gate metal (W) was no longer present. In order to understand the degradation of the device from a materials perspective, energy-dispersive X-ray spectroscopy was conducted on the gate region of both DUTs. As shown in Fig. 6(d), the ratio of the intensity of the O peak to the intensity of the Ga peak increased from 0.61 (1 day HT treatment) to 3.68 (25 day HT treatment), which was an increase by a factor of 6. A likely cause for the significant introduction of oxygen is the leakage of atmospheric air into the furnace during the HT treatment. Nevertheless, no significant degradation to the epitaxial structure was found.

In terms of the back-end-of-line (BEOL) structures, significant inter-diffusion was observed in the Ti/Au layers (Fig. 6(d)), which serve as bonding pads (Fig. 2(d)). This is identified as the main cause of the current (I_{Dmax}) degradation in the packaged DUT after being exposed to HT. Metallization schemes which are less susceptible to inter-diffusion, such as Ni/Au, should be used in the future, considering that Ni is widely viewed as a diffusion barrier in Ti/Al/Ni/Au ohmic contacts [33].

A benchmarking of HT performance with published / commercially available wide band gap transistors is presented in Fig. 7. Two parameters, namely relative change in I_{Dmax} and V_{th}, are chosen due to their significance in circuit design. Fig. 7(a) indicates that, the reported p-GaN-gated AlGaN/GaN-on-Si HEMTs, exhibit similar HT current degradation as other transistors. It should be noted that, besides the epitaxial

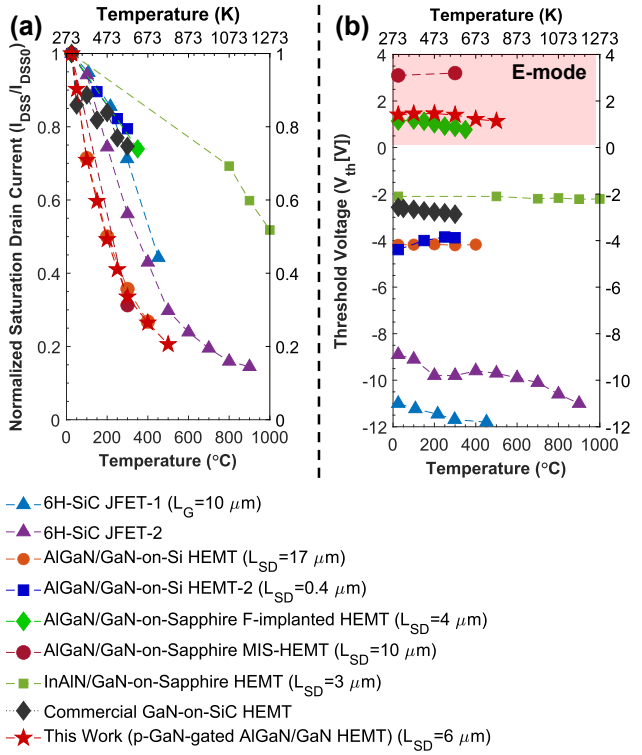

Fig. 7. Benchmarking of performance variations at HT of the reported DUT with other published and commercially available wide band gap transistors, (a) saturation drain current as a function of temperature, normalized to value at RT. The DUT shows similar current degradation trend with typical AlGaN/GaN-on-Si HEMTs. (b) V_{th}, which is relatively stable and exhibits E-mode characteristics from RT to 500 °C. All of the listed devices are bare die devices [3], [5], [10], [36], [37]. The respective channel dimensions (L_G or L_{SD}), if published, are listed.

structure and the device type (conventional HEMT / MIS-HEMT / p-GaN-gated HEMT), an important factor in device degradation with temperature is the relative contribution of the contact resistance and channel resistance towards the ON-resistance (therefore drain current), because these two components of resistance vary at different rates with temperature. The transistor studied in this work is a long-channel transistor ($L_{SD} = 6$ µm), where $R_{ON} = 15$ Ω·mm, total contact resistance is 1 Ω·mm, therefore channel resistance is 14 Ω·mm (94 %) (estimated RT values). Channel length scaling would be a straightforward approach to reducing the HT degradation, if the DUT is intended to work over a wide temperature range [34], and the further scaling of the proposed transistor technology has been demonstrated [35]. Fig. 7(b) shows that, a relatively stable V_{th} (E-mode operation) is maintained from RT to 500 °C, which would greatly aid the design of mixed-signal circuits intended to work over a wide temperature range.

IV. Conclusion

The HT robustness of the p-GaN-gated AlGaN/GaN HEMT was systematically studied at 500 °C. The DUTs show stable performance over long-term survival tests, therefore attesting to the HT robustness of the proposed transistor technology for digital and analog mixed-signal applications. Nevertheless,

several areas were identified to improve robustness, including choice of metallization scheme for bonding pads, and better passivation layer to protect the intrinsic DUT from moisture and reactive gases. Future research on the reliability of the DUT at high temperature, e.g. dynamic R_{ON}, would be valuable for a comprehensive understanding of the p-GaN-gated HEMT and their eventual large-scale application in HT electronics.

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GaN Ring Oscillators Operational at 500 °C Based on a GaN-on-Si Platform

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***Abstract*— A study of GaN for high temperature (HT, up to 500 °C) digital circuits was conducted. A HT-robust GaN-on-Si technology based on enhancement-mode p-GaN-gate AlGaN/GaN high electron mobility transistors (HEMTs) and depletion-mode AlGaN/GaN HEMTs was proposed and used to implement different digital circuit configurations, namely E/D-mode and E/E-mode (E: enhancement, D: depletion). The E/D-mode inverter was found to offer significantly better performance in terms of voltage swing, noise margin, and gain, across temperature and V_{DD} scaling. As calculated from E/D-mode ring oscillators (ROs) with $L_G = 2$ μm, a RO exhibited a propagation delay (t_p) of < 1.48 ns/stage at 500 °C. The best RO achieved t_p < 0.18 ns/stage at 25 °C. To the best of the authors' knowledge, the proposed technology sets a new boundary of t_p *vs.* L_G in wide band gap digital logic, and is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology for emerging HT applications at 500 °C and beyond.**

***Index Terms*— GaN, p-GaN-gate, transistor, high temperature, E/D-mode, E/E-mode, ring oscillator, propagation delay.**

I. Introduction

EMERGING applications such as deep well oil drilling, hypersonic aircrafts, and exploration of Venus require high temperature (HT)-rated electronics components beyond the Si technology's typical temperature limit of 250 °C [1], [2]. Wide band gap semiconductors (SiC and GaN) are well suited to meet this demand thanks to their wide band gap and negligible carrier thermal generation at these temperatures [3]. While SiC HT digital circuits based on several transistor types have been proposed [4], [5], [6], [7], GaN and III-N materials offer significant advantages in a *wider* range of applications from power [8], [9], [10] and RF [11], [12], [13], to MEMS [14], [15] and digital circuits [16], [17] across a large range of temperatures (from deep cryogenic temperature of 4 K to HT > 1000 °C). In spite of these opportunities, their use in HT digital and analog circuits remains a relatively unexplored area.

For GaN digital circuits, an Enhancement-mode (E-mode) transistor is highly desired to avoid the need of an additional negative voltage supply (V_{SS}) [18]. This E-mode transistor could be realized using a number of technology options, including, (1) F-plasma treatment of gate region [19]; (2) recessed MIS gate [20]; (3) FinFET [21]; (4) p-GaN-gate [22]. Among these, the p-GaN-gate is especially interesting for HT robust operation thanks to the lack of gate dielectric (which degrades at HT and may introduce traps at the dielectric/semiconductor interface), and simplicity in process flow. Furthermore, at the technology platform level, the p-GaN-gate AlGaN/GaN HEMT offers the possibility of monolithic integration with both depletion-mode (D-mode) n-FETs ([23], [24]) and E-mode p-FETs ([16], [17], [25], [26]).

In this work, HT digital circuits were realized based on p-GaN-gate AlGaN/GaN HEMTs which are optimized for HT operation and have been demonstrated to offer robust performance at least up to 500 °C [27]. The DC (static) performance of inverters with two different circuit configurations (E/D-mode and E/E-mode) was studied. Based on the results at the inverter-level, ring oscillators (ROs) were demonstrated in order to understand the propagation delay (t_p), an important performance metric for HT digital circuits.

II. Choice of Inverter Circuit Configuration

As illustrated in Fig. 1(a), the wafer platform used in this work is p-GaN/AlGaN/GaN-on-Si and allows for the monolithic integration of two types of transistors, E-mode p-GaN-gate AlGaN/GaN HEMTs and D-mode AlGaN/GaN HEMTs, using the process flow described in [28]. Here, HT transistors with refractory metal gate and self-alignment in p-GaN-gate were fabricated. The typical transfer characteristics of the E-mode and D-mode transistors ($L_G = L_{GS} = L_{GD} = 2$ μm) are shown in Fig. 1(b). Good ON-OFF ratio (> 3×10^7, limited by gate leakage) and V_{th} of 1.4 V at room temperature are obtained for the E-mode transistors. The D-mode transistor shows a V_{th} of −1 V.

In order to identify the optimal implementation of the GaN high temperature logic, the characteristics of two classic inverter configurations (E/D-mode and E/E-mode inverters) (Fig. 1(c)) were experimentally evaluated at high temperature.

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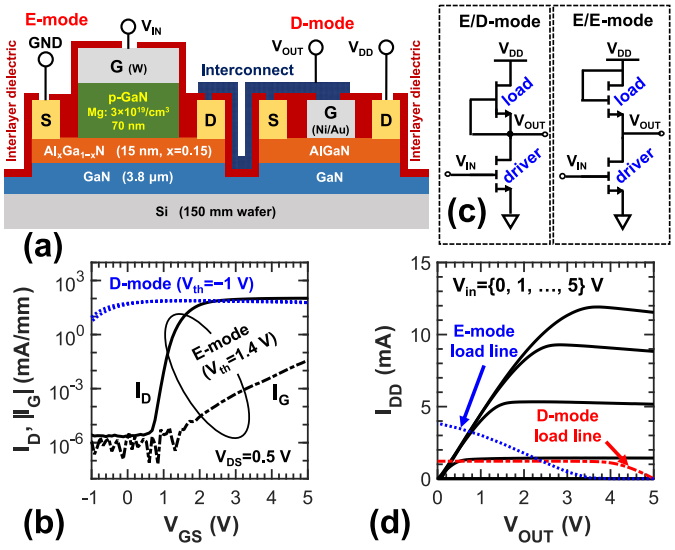

Fig. 1. Transistor technology and circuit configurations of *n*-FET only logic. (a) Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter. In all transistors, $L_G = L_{GS} = L_{GD} = 2$ μm. (b) Typical transfer characteristics of the E-mode and D-mode transistors. (c) Circuit configurations of E/D-mode and E/E-mode logic. (d) IV curves of an E-mode transistor ($W/L = 36/2$ μm/μm). $I_{D,max} = 330$ mA/mm, $R_{ON} = 12$ Ω·mm (measured at $V_{GS} = 5$ V). The load line, realized using a either D-mode or E-mode transistor ($W/L = 12/2$ μm/μm), is also included. The above measurements are conducted at room temperature.

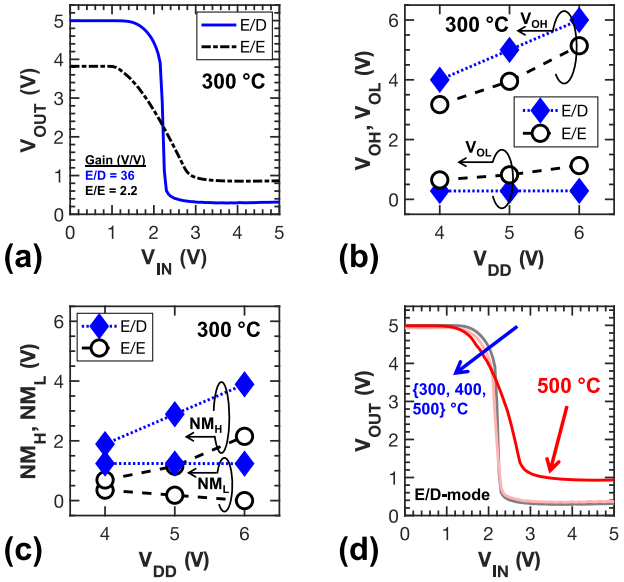

Fig. 2. Comparison of E/D-mode and E/E-mode inverters. (a) VTC at 300 °C. Maximum voltage gains of E/D-mode and E/E-mode are 36 V/V (at $V_{in} = 2.1$ V) and 2.2 V/V (at $V_{in} = 2.6$ V), respectively. (b) V_{OH}, V_{OL} *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. V_{swing} may be calculated by $V_{OH} - V_{OL}$. (c) Noise margins (NM_L, NM_H) *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. (d) VTC of E/D-mode up to 500 °C.

In principle, the E/E-mode inverter offers: (1) higher simplicity, (2) higher current, and (3) higher speed at higher V_{DD}, while the E/D inverter features (1) lower power consumption, (2) better gain, voltage swing (V_{swing}), and noise margin (NM), and (3) higher speed at lower V_{DD}, based on basic digital circuit theory and the prior work in other semiconductor technologies [29]. In the inverters of this work, the driver and load transistors are set to $W/L = 36/2$ μm/μm and $12/2$ μm/μm, respectively. The transistor sizing is determined based on: (1) the characteristics of the load line (Fig. 1(d)), (2) trade-offs between symmetricity in the DC (static) and transient (dynamic) characteristics of the inverter, (3) tolerance to non-uniformity and temperature variation in transistor characteristics, and (4) layout area. For a fair comparison between E/D-mode and E/E-mode, the same sizing is used.

A comparison of the voltage transfer curves (VTCs, Fig. 2(a)) at 300 °C reveals that, the E/D-mode inverter features significantly better performance than the E/E-mode inverter, in terms of V_{swing} ($= V_{OH} - V_{OL}$), gain, and NM. This is because: (1) In E/D-mode, $V_{OH} = V_{DD}$, whereas in E/E-mode, $V_{OH} = V_{DD} - V_{th(E)}$; (2) In both circuit configurations, V_{OL} is limited by the voltage drop across the E-mode driver. While the R_{ON} of both drivers is similar, the current drive of the E-mode load (diode-connected), when input is HIGH, is significantly stronger than that of the D-mode load (GS-tied) (Fig. 1(d)).

The above observations are also valid with the scaling of V_{DD}, an important design parameter in digital circuits (Fig. 2(b)–(c)). With the increase in V_{DD}, the V_{swing} of E/D-mode and E/E-mode inverters generally improves. However, the magnitude of improvement is better for the E/D-mode, thanks to the constant V_{OL} across different V_{DD}. When the output is LOW, the R_{ON} of the E-mode driver is almost independent of V_{DD} (Fig. 1(d)). To first order, the D-mode load supplies a constant current, compared to the current of E-mode load with V_{DD}^2 dependency, leading to a better V_{OL} at higher V_{DD}.

Having established that E/D-mode technology offers significantly better performance in GaN digital circuits at 300 °C, the temperature dependence of E/D-mode was further studied for higher temperatures. Measurements beyond 300 °C were conducted using a probe station with a hot chuck (maximum rating of 500 °C) and sealed chamber in N_2 ambient. As presented in Fig. 2(d), the VTC of the E/D-mode remains largely constant up till 400 °C, though NM_L is reduced slightly (by ~0.15 V) due to the faster degradation in the ON-resistance of the E-mode driver transistor than in the D-mode load transistor. At 500 °C, an increase in V_{OL} (hence reduction of V_{swing} by 0.6 V_{PP}) was observed, which can also be explained by the faster degradation of the E-mode device ON-resistance.

III. High Temperature Ring Oscillator and Propagation Delay

In order to estimate the t_p of the proposed GaN E/D-mode technology, ROs were fabricated with $(W/L)_{\{E,D\}} = \{36/2, 12/2\}$ μm/μm (Fig. 3(a)). t_p was calculated by $T_{RO}/2N_{RO}$, where T_{RO} is the period of the RO waveform V_{OUT}, N_{RO} is the number of stages of the RO. The V_{DD} scaling trends of ROs were compared at 300 °C (Fig. 3(b)). The t_p may be modeled as $\frac{1}{2}C_L \times V_{DD}/I_{ave}$, where C_L is the load capacitance, and I_{ave} is the average charge/discharge current. To first order, the charge current through the D-mode load is constant with V_{DD} (refer to Fig. 1(d)), therefore t_p from LOW to HIGH (t_{pLH}) is proportional to V_{DD}. The discharge current through the E-mode driver, same as Si CMOS circuits, is roughly proportional to V_{DD}^2, therefore $t_{pHL} \propto 1/V_{DD}$.

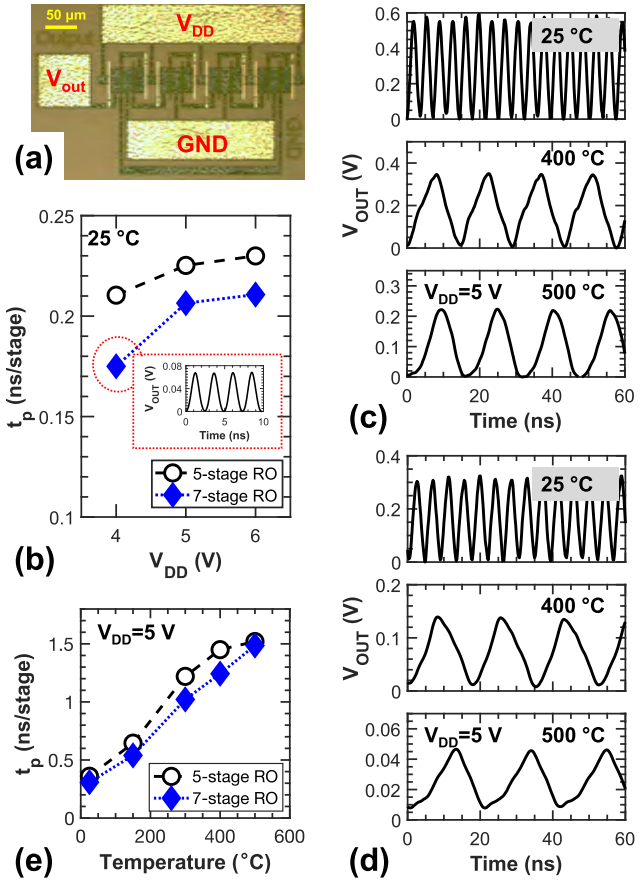

Fig. 3. GaN ring oscillators (ROs). (a) Micrograph of a 7-stage RO. (b) V_{DD} scaling trend of the best 5-stage RO and 7-stage RO at 25 °C. The inset presents the output waveform V_{OUT} of the 7-stage RO which demonstrates the best $t_p < 0.18$ ns/stage in this work. (c) Waveforms of another 5-stage RO at various temperatures. (d) Waveforms of another 7-stage RO at various temperatures. (e) t_p *vs.* temperature, estimated from the data reported in (c)–(d).

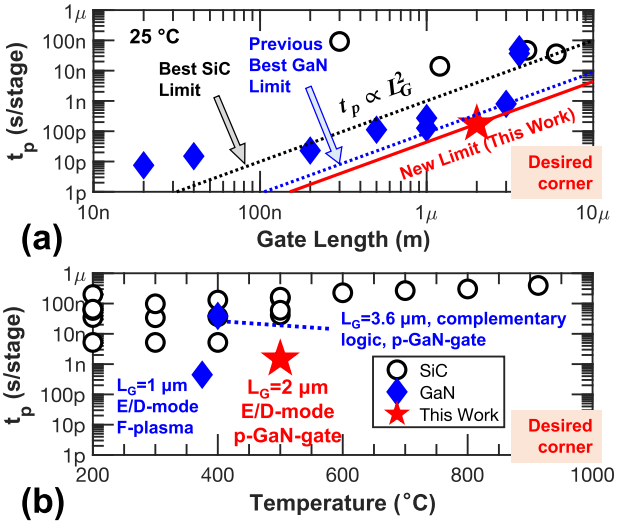

Fig. 4. A summary of ROs reported in the literature based on wide band gap electronics (GaN [17], [19], [22], [30], [31], [32], [33] and SiC [4], [5], [6], [7]). (a) t_p *vs.* L_G. The general scaling trends ($t_p \propto L_G^2$) for the best SiC demonstration, previous best GaN demonstration and the best result of this work (Fig. 3(b) inset) are included for reference. The L_G of the pull-down transistor is chosen. (b) t_p *vs.* temperature. The data points showing GaN RO demonstrations are labelled with the L_G of the pull-down transistor, the logic family/circuit configuration and the type of E-mode n-FET. To the best of the authors' knowledge, the proposed technology in this work defines a new boundary of t_p *vs.* L_G, as well as the operating temperature of GaN digital circuits.

Due to the significantly lower charge current, t_{pLH} dominates t_p. Hence, a lower V_{DD} results in a lower t_p. However, the reduction of V_{DD} results in trade-offs in NM and V_{swing} (Fig. 2(c)–(d)). Therefore, V_{DD} of 5 V was chosen for the RO as a compromise.

The ROs were operational at 500 °C, as shown in Fig. 3(c). The degradation of t_p from 0.31 ns/stage (25 °C) to 1.48 ns/stage (500 °C) (Fig. 3(d)) may be attributed to the performance degradation of both E/D-mode transistors (increase in R_{ON} of the E-mode driver, reduction in current drive capability of the D-mode load) and an increase in parasitics.

The best RO of this work ($t_p < 0.18$ ns/stage, Fig. 3(b) inset) was benchmarked against other ROs based on wide band gap electronics (GaN [17], [19], [22], [30], [31], [32], [33] and SiC [4], [5], [6], [7]). As shown in Fig. 4(a), to the best of the authors' knowledge, at room temperature, the proposed technology sets a new boundary in the well-known relationship of t_p *vs.* L_G^2 [34]. Furthermore, as shown in Fig. 4(b), the reported RO is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology, which is based on p-GaN-gate AlGaN/GaN HEMTs optimized for HT ($\geq$ 500 °C) applications.

The measured values of t_p should be considered as an upper limit for the intrinsic t_p. As verified in Fig. 3(d), ROs with more stages would give a more accurate estimation of the intrinsic t_p. In the RO, in addition to the odd number of inverters connected in a circular chain, an output buffer is used for the readout of the output waveform (V_{OUT}). This buffer stage introduces a fixed delay whose relative contribution decreases as the number of stages increases. In this experiment, the number of stages in the E/D-mode RO was limited by the uniformity and yield of the fabrication. On the other hand, for E/E-mode ROs, the number of stages is limited by the low gain and low noise margins (especially NM_L) of each E/E-mode inverter stage (Fig. 2(a)), which makes the oscillations extremely difficult at high temperature.

IV. Conclusion

A study of E/D-mode and E/E-mode inverters realized by HT-optimized E-mode p-GaN-gate HEMT technology based on a GaN-on-Si platform was conducted. E/D-mode inverters were found to offer significantly higher performance than E/E-mode inverters at 300 °C. The reported RO exhibited a t_p of $<$ 1.48 ns/stage at 500 °C. The best RO achieved $t_p <$ 0.18 ns/stage at 25 °C with $L_G = 2$ μm. Further advancement of the proposed technology, e.g. optimization of the epitaxial structure, reduction of layout parasitics, and introduction of HT-rated advanced packaging [35], could significantly push the performance limit of GaN HT electronics.

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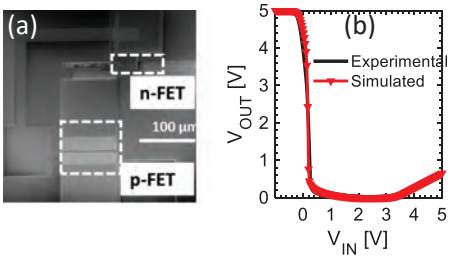

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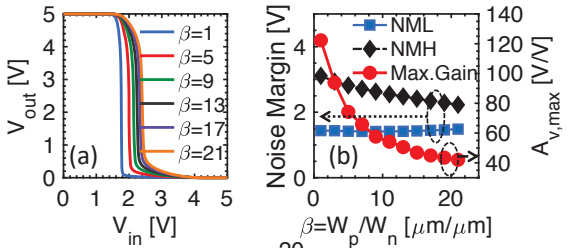

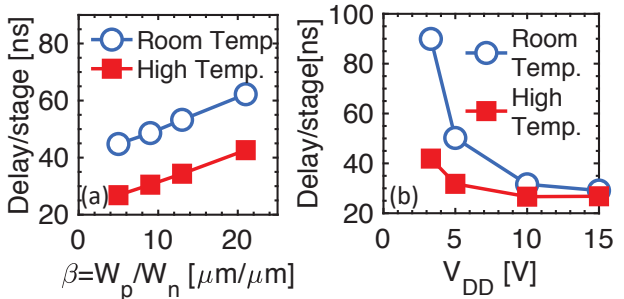

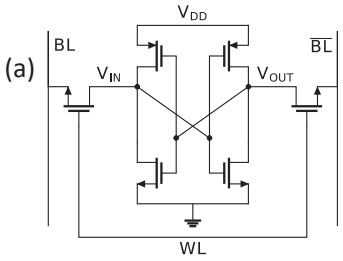

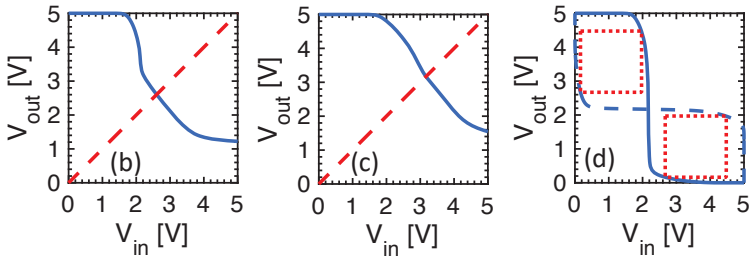

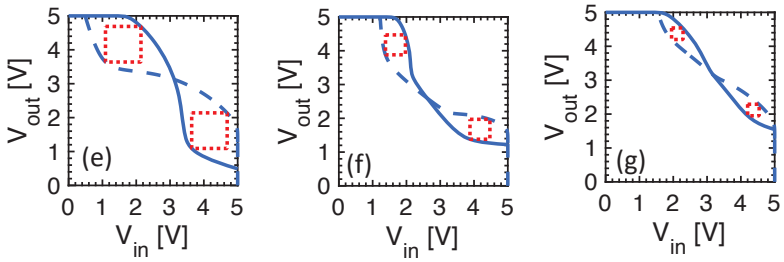

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Regrowth-Free GaN-Based Complementary Logic on a Si Substrate

Nadim Chowdhury, *Student Member, IEEE*, Qingyun Xie, *Student Member, IEEE*, Mengyang Yuan, *Student Member, IEEE*, Kai Cheng, Han Wui Then, *Senior Member, IEEE*, and Tomás Palacios, *Fellow, IEEE*

***Abstract*— This paper demonstrates a complementary logic circuit (an inverter) on a GaN-on-Si platform without the use of regrowth technology. Both n-channel and p-channel GaN transistors are monolithically integrated on a GaN/AlGaN/GaN double heterostructure. N-channel FETs show enhancement-mode (E-mode) operation with a threshold voltage around 0.2 V, ON-OFF current ratio of 10^7 and R_{ON} of 6 Ω · mm, while the p-channel FETs show E-mode operation with V_{th} of −1 V, ON-OFF current ratio of 10^4 and R_{ON} of 2.3 kΩ·mm. Complementary logic inverters fabricated with this technology yield a record maximum voltage gain of ∼27 V/V at an input voltage of 0.59 V with $V_{DD} = 5$ V. Excellent transfer characteristics have been obtained up to 300 °C operating temperatures, which demonstrates the suitability of this technology for low-power high-temperature electronic applications.**

***Index Terms*— GaN CMOS, AlGaN, integrated circuit, high temperature operation.**

I. Introduction

By 2030, about 80% of the power generated in United States will go through or get recycled by some sort of power electronics circuits [1]. The power density (and form-factor) of these power electronic circuits is often dominated by the size of passive components like inductors and capacitors, which depends on the operating frequency [2]. By increasing the switching speed of power electronic circuits, the energy storage requirement of inductors and capacitors can be significantly reduced, which allows for smaller components. However, the maximum operating frequency of a state-of-the-art GaN transistor, one of the promising candidates for high voltage compact switches, is typically limited by the gate inductance between the gate electrode and the driver circuit [2], [3]. This inductance can be significantly reduced by monolithically integrating the driver circuit and power transistor on the same chip.

Recently, there has been a number of demonstrations of GaN-based power integrated circuits (IC) [4]–[6]. However, all of these demonstrations rely on the integration of enhancement mode (E-mode) and depletion mode (D-mode) n-type AlGaN/GaN High Electron Mobility Transistors (HEMTs), a technology that suffers from static power dissipation and reduced voltage swing at the output. To increase the efficiency of GaN-based ICs, a CMOS-like circuit technology is needed. Major benefits of such a technology are that it consumes zero or negligible static power, reduces the circuit complexity and it also offers higher noise immunity and linearity [7]. However, the lack of high-performance GaN p-FETs and the challenges of its monolithic integration with E-mode n-FET devices are major roadblocks towards achieving such a technology. Although a number of GaN p-FETs have been recently demonstrated on various epitaxial structures [8]–[15], their integration with n-FET devices requires expensive regrowth technology and/or the use of non-Si substrates. This work proposes and demonstrates a new GaN-based complementary circuit platform which overcomes these challenges.

II. Epitaxial Structure

The epitaxial stack used in this work was grown by Enkris Semiconductor, Inc. on a 6 inch Si (111) substrate using metal organic chemical vapor deposition (MOCVD). The structure, from top to bottom, is as follows: 20 nm p^{++}-GaN (Mg: 6×10^{19} cm^{-3} with 2–3% ionization at room temperature), 50 nm p-GaN (Mg: 1×10^{19} cm^{-3}), 20 nm UID-GaN (Si: 5×10^{16} cm^{-3}), 20 nm $Al_{0.2}Ga_{0.8}N$ (Si: 5×10^{16} cm^{-3}), 150 nm UID-GaN (Si: 5×10^{16} cm^{-3}), 3.8 μm proprietary III-Nitride buffer, and Si <111> substrate (Fig. 1(a)). The activation of p-GaN is performed in the MOCVD chamber right after the growth, by annealing in N_2 ambient at 750 °C for 45 min. From X-ray diffraction measurements, the estimated total threading dislocation is found to be 10^9 – 10^{10} cm^{-2}. The GaN/AlGaN/GaN double heterostructure allows the formation of both a two-dimensional hole gas (2-DHG) and a two-dimensional electron gas (2-DEG) at the top and bottom heterointerface respectively, due to polarization difference.

III. Fabrication of the Inverter

The fabrication starts with etching the top p^{++}-GaN, p-GaN and UID-GaN layers from the source and drain regions of

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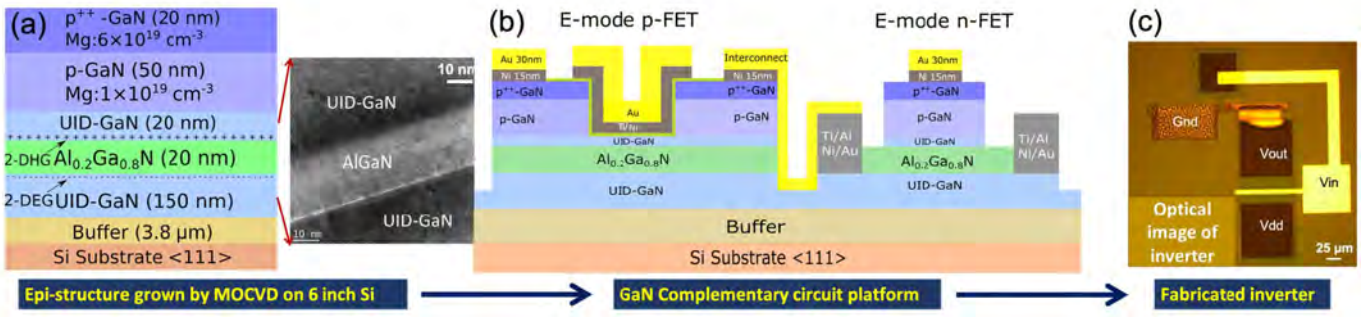

Fig. 1. (a) Cross-section schematic of the epitaxial structure used in this work along with a transmission electron micrograph (TEM) image of the double heterostructure used for the n-type and p-type channels; (b) Schematic of the demonstrated GaN complementary circuit platform; (c) Optical image of the complementary logic inverter fabricated on this platform.

the n-FET by using selective dry etching technology [16]. A Ti (20 nm)/Al (100 nm)/Ni (25 nm)/Au (50 nm) ohmic metal contact is then deposited by electron beam evaporation. An ohmic contact to the 2-DEG is formed by annealing the Ti/Al/Ni/Au metal stack at 800 °C in N_2 ambient. Then, mesa etch is performed by Cl_2/BCl_3-based Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) using photo-resist mask to define the active region of both n- and p-FETs. The photoresist is removed by oxygen plasma etching. A timed Cl_2/BCl_3-based ICP-RIE process is used to etch 70 nm of p^{++}-GaN and p-GaN using photoresist as the etch mask for the p-FET. Following the gate recess etch of the p-FET, the sample is dipped into heated 25 % tetramethylammonium hydroxide (TMAH) for 10 min. This TMAH dip removes the photoresist and reduces the etch-induced roughness.

Ni/Au-based source and drain ohmic contacts for the p-FET devices are formed on top of the p^{++}-GaN layer using photolithography and lift-off technologies. A Ni/Au-based gate electrode is also defined in the n-FETs at this time. The sample is then annealed in O_2 ambient at 550 °C for 3 min so that Ni can be oxidized into NiO_x to form ohmic contact to p^{++}-GaN layer. Next, a 20 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition. Finally, Ti (10 nm)/Ni (20 nm)/Au (100 nm) gate electrodes are defined by electron beam evaporation and lift-off technology for p-type transistors. This step also serves as the interconnect layer to connect both n- and p-FETs gates. Fig. 1(b) shows the schematic cross-section of the demonstrated GaN complementary inverter. Fig. 1(c) shows the top view of the fabricated device.

IV. Results and Discussion

Fig. 2(a) shows the I_D-V_{GS} characteristics of the fabricated n-FET ($L_G = 4\ \mu$m, $L_{SD} = 12\ \mu$m) with a ON-OFF current ratio of $\sim 10^7$ and threshold voltage of 0.2 V. An ON-resistance of 6 $\Omega \cdot$ mm and good pinch-off behavior can be observed in the output characteristics of the same device in Fig. 2(b). The I_D-V_{GS} characteristics of the fabricated p-FET ($L_G = 2\ \mu$m, $L_{SD} = 6\ \mu$m) are shown in Fig 2(c), which demonstrate an ON-OFF current ratio of 10^4 and threshold voltage around -1 V. Both the ON-OFF ratio and the threshold voltage can be tuned by controlling the recess depth [11]. The output characteristics of the same p-FET show an ON-resistance of 2.3 k$\Omega \cdot$ mm with good pinch-off behavior (see Fig. 2(d)). A 2-DHG density of 5×10^{12} cm^{-2} and mobility of 10 cm^2/V•s

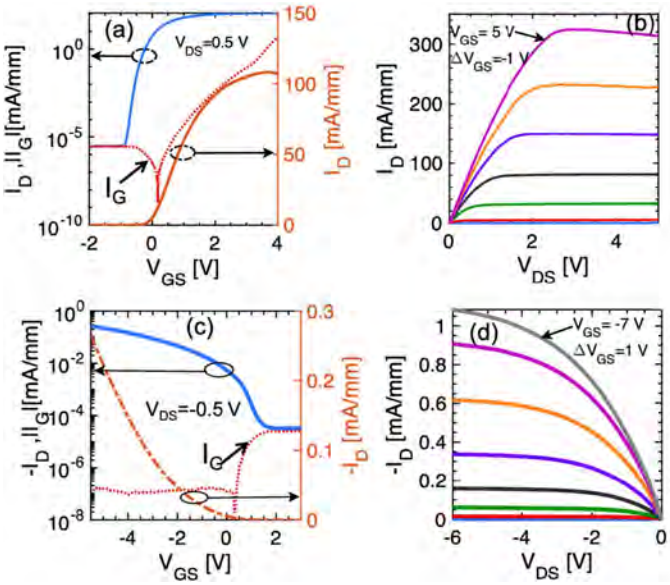

Fig. 2. (a) I_D-V_{GS} characteristics of the n-FET in logarithmic (along with gate leakage I_G◁ and linear scale showing an ON-OFF ratio of $\sim 10^7$ and threshold voltage of 0.2 V ($V_{DS} = 0.5$V); (b) I_D-V_{DS} characteristics of the n-FET; (c) I_D-V_{GS} characteristics of the p-FET in logarithmic (along with gate leakage I_G) and linear scale showing an ON-OFF ratio of $\sim 10^4$ and threshold voltage of -1 V ($V_{DS} = -0.5$V); (d) I_D-V_{DS} characteristics of the p-FET shows ON-resistance of 2.3 k⁀· mm. For a $|V_{GS}|$ transition from 0 to 5 V, the ON-OFF ratio for both n-FET and p-FET is $\sim$100.

were obtained through the characterization of FAT-FET structures with a gate length of 100 μm. The poor performance of p-FET in terms of ON-resistance can mainly be attributed to the higher ohmic contact resistances [14].

Fig. 3(a) shows the DC transfer characteristics of the inverter for a V_{DD} of 5 V. A few observations could be made from these measured characteristics. First, unlike E/D-mode inverters [17], the transfer curve of the reported complementary logic inverter shows very good switching transition from high to low voltage with a swing voltage V_{swing} of 4.91 V. The transfer also yields a voltage gain of $\sim$27 V/V at an input voltage of 0.59 V. Second, the transition from high-to-low occurs at $\sim$0.2 V due to a relatively low threshold voltage of the n-FET of 0.2 V. Ideally, the transition from high-to-low voltage for a complementary inverter should occur near $V_{DD}/2$. The low threshold voltage in the n-FET is due to the insertion of 20 nm UID-GaN layer between p-GaN and AlGaN. This impact of this layer on the threshold voltage of

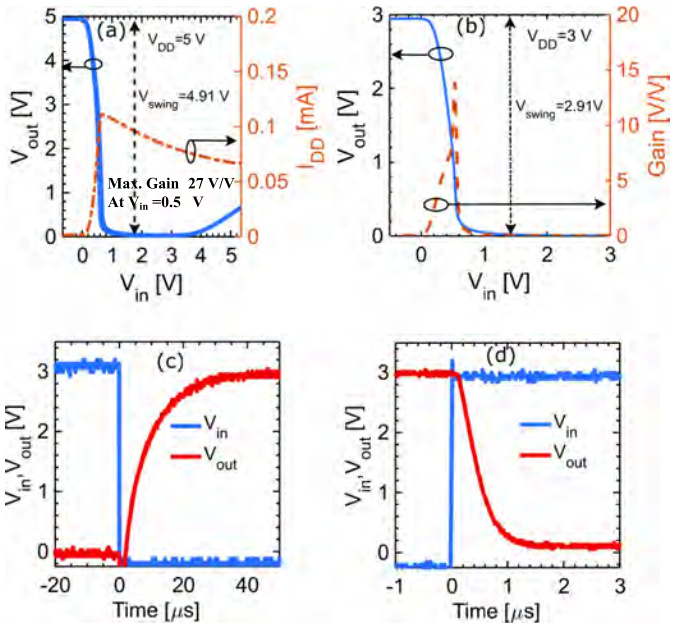

Fig. 3. DC transfer curve of the fabricated inverter with (a) V_{DD} = 5 V and (b) V_{DD} = 3 V. Transient response of the inverter showing (c) rise time and (d) fall time. (W_n/W_p = 12/110 μm).

n-FET is around 1 V [14]. In addition, the threshold voltage could be increased even further by fabricating Fin-FET-like structures with Tri-gate [18].

Third, the input voltage starts to rise around 3.6 V, this is because of the gate leakage from the p-GaN gated n-FET. This effect can be eliminated in future by fabricating a Fin-like structure with, gate-oxide and Tri-gate [18]. The gate oxide would significantly reduce the gate leakage hence preventing the V_{out} from increasing. Nevertheless, the demonstrated technology is deemed suitable for V_{DD} less than 3.5 V. Fig. 3(b) shows the transfer characteristics for V_{DD} = 3 V exhibiting excellent inverting behavior with V_{swing} = 2.91 V and maximum gain of ~15 V/V.

Finally, the dynamic switching of the inverter was characterized by connecting the inverter input to a pulse generator, and the output to the high impedance port of an oscilloscope. The V_{DD} was kept at 3 V because of the high gate leakage in the p-GaN gated n-FET above that voltage. The voltage of the input pulses varied from −0.2 V to 3 V with a ramp time of 100 ns. Measured waveforms of the input and output signals are presented in Fig. 3(c)-(d). The output signal showed a voltage swing close to 0~3 V. The fall time was 1 μs; and rise time was 20 μs. It should be noted that these times represent an upper bound on the fall and rise times, as the measurements are limited by the very high input capacitance of the oscilloscope port (~350 pF). Table I benchmarks this work against some of the GaN complementary logic inverters reported in the literature.

The fabricated inverters were also characterized under high temperature operation in a Cascade Microtech Tesla 200 probe station with thermal chuck. As shown in the Fig 4(a), the voltage gain is reduced as the temperature is increased. The maximum available voltage swing at the output is also reduced due to the rise of low-level V_{out}, which can be attributed to the reduction in ON-OFF current ratio of the p-FET at

TABLE I
COMPARISON OF PERFORMANCE METRICS FOR DEMONSTRATED GaN COMPLEMENTARY LOGIC INVERTERS

Affiliation	Substrate	V_{DD} [V]	Gain [V/V]	V_{swing} [V]	t_{rise} [µs]	t_{fall} [µs]	C_{load} [pF]	W_n/W_p [µm/µm]
RWTH [19]	Sapphire	1	-	0.65	-	-	-	-
HRL [20]	Sapphire (regrowth)	5	9.6	4.4	0.09	0.67	-	50/500
MIT (This work)	Si	3	15	2.91	20	1	350	12/110
		5	28	4.91	-	-	350	12/110

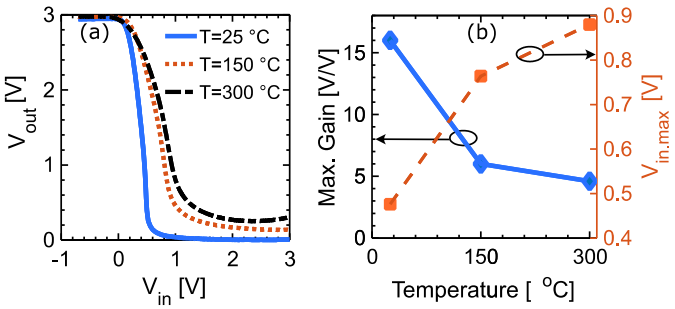

Fig. 4. Temperature dependence of inverter DC characteristics. (a) DC transfer curve; (b) Maximum gain and input voltage.

TABLE II
NOISE MARGINS OF THE INVERTER MEASURED AT DIFFERENT TEMPERATURES. V_{DD} WAS FIXED AT 3 V

Temperature	RT	150 °C	300 °C
Low-level noise margin (NM_L)	0.12 V	0.09 V	0.04 V
High-level Noise margin (NM_H)	2.24 V	1.82 V	1.75 V

high temperature. Table II summarizes the measured Low-Level Noise Margin (NM_L) and High-Level Noise Margin (NM_H) of the inverter at various temperatures (from room temperature (RT) to 300 °C). A reduction in the noise margins are observed at higher temperatures compared to RT, which can be attributed to performance degradation of both n-FET and p-FET at higher temperature.

To the best of our knowledge, these results are the first demonstration of operation at 300 °C of any complementary logic technology, which confirm the potential of GaN for low-power digital applications under harsh environment operation.

V. CONCLUSION

In this work, a GaN complementary circuit technology is demonstrated. The enhancement-mode GaN n-FET and p-FET are monolithically integrated on a Silicon substrate without any regrowth step. The reported inverter exhibits 0-to-5 V voltage switching with a record voltage gain of 27 V/V. Transient characteristics with 0 V-to-3 V switching show a fall time of 1 μs and rise time of 20 μs with 350 pF load. While there is room for significant performance improvement, this demonstration opens up a number of application domains for GaN such as integrated CMOS driver circuits, CMOS logic, logic and signal conditioning under harsh environment operation, among many others.

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