Power Devices and Circuits

Large-Signal Characterization of Piezoelectric Resonators for Power Conversion

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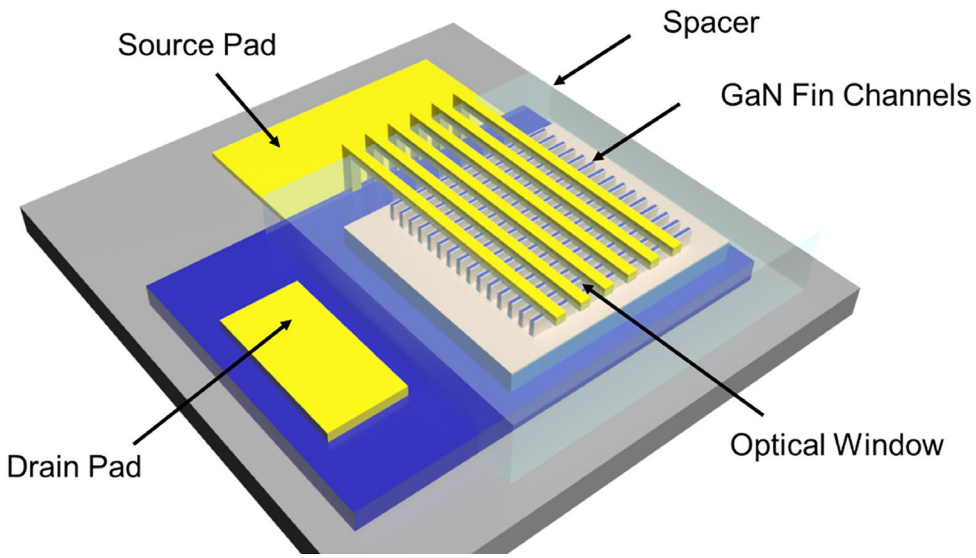
Sponsorship: Texas Instruments, NSF Graduate Research Fellowship

As the world moves towards increased electrification and integration of renewable energy sources, there is a need for smaller, lighter, and more efficient power converters. Magnetics are key components of conventional power converters, but they are often the bottleneck to achieving high power density due to their size, weight, and poor performance at small sizes. Piezoelectric devices, when operated in their inductive regime, can serve a purpose similar to that of magnetic components and offer favorable scaling properties as components are miniaturized. Several sources have demonstrated the viability of piezoelectric-based power converters, but selection of the optimal material and component size is limited by a lack of data on the performance of these materials at high drive levels. This work aims to fill that gap by collecting data to examine the variation in resonator quality factor, a geometry-independent metric for the power processing efficiency. The quality factor is measured across a range of drive levels for multiple resonator sizes, frequencies, and materials. By normalizing the collected data against resonator geometry, material trends are derived that can predict resonator losses under high drive levels, offering more insight into realistic converter operation than the currently available small-signal data sheet values. Based on these trends, implications for converter efficiency and selection of material and dimensions are discussed.

First Demonstration of Optically Controlled Vertical GaN Power FinFETs

J.-H. Hsia, J. Perozek, T. Palacios
Sponsorship: Office of Naval Research (Grant No. N00014-22-1-2468)

In recent years, the boost in consumer electronics and data centers has increased the electricity demand. The delivery and transformation of power though electric grids require many efficient power converters and electronics that can withstand high current and voltages. However, traditional power electronics are mostly electrically triggered, which can complicate the circuitry design and cause electromagnetic interference (EMI). The use of optically triggered devices will simplify the circuitry design, reduce EMI, and potentially increase the operating frequency, which can lead to more reliable systems with reduced costs. However, most optically triggered devices require the use of complex and expensive ultraviolet lasers due to low optical responsivities. In this work, we have demonstrated optically controlled vertical GaN transistors with J_{DS} > 90A/cm² at V_{DS} = 3V under an illumination intensity of 1μW, which translates into a high optical responsivity, > 10^5 A/W, allowing such devices to be triggered by light-emitting diodes. The initial results have demonstrated potential of these devices for future high-power electronics.



▲ Figure 1: Three-dimensional schematic of an optically triggered, vertical GaN fin field-effect transistor (FinFET).

FURTHER READING

- J.-H. Hsia, J. A. Perozek, and T. Palacios, "First Demonstration of Optically-Controlled Vertical GaN finFET for Power Applications," *IEEE Electron Device Letts.*, vol. 45, no. 5, pp. 774-777, May 2024. doi: 10.1109/LED.2024.3375856

In-situ Monitoring of GaN Power Transistor Parameters Under Continuous Hard-switching Operation

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Sponsorship: Analog Devices

Gallium Nitride (GaN) transistors have garnered attention in the field of power electronics due to their high-speed switching capabilities, low on-resistance, and excellent thermal properties. GaN devices are commonly used in applications like power supplies, electric vehicles, and Radio Frequency (RF) amplifiers. However, their switching reliability is a crucial consideration.

There are many challenges to be addressed to improve GaN switching reliability, including robust gate drive circuitry, effective thermal management, and protection against voltage and current spikes during switching events. Additionally, GaN transistors can be sensitive to voltage and temperature stresses, requiring careful consideration in design and application.

The aim of our work is to devise techniques to continuously monitor GaN Power transistor parameters under hard-switching operation, and to investigate the role of switching transitions on device parameter drift. To this end, we have constructed a unique experimental setup while taking thermal management into account. The setup is capable of repeating the Double-Pulse Testing Technique multiple times and measuring device parameters in-situ as well as maintaining device temperature to avoid self-heating.

In summary, GaN transistors offer significant advantages in terms of switching reliability, especially in high-frequency and high-power applications. However, their successful deployment demands proper design, thermal management, and protection measures to ensure long-term performance and reliability in various electronic systems.

Low-Power Robot Platforms for Development of Energy-Efficient Algorithms for Pose Estimation, Mapping, and Activity Planning

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Sponsorship: MIT Department of Aeronautics and Astronautics

Small-form autonomous robots are becoming quicker and more performant, giving them the potential to change the way we approach missions like environmental monitoring, search and rescue, and medicine. However, in order to enable long-duration missions, these robots must be extremely energy-efficient to compensate for their small batteries. Unlike in larger robotic systems, the energy spent sensing, mapping, estimating pose, and motion planning on small-form robots is comparable to energy spent on their actuators. In this work, we have used a small robotic car to begin collecting real-time computation and actuation power data using onboard power sensors and real-time pose data using a motion capture system. We have set a power consumption baseline for this autonomous robot of 0.41 W over a 0.60 W idle when moving at 0.32 m/s that will be used to compare the power consumption of different path-planning algorithms on a common platform. We will also test early-termination algorithms that stop computation on a path-planner early based on estimated energy consumption over execution of the path. Future work includes experiments using different path-planning and early-termination algorithms, and work on including computation energy in mapping and pose estimation algorithms optimized for total energy consumption. This research is novel in considering the energy consumption of computing hardware when optimizing path-planning algorithms for total energy consumption, and aims to demonstrate a new method for increasing the lifetime of severely energy constrained autonomous robots.

High-Speed Controllable Transformation Matching Network for Enhanced RF Power Delivery in Semiconductor Plasma Processes

K. N. Rafa Islam, D. J. Perreault

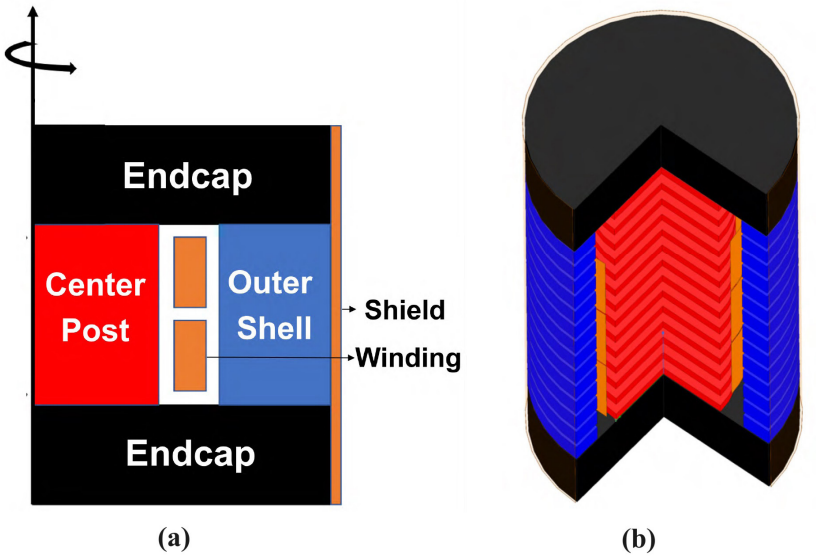
Efficient and controlled delivery of radio-frequency (rf) power for semiconductor plasma processing typically relies upon tunable matching networks to transform the variable plasma load impedance to a fixed impedance suitable for most rf power amplifiers. Plasma applications require fast tuning speed from the matching networks while operating at high frequency range. However, it is difficult to meet the requirements for many semiconductor plasma applications with conventional impedance matching solutions due to their limited response speeds. This slow speed comes from the presence of mechanical components in the matching network, since they can be tuned only mechanically. This work introduces a novel Controllable Transformation Matching Network (CTMN) intended to address the need for high-speed, tunable impedance matching. Here we show a controllable switching network at the core of the CTMN, leveraging switched-mode energy processing to provide high efficiency and exceptional control speed over a wide operational range.

The CTMN's design employs a two-port switching network coupled with a high-Q passive network, enabling rapid voltage adjustments and dynamic reactance tuning to swiftly accommodate both resistive and reactive load variations. Control strategies are introduced to maintain zero-voltage switching within the CTN as needed to minimize switching losses. This approach is substantiated through simulations, which indicates the CTMN's capability to achieve precise impedance matching with the potential for substantially faster response times (microseconds range) than traditional systems. It is anticipated that the proposed approach will enable ultra-fast, high-efficiency tunable impedance matching to address the needs of modern plasma systems.

High-Performance High-Power Inductor Design for High-Frequency Applications

M. V. Joisher , R. S. Bayliss, M. K. Ranjram, R. S. Yang, A. S. Jurkov, D. J. Perreault
Sponsorship: MKS instruments, Inc.

Magnetic components significantly impact the performance and size of power electronic circuits. This is especially true at radio frequencies (rf) of many MHz and above. As operating frequencies rise, the impact of losses in both copper and core becomes a substantial hurdle. Hence, in the high-frequency (HF, 3-30 MHz) range, coreless (or "air-core") inductors are conventionally preferred over cored magnetics. These inductors have typical Q (Quality factor: a measure of an inductor's efficiency) of 200-500 and are often the major contributor to a system's overall loss and size. Even when they can achieve high-Q, air-core inductors can induce electromagnetic interference (EMI) and eddy current loss in surrounding components, thus limiting system miniaturization. With recent advances in high frequency magnetic materials, there is interest in the design of cored inductors to achieve improved combinations of size and loss. This work investigates an approach to achieving high power, high-frequency, high-Q cored inductors. The proposed design approach leverages high-frequency magnetic materials, core geometry, quasi-distributed gaps, and a shield winding to realize high-frequency inductors that emit little flux outside their physical volume. Design guidelines for such inductors are introduced and experimentally verified with a 500 nH inductor (Q = 1150) designed to operate at 13.56 MHz with a peak ac current of up to 80 Amps. Such high-Q inductors can enhance the performance of the overall circuit and enable space-efficient designs for high-frequency high-power applications (e.g. rf plasma generation, HF wireless power transfer).



▲Figure 1: (a) Radial cross-section of the proposed inductor design, featuring the center post, outer shell, end caps, copper shield and a single-layer winding. (b) 3D model with a transparent shield and a pie cut out for better visibility.

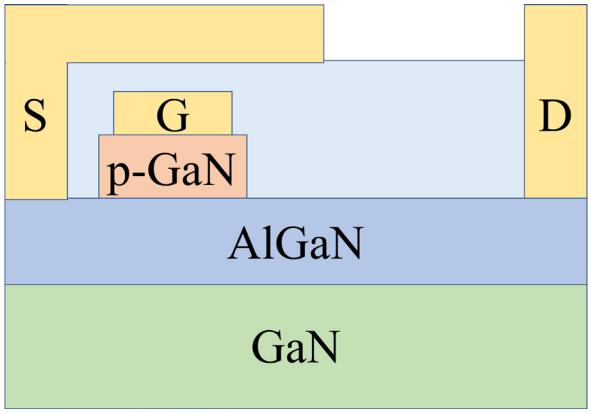
Gate Stack Design of p-GaN Gate GaN HEMTs

Y. Yu, J. A. del Alamo
Sponsorship: Texas Instruments

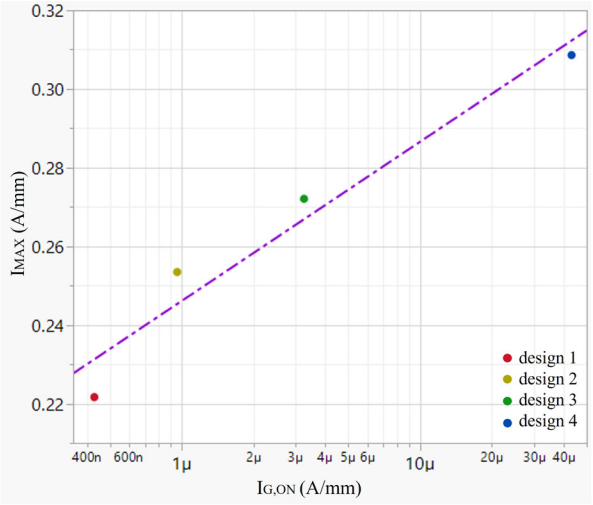
Gallium nitride (GaN) high electron mobility transistors (HEMTs) represent a significant advance in semiconductor technology, offering superior high-frequency and high-power capabilities. Despite their exceptional potential, the reliability of GaN HEMTs continues to be a critical challenge, particularly as it pertains to the variability in device behavior influenced by multiple factors including device scaling, thermal management, material defects, and susceptibility to electrical overstress. This study explores the reliability issues of p-GaN gate GaN HEMTs, the most promising structure for power management applications (Figure 1). In this work, we study the electrical characteristics of experimental transistors and correlate them with detailed characterization of specialized p-GaN test structures. In particular, we focus on understanding the impact of p-GaN gate design and fabrication process in transistor performance and reliability.

Our current experimental results suggest a strong connection between p-GaN gate process and electrical performance metrics, especially a trade-off between the peak saturation drain current (I_{MAX}) and ON-state current ($I_{G,ON}$). Generally, a gate design that yields a higher I_{MAX}, also results in higher $I_{G,ON}$. However, relatively modest process changes can result in large swings in I_{MAX} over 40% and $I_{G,ON}$ over two orders of magnitude (Figure 2). Our current studies of specialized test structures focus on understanding the origin of this phenomenon so as to synthesize device and process design guidelines.

The significance in this work extends beyond improving performance and reliability of GaN HEMTs. Our work aims to develop predictive models that can guide future GaN device design and fabrication techniques.



▲ Figure 1: Cross-sectional view of p-GaN gate GaN HEMT.



▲ Figure 2: Trade-off between I_{MAX} and $I_{G,ON}$ through four differently designed wafers.