IAB2025:

MTL Industrial Advisory Board Annual Meeting 2025

MTL MICROSYSTEMS TECHNOLOGY LABORATORIES

January 16, 2025
Cambridge, MA

MICROSYSTEMS TECHNOLOGY LABORATORIES • MASSACHUSETTS INSTITUTE OF TECHNOLOGY

IAB2025:

INDUSTRIAL ADVISORY BOARD ANNUAL MEETING
JANUARY 16, 2025

AGENDA

7:45am	**Breakfast**
8:30am	**MTL Director's update,** *Tomás Palacios*
9:00am	**Discussion with MIT/MTL Leadership** *Tomás Palacios and Marc Baldo*
9:30am	Group Photo
9:40am	**Break**
10:00am	**MTL Start-up Elevator Pitch Presentations (Part 1)**
10:45am	**Research Update 1: MTL Centers** *Ahmad Bahai, Ruonan Han, Jeehwan Kim*
12:00pm	**Lunch**
1:00pm	**Research Update 2: Faculty Research Highlights** *Duane Boning, Joseph Casamento, Jing Kong, Farnaz Niroui*
2:00pm	**MTL Start-up Elevator Pitch Presentations (Part 2)**
3:15pm	**Break**
3:30pm	**MIT.nano Update** *Vladimir Bulović*
3:45pm	**Discussion with faculty**
4:15pm	**IAB discussion and feedback to MTL leadership**
5:00pm	**Adjourn**

MIG MEMBER BIOGRAPHIES

Clifford King
Sr. Director of External Engagement
Analog Devices

Cliff King is Sr. Director of External Engagement at Analog Devices in Wilmington, MA. He received his Ph.D. in EE from Stanford Univ. where he fabricated the world's first SiGe heterojunction bipolar transistor in 1988 using chemical vapor deposition, the dominant technique used today. He was a Distinguished Member of Technical Staff and manager at Bell Laboratories in Murray Hill, NJ where he led a team that developed and placed a high-speed SiGe BiCMOS process into production for optical networking and wireless applications. In 2002, he founded NoblePeak Vision Corp. to produce shortwave infrared cameras using a low dark current Ge-enhanced CMOS image sensor process. He joined L-3 Technologies in 2010 as CTO of the Warrior Systems Division before coming to Analog Devices in 2022. He is a Fellow of the IEEE.

Dr. Marc Ulrich
Advanced Electronics Branch Chief
DEVCOM - Army Research Laboratory

David Carter
Laboratory Fellow
Draper

Dr. Marc Ulrich received his Ph.D. in Physics from Auburn University in 2001 with an emphasis on modeling of thermoelectric and thermionic properties of materials. He was subsequently a National Research Council Postdoctoral Fellow working with the Army Research Laboratory at North Carolina State University where he utilized the National Synchrotron Light Source to study interface states in high-k dielectrics for field effect transistors including hafnia, zirconia and various oxide solid solutions. In 2003, he joined the Army Research Office as the program manager for the Condensed Matter Physics program. As a program manager, he supported work advancing strongly correlated phenomena and other emerging physics in complex oxides, 2D, topological and other electronic materials. In 2022, he transferred to the intramural research directorate of the DEVCOM Army Research Laboratory to lead the Advanced Electronics branch. In this role, he directs efforts in the study of emerging materials such as topological and 2D materials, devices such as neuromorphic device primitives and circuits such as mixed signal artificial intelligence accelerators.

Dr. David Carter is a Laboratory Fellow at Draper Laboratory. He has been at Draper for 23 years, where he has led efforts to apply nanofabrication and nanotechnology in a variety of areas including RF MEMS, integrated optics, plasmonic devices, carbon nanotube MEMS/NEMS integration, medical devices, and advanced packaging of electronic devices. His work in molded nanoscale polymers led to the first-ever demonstration of human climbing using biomimetic synthetic gecko adhesion. He has advised several graduate Draper Scholars and has initiated multiple collaborations with university researchers while at Draper.

Prior to Draper, he held a research staff position at MIT, where he led the development of zone-plate-array lithography (ZPAL). Before MIT, he held a staff position at Harvard University, where he managed the cleanroom facility. Dr. Carter received his Ph.D. in Electrical Engineering from MIT and his A.B. and M.S. degrees in Engineering Sciences from Dartmouth College. He has co-authored 35 journal and conference papers and has 21 patents in micro/nanofabrication, nanotechnology, and materials.

George Courville
Business Development Manager, Technology
Edwards

George has over 25 years of experience as a marketing and business development professional. His career has included senior management positions with both large, multi-national corporations as well as small, nanotechnology start-ups. He has led global business development teams offering high performance materials and equipment for many uses in semiconductor, display, solar and other high technology markets. He was responsible for managing a marketing and applications team that introduced and supported the first dry vacuum pumps for the semiconductor market.

George received his Bachelor of Science degree in Chemical Engineering from Tufts University, and an MBA from Boston University.

Anthony Taylor
Applications Technologist
Edwards

Anthony has over 30 years' experience working in the semiconductor industry and conducting research in thin film technology and microsystems. He has been with Edwards, Sanborn, New York, as an Applications Engineer and Applications Technologist for the past 28 years and a visiting scientist at MIT since 2014. His work at MIT has focused on novel fabrication methods of micro and nano-systems, specifically graphene-based gas sensors for vacuum and exhaust management applications, and 3D-printed miniature vacuum and liquid pumps. He received a Bachelor of Science degree in Physics (cum laude) from Saint Lawrence University, a Master of Science degree in Physics from the University of Arizona, and the Doctor of Philosophy in Physics from Rensselaer Polytechnic Institute (RPI).

Fredrik Dahlgren
Head of Device Platform Research
Ericsson Research

Greg Bartlett
Chief Technology Officer
GlobalFoundries

Fredrik Dahlgren is Head of Device Platform Research at Ericsson Research. He is also an Adjunct Professor at Chalmers University of Technology. Before this, he was Director of WARA, the Research Arenas of the Wallenberg Autonomous Systems and AI research program, during 2016-2017, and in that role he was also a Guest Professor at Linköping University. Fredrik Dahlgren has a PhD in Computer Architecture from Lund University in 1994. He was a visiting scientist at MIT 1995/1996 after which he became an associate professor at Chalmers. From 1999, he has been with Ericsson Group in various leading positions, including Head of Research at Ericsson Mobile Platforms, Head of Technology Management in the CTO Office (ST-Ericsson), and system architecture program manager for highly integrated multi-core and multimedia-centric smartphone platforms at ST-Ericsson.

Gregg Bartlett is Chief Technology Officer for GF, a position he was appointed to in 2022. He leads the company's core technology and gf Labs' functions to drive innovation and long-range R&D portfolio by partnering with key universities and institutions for GF's differentiated technology capabilities.

Mr. Bartlett has served in various senior executive roles at GF in technology and business since 2009. Before joining GF, Mr. Bartlett spent 25 years in technical and management positions at Freescale Semiconductor and Motorola. In support of the CHIPS and Science Act, Mr. Bartlett serves on the Industrial Advisory Committee. He represents GF on the Purdue Semiconductor Degree Program Leadership Board. He also serves on the Governing Council for SRC's JUMP program. Mr. Bartlett serves as a board member of the Carbice Corporation.

Mr. Bartlett holds a bachelor's degree in Chemical Engineering from Kansas State University.

Ted Letavic
Corporate Fellow
Senior Vice President of Technology
GlobalFoundries

Ted Letavic is a Corporate Fellow and Senior Vice President of Technology Innovation at GlobalFoundries. He is a group leader with technical roadmap responsibility for solution architecture and semiconductor innovation in market segments that include compute and datacenter, wired and wireless infrastructure, mobility, industrial/IoT/ATV, and high speed communications. His recent research interests include silicon photonics, sub tera-Hertz semiconductor devices, analog compute-in-memory, and quantum systems. He has over 60 US patents granted, has authored over 70 reviewed scientific papers, and serves on numerous academic and industrial advisory boards. He received a PhD in Electrical Engineering from Rensselaer Polytechnic Institute.

Hiroshi Suzuki
General Manager, Technology Strategy Division
Hitachi High-Tech

Dr. Hiroshi Suzuki is the General Manager of the Technology Strategy Division of Hitachi High-Tech (HHT) headquarters in Tokyo and is responsible for the technology strategy of the HHT group.

He joined Central Research laboratory (CRL), Hitachi Ltd. in 1989, and researched electron-beam instruments for improving yields of semi-conductor and/or magnetic devices. He developed several methods and apparatuses to characterize the electrical properties of LSIs and to analyze the magnetic properties of several magnetic devices used in HDDs. He received academic awards including the Technology Development Award (JIM, 1999) and the Technology Award (JSPE, 2003). As a part of his carrier in Hitachi, he worked in research planning at CRL for several years, and he was temporary transferred to the corporate venture capital (CVC) of Hitachi's R&D division from 2004 to 2005.

He moved to Hitachi High-Technologies Corporation in 2011, where he was in charge of R&D planning and strategy, and he was temporary transferred to the HHT's subsidiary company to develop new technologies for inspection of social infrastructure from 2016 to 2018.

He graduated with his Bachelor's and Master's degrees in precision engineering from Tohoku University in 1987 and 1989. He obtained a Ph.D. in engineering from Tohoku University in 2007 when he worked for CRL, Hitachi Ltd.

Junichi Tanaka
Senior Chief Engineer
Chief Technology Officer of Nano-technology Solution Business Group
Hitachi High-Tech

Dirk Pfeiffer
Director, Microelectronics Research Laboratory
IBM

Junichi Tanaka is the Senior Chief Engineer and Chief Technology Officer of Nano-technology Solution Business Group at Hitachi Hightech. He is dedicated to the careful monitoring and control of semiconductor device fabrication processes. Dr. Tanaka's first research was designing plasma process simulators and crafting monitoring tools specifically for plasma etchers. From 1998 to 1999, he was a Visiting Scholar at the University of California, Berkeley. During this tenure, he spearheaded the development of a pioneering force-potential model, which facilitated molecular dynamics simulations of SiO2 reactive ion etching, providing predictions of etched pattern shapes.

He innovated various techniques to enhance etched profiles by harnessing the power of plasma spectra and integrating a customized FTIR wall monitor. These advancements paved the way for his involvement in a comprehensive Advanced Process Control (APC) project.

In 2008, he was awarded the Semicon-Japan Technology Symposium Award. A significant component of this achievement hinged on the consistent repeatability of CDSEM measurements. His current work is focused on exploring state-of-the-art technologies within the realms of metrology and inspection. Dr. Tanaka especially interested in various time-domain metrologies employing both lasers and electron beams.

Dr. Dirk Pfeiffer is the director of the Microelectronics Research Laboratory (MRL) at the IBM TJ Watson Research Center. The MRL is a semiconductor R&D facility with key capabilities including a 200mm wafer scale fabrication line, die and wafer level packaging & assembly, surface mount technology, characterization and other for advanced prototyping and process development of new materials and devices. The key mission of the MRL is to accelerate technologies from early stages of innovation to wafer scale development and manufacturing ("Lab to Fab" prototyping). Its project portfolio include quantum, semiconductor device and materials development, embedded analog devices for memory and AI applications, IoT and biomedical devices for health care applications, 2.5 and 3D packaging development and cooling and others. Dr. Dirk Pfeiffer has 25 years of experience in semiconductor and material process development as well as building and operating semiconductor fabrication facilities. He is author and coauthor of 80 plus patents, publications as well as several IBM outstanding technology achievement awards and has a PhD in Chemistry.

Ali Khakifirooz
Principal Engineer
Intel Foundry Technology Development

Esther Jeng, Ph.D.
Senior Manager of Open Innovation
Lam Research Corporation

Ali Khakifirooz is a Principal Engineer at Intel Foundry Technology Development, working on logic technology pathfinding. Prior to his current rule and since joining Intel in 2015, he worked on 3D-integrated embedded memory and multiple generations of 3D NAND technology from 64-tier to +200-tier. He managed the 3D NAND Media Architecture Pathfinding and was part of the team that developed and qualified the industries first 4-bit-per-cell technology in 2018 and the first 5-bit-per-cell technology in 2022.

Earlier in his career, Ali worked at IBM Research, were he developed the fully-depleted SOI technology and made key contributions to the development of 10nm and 7nm technologies. He received his BS and MS degrees from the University of Tehran in 1997 and 1999, respectively, and his PhD from MIT in 2007. He has published more than 100 technical papers, holds more than 750 US Patents, and was named an IEEE Fellow in 2019.

Dr. Esther Jeng is senior manager of open innovation in the Office of the CTO at Lam Research where she connects emerging technologies to Lam's semiconductor products for manufacturing new generations of chips. She manages a portfolio of exploratory technologies in partnership with university and startup ecosystems to find solutions to the industry's grand challenges. Esther has held multiple roles at Lam, leveraging 14 years of experience in ALD and CVD metals thin-film deposition. She has collaborated closely with leading-edge customers and led globally located engineering teams to develop products from initial power-up in the lab to high-volume production for logic and memory fabrication. Her areas of expertise include plasma and thermal thin film deposition, chemical process development and precursor handling in vacuum systems, and defect management. Her first immersion into engineering was at MIT where she learned to foster technical discourse and execution at all levels, from the use of liquid nitrogen to make the smoothest ice cream to the development of fluorescent carbon nanotube sensors. She believes that the most robust solutions are developed from open discussions where everyone contributes. Esther earned B.S. and Ph.D. degrees from MIT and an M.S. from the University of Illinois Urbana-Champaign in chemical engineering and has authored several papers and patents. She enjoys exploration: from cities worldwide to seedlings sprouting in her backyard.

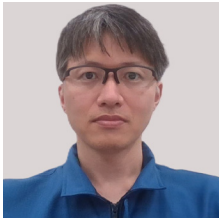
Anand Murthy
Vice President of Advanced Technology Integration
Lam Research Corporation

Keith Lynn
General Manager and Site Lead for the Space Microelectronics R&D Center
Lockheed Martin

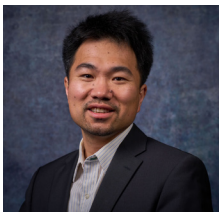
Anand Murthy is the Vice President of Advanced Technology Integration within the Office of the CTO at Lam Research Corporation. Anand manages various process technology initiatives in Logic and Memory with several research consortia fostering strong integration and collaboration. Prior to joining Lam this year, Anand was an Intel Fellow with over 28 years of technical and leadership experience in advancing Moore's law of transistor scaling. Anand holds 320 U.S. patents granted for pioneering work in the fabrication of CMOS and HBT transistors based on Si, SiGe, Ge and III-V compound semiconductor materials. Anand graduated from University of Southern California with Ph.D. in Materials Science and Engineering in 1993.

Keith Lynn is General Manager and site lead for the Space Microelectronics R&D Center at Lockheed Martin (LM). Since taking this position in 2020, Keith has expanded the 5,000 sq. ft. laboratory capability to create LM's only Gallium nitride fabrication line and state-of-the-art anti-tamper hardware device fabrication. With over $2M in capital investment, the Center is now leading strategic efforts for edge digital processing and next-gen hypersonic strike.

In addition to program execution, Keith has supported Corporate in the development of multiple Fortune 100 partnerships. This includes MoU and co-bidding efforts with Intel, GlobalFoundries, and Microsoft, with additional support to GE, GM, and IBM relationship development. Keith was also nominated as the LM representative to NextFlex's Governing Council, where he helps shape future research programs toward top DoD needs.



Saneaki Ariumi
Senior Manager, Next Generation
Telecommunication Business Development Office
Murata Manufacturing Co.,Ltd.



Rui Ma
Director of mmWave PA Systems
Murata Electronics North America, Inc.

Saneaki Ariumi joined the Murata Manufacturing Company, Ltd., Kyoto, Japan, in 2001. He has been with IMEC, Leuven, Belgium, as an Industrial Resident for the Murata Manufacturing Company, Ltd., from 2012 to 2015.

He is currently the Senior Manager of the Next Generation Telecommunication Business Development Office, where he was involved in research and development efforts in sub-THz, mm-wave module, RF front-end and network system.

Dr. Rui Ma is currently a Director of mmWave PA Systems at pSemi, A Murata Company. Prior to joining pSemi, he was with Mitsubishi Electric Research Labs working in the area of RF devices and circuits research. Dr. Ma was a Visiting Scientist with THz Integrated Electronics Group at MIT. He currently serves as an IEEE Distinguished Microwave Lecturer (DML).

Johan Suzuki
Manager, Corporate Technology & Innovation
Murata Electronics North America, Inc.

Sota Kagami
Researcher, Secure System Platform Research Laboratories
NEC Corporation

Johan Suzuki is a Corporate Technology & Innovation Manager at Murata Manufacturing Co., Ltd. Since 2024, he has been engaged as a Visiting Scientist at MIT, aiming to strengthen the company's R&D through industry-academia collaboration. The research in his group focuses on next-generation communication / 6G, optics & semiconductors, the environment, and bioelectronics.

He began his career at Murata in 2015, where he was responsible for the design of wireless communication modules at the headquarters in Kyoto, Japan. From 2020 to 2024, he served as Corporate Venturing Manager in San Jose, CA, contributing to developing partnerships with startups and creating new business opportunities.

He received his B.S. and M.S. degrees in electrical engineering from Keio University. Prior to joining Murata, he worked as an RF engineer involved in the design of PCs and smartphones.

Mr. Sota Kagami is a Researcher at NEC Secure System Platform Research Laboratories. His research has focused on quantum sensing, including atomic clocks based on atomic vapor cells and cold atoms. He received B.S. and M.S. degrees in physics from Tokyo Institute of Technology, Japan, in 2007 and 2009, respectively. He joined NEC Corporation in 2009 and engaged in the research and development of infrared detectors based on semiconductor nanostructures. From 2016 to 2017, he joined NIST in Boulder, Colorado, U.S. as a visiting scholar and was engaged in developing atomic optical magnetometers. His research interests include devices and sensors based on quantum nanostructures, superconducting circuits, atoms, and nitrogen vacancy centers in diamond.

Dr. Ionut Radu
Senior Director, Emerging Technologies
Soitec

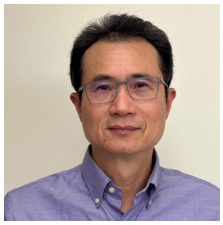
Cesar Roda Neve
R&D Program Manager
Soitec

Ionut Radu is Senior Director, Emerging Technologies at Soitec. He leads the path finding and worldwide partnerships with industrial and academic innovation platforms supporting strategic developments of engineered substrate technologies for semiconductor industry.

Dr. Radu obtained his B.S. and Ph.D in physics from University of Bucharest and Martin-Luther University Halle-Wittenberg respectively. Dr. Radu has 25 years of experience in semiconductor and material development and he has co-authored more than 100 papers in peer-reviewed journals, conference proceedings and reference handbooks and holds 80 patents. Ionut is an IEEE Fellow and he serves on several IEEE conference committees.

Cesar Roda Neve was born in Madrid, Spain, in 1975. He received the Msc. Engineer degree from the ICAI Universidad Pontificia de Comillas, Madrid, Spain, in 2000. In 2012, he received the Ph.D. degree in engineering sciences from the Université catholique de Louvain (UCL), Belgium. From 2004 to 2006, he was with the Electronics Department of the University Carlos III of Madrid, Spain, where he worked on ROF links and optoelectronic devices. From 2006 to 2012, he joined the Microwave Laboratory at the Université catholique de Louvain (UCL), Belgium, where he worked on the characterization and application of Si-based substrates for RF integration, in particular the use of HR-Si, HRSOI, and trap-rich HR-SOI substrates, non-linearities and parasitic effects. From 2013 to 2016 he was with the 3D and Optical Technology group of IMEC, Leuven, Belgium, focusing on new technologies development with special attention to 2.5D, 3D stacking and packaging. From 2016 to 2021 he worked at M3 Systems Belgium, as senior project manager and coordinator on GNSS related projects and satellite / UAV communications, in close cooperation with the European Space Agency. In 2021 he joined SOITEC as R&D Program Manager working on strategic research for applications and products, mainly focusing on RF, 6G, quantum, and advanced CMOS technologies.

Cesar Roda Neve
R&D Program Manager
Soitec



Tony Shao
Department Manager, Forward Looking Program PDF for System Integration
TSMC

Cesar Roda Neve was born in Madrid, Spain, in 1975. He received the Msc. Engineer degree from the ICAI Universidad Pontificia de Comillas, Madrid, Spain, in 2000. In 2012, he received the Ph.D. degree in engineering sciences from the Université catholique de Louvain (UCL), Belgium. From 2004 to 2006, he was with the Electronics Department of the University Carlos III of Madrid, Spain, where he worked on ROF links and optoelectronic devices. From 2006 to 2012, he joined the Microwave Laboratory at the Université catholique de Louvain (UCL), Belgium, where he worked on the characterization and application of Si-based substrates for RF integration, in particular the use of HR-Si, HRSOI, and trap-rich HR-SOI substrates, non-linearities and parasitic effects. From 2013 to 2016 he was with the 3D and Optical Technology group of IMEC, Leuven, Belgium,

Dr. Tony Shao is department manager of Pathfinding for System Integration at Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC). He received his BSc degree from National Cheng Kung University, MSc degree from National Taiwan University, and PhD degree on materials science from National Chiao Tung University in Taiwan.

Tony served in a variety of roles throughout his career including R&D in system integration technologies including Flip-Chip, Fan-In, Fan-Out, and direct bonding. Before joining TSMC, Dr. Shao was a senior R&D manager at AU Optronics Corporation in Taiwan, and responsible for LCD display development from 2002 to 2008. He has received more than 50 worldwide patents.

Jim Wieser
Director of University Research and Technology
Texas Instruments

Michael H. Perrott
Systems Engineer
Texas Instruments

Jim serves Texas Instruments as Director of University Research and Technology within the university relations organization in close collaboration with the CTO Office. In this role he identifies and drives strategic technology initiatives, research strategy and aligns university research to the needs of the company. His semiconductor experience spans over 40 years in the areas of design, product development management and technologist. He is an IEEE Senior Member and SRC Executive Technical Advisory Board member for TI.

Jim received his BSEE and MSEE from University of Michigan and joined National Semiconductor starting his career in the semiconductor industry. He began as a circuit designer in the pioneering days of analog CMOS, including switched capacitor filters and data converters. Jim developed circuits and managed design of telecom products, including voice band codecs, modems, ISDN and ADSL. Jim spent two years as Director/VP of Analog/Mixed Signal Methodology refining the analog design flow to address National's SoC product strategy. Later he led the development of 10/100 and Gigabit Ethernet Phys and MACs in the Networking division as Design Director. In 2002 Jim was promoted to Chief Technologist of the Interface Division and was later promoted to Chief Technologist for the Product Group covering four product divisions. He later joined the CTO office to drive strategic technology and university research. Jim holds 21 patents in the area of analog circuits and system design.

Michael H. Perrott received the B.S. degree in electrical engineering from New Mexico State University, Las Cruces, NM, and the M.S. and Ph.D. degrees in electrical engineering and computer science from Massachusetts Institute of Technology (MIT), Cambridge, MA. He was a visiting Assistant Professor with the Hong Kong University of Science and Technology in 1999, was an Assistant and then Associate Professor with the Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA from 2001 to 2008, and was a Professor with the Masdar Institute of Science and Technology, Abu Dhabi, UAE, from 2011 to 2013. He has worked in industry at Hewlett-Packard Laboratories, Palo Alto, CA (1999), Silicon Laboratories, Austin, TX (1999-2001, 2013-2014), SiTime Corporation, Sunnvale, CA (2008-2010), Invensense, San Jose, CA (2014-2019), and is now at Texas Instruments, Manchester, NH as of 2019. His key areas of interest include high performance timing circuit architectures, such as wide bandwidth, low jitter fractional-N phase-locked loops, and precision circuit architectures. He is a Fellow of the IEEE.

MTL LEADERSHIP BIOGRAPHIES

Tomás Palacios

Director, Microsystems Technology Laboratories
Clarence J. LeBel Professor, Department of Electrical Engineering & Computer Science

Tomás Palacios is the Clarence J. LeBel Professor in the Department of Electrical Engineering and Computer Science at MIT. He received his PhD from the University of California - Santa Barbara in 2006, and his undergraduate degree in Telecommunication Engineering from the Universidad Politécnica de Madrid (Spain). His current research focuses on demonstrating new electronic devices and applications for novel semiconductor materials such as graphene and gallium nitride. His work has been recognized with multiple awards including the Presidential Early Career Award for Scientists and Engineers, the IEEE George Smith Award, and the NSF, ONR, and DARPA Young Faculty Awards, among many others. Prof. Palacios is the founder and director of the MIT MTL Center for Graphene Devices and 2D Systems, as well as the Chief Advisor and co-founder of Cambridge Electronics, Inc. He is a Fellow of IEEE.

Ruonan Han

Associate Director, MTL
Associate Professor, Department of Electrical Engineering and Computer Science
Director of MTL Center of Integrated Circuits and Systems

Ruonan received his B.S. degree in microelectronics from Fudan University, China, in 2007, M.S. degree in electrical engineering from University of Florida in 2009, and Ph.D. in electrical and computer engineering from Cornell University in 2014. He joined MIT in July 2014 and is now an associate professor at the Department of Electrical Engineering and Computer Science. His research group aims to explore microelectronic circuits and systems to bridge the terahertz gap between microwave and infrared domains. He has served on the committees of a few conferences, including the technical-program committee (TPC) of IEEE International Solid-State Circuits Conference (ISSCC) (2022~present), IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium (2017~present), and 2019 International Microwave Symposium (IMS) Steering Committee. He was the associate editor of the IEEE Transactions on Quantum Engineering (2020~present) and IEEE Transactions on Very-Large-Scale Integration (VLSI) Systems (2018~2021), and the Guest Editor of the IEEE Transactions on Microwave Theory and Techniques (T-MTT) (2019). He is the 2020~2022 Distinguished Microwave Lecturer of IEEE Microwave Theory Techniques Society (MTT-S). Ruonan is the recipient of three Best Student Paper Awards from IEEE RFIC Symposium (2012, 2017 and 2021), NSF Faculty Early CAREER Development Award (2017), Intel Outstanding Researcher Award (2019) and the IEEE Solid-State Circuit Society New Frontier Award (2023). In 2023, he was appointed as the Associate Director of Microsystem Technology Laboratories (MTL) and Director of MTL Center of Integrated Circuits and Systems (CICS).

Bilge Yildiz

Associate Director, MTL
Professor, Department of Nuclear Science and Engineering

Bilge Yildiz is the Breene M. Kerr (1951) Professor at Massachusetts Institute of Technology, where she leads the Laboratory for Electrochemical Interfaces. Yildiz's research focuses on laying the scientific groundwork to enable next generation electrochemical devices for energy conversion and information processing. Yildiz's teaching and research efforts have been recognized by the Argonne Pace Setter (2006), ANS Outstanding Teaching (2008), NSF CAREER (2011), IU-MRS Somiya (2012), the ECS Charles Tobias Young Investigator (2012), the ACerS Ross Coffin Purdy (2018) and the LG Chem Global Innovation Contest (2020) awards. She is a Fellow of the American Physical Society (2021), the Royal Society of Chemistry (2022), and the Electrochemical Society (2023) and an elected member of the Austrian Academy of Science (2023)

2024 ANNUAL RESEARCH REPORT

MTL MICROSYSTEMS TECHNOLOGY LABORATORIES

IN APPRECIATION OF OUR MTL INDUSTRIAL GROUP MEMBER COMPANIES:

Analog Devices
Applied Materials
Draper
Edwards
Ericsson
GlobalFoundries
Hitachi High-Tech
IBM
Intel
Lam Research Corp.
Lockheed Martin
muRata
NEC
Soitec
TSMC
Texas Instruments